

Universal Serial Bus 4 (USB4[®]) Specification

Apple Inc.
HP Inc.
Intel Corporation
Microsoft Corporation
Renesas Corporation
STMicroelectronics
Texas Instruments

Version 2.0 ~~with Errata and ECN through September 25, 2024~~

November 2025~~September 2024~~

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1 Introduction

1.1 Scope of the Document

This specification is primarily targeted at peripheral developers and platform/adaptor developers, but provides valuable information for platform operating system/BIOS/device driver, adaptor independent hardware vendors/independent software vendors, and system OEMs. This specification can be used for developing new products and associated software.

1.2 USB Product Compliance

Adopters of the USB4® specification have signed the USB4 Adopters Agreement, which provides them access to a royalty-free reasonable and nondiscriminatory (RAND) license from the Promoters and other Adopters to certain intellectual property contained in products that are compliant with the USB4 specification. Adopters can demonstrate compliance with the specification through the testing program as defined by the USB Implementers Forum (USB-IF). Products that demonstrate compliance with the specification will be granted certain rights to use the USB-IF logos as defined in the logo license.

1.3 Document Organization

Chapters 1 and 2 provide an overview for all readers, while Chapters 3 through 13 contain detailed technical information defining USB4.

1.4 Design Goals

USB 3.1 and USB 3.2 were evolutionary steps to increase bandwidth. The goal for USB4 remains the same with the added goal of helping to converge the USB Type-C® connector ecosystem and minimize end-user confusion. Several key design areas to meet this goal are listed below:

- Offer display, data, and load/store functionality over a single USB Type-C connector.
- Retain compatibility with existing ecosystem of USB and Thunderbolt™ products.
- Define Port Capabilities for predictable and consistent user experience.
- Provide increased host flexibility to configure bandwidth, power management, and other performance-related parameters for system needs.

1.5 Related Documents

Universal Serial Bus 3.2 Specification, Revision 1.0, September 22, 2017 (USB 3.2 Specification)

USB Type-C® Cable and Connector Specification, Release 2.2, October 2022 (USB Type-C Specification)

USB 3.0 Jitter Budgeting white paper (USB Jitter Paper)

Universal Serial Bus Power Delivery Specification, Revision 3.1, Version 1.6, October 2022 (USB PD Specification)

PCI Express® Base Specification, Revision 4, Version 1, September 27, 2017 (PCIe Specification)

PCI Express® Base Specification, Revision 5.0, Version 1.0, 22 May 2019 (PCIe Specification)

VESA DisplayPort™ Standard, Revision 1.2a, May 2012 (DisplayPort 1.2a Specification)

VESA DisplayPort™ Standard, Revision 1.4a, April 19, 2018 (DisplayPort 1.4a Specification)

VESA DisplayPort™ Standard, Revision 2.1, October 10, 2022 (DisplayPort Specification)

VESA DisplayPort™ 1.4a PHY Layer Compliance Test Specification, Revision 1.0, 27 July, 2018 (DisplayPort 1.4a PHY CTS)

VESA DisplayPort™ 2.1 PHY Layer Compliance Test Specification, Revision 1.0 [Release Date TBD] (DisplayPort PHY CTS)

VESA DisplayPort™ Alt Mode on USB Type-C Standard, Revision 2.0, June 26, 2019 (DisplayPort Alt Mode Specification)

eXtensible Host Controller Interface for Universal Serial Bus, Revision 1.2, May 2019 (xHCI Specification)

USB4 Connection Manager (CM) Guide, Revision 1.0, April 2021 – (Connection Manager Guide)

USB4 Re-Timer Specification, Version 1.0, October 2021 – (USB4 Re-Timer Specification)

USB4 Device ROM (DROM) Specification, Revision 1.0, February 2021 – (USB4 DROM Specification)

USB4 Inter-Domain Service Protocol, Version 1.0, November 2021 – (USB4 Inter-Domain Specification)

HDCP on DisplayPort™ Specification, Revision 2.3, January 22, 2019 (HDCP Specification)

1.6 Conventions

1.6.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and then text.

Note: The text, figures, and tables in this specification all contain necessary information for building an implementation and need to be read together to get a full understanding of USB4 technology.

1.6.2 Keywords

The following keywords differentiate between the levels of requirements and options.

1.6.2.1 Informative

Informative is a keyword that describes information with this specification that intends to discuss and clarify requirements and features as opposed to mandating them.

1.6.2.2 May

May is a keyword that indicates a choice with no implied preference.

1.6.2.3 N/A

N/A is a keyword that indicates that a field or value is not applicable and has no defined value and shall not be checked or used by the recipient.

1.6.2.4 Normative

Normative is a keyword that describes features that are mandated by this specification.

1.6.2.5 Optional

Optional is a keyword that describes features not mandated by this specification. However, if an optional feature is implemented, the feature shall be implemented as defined by this specification (optional normative).

1.6.2.6 Reserved

Reserved is a keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. The use and interpretation of these may be specified by future extensions to this specification and, unless otherwise stated, shall not be utilized or adapted by vendor implementation. A reserved bit, byte, word or field shall be set to zero by the sender and

shall be ignored by the receiver. Reserved field values shall not be sent by the sender and, if received, shall be ignored by the receiver.

1.6.2.7 Shall

Shall is a keyword indicating a mandatory (normative) requirement. Designers are mandated to implement all such requirements to ensure interoperability with other compliant devices.

1.6.2.8 Should

Should is a keyword indicating flexibility of choice with a preferred alternative. Equivalent to the phrase “it is recommended that”.

1.6.3 Capitalization

Some terms are capitalized to distinguish their definition in the context of this specification from their common English meaning. Words not capitalized have their common English meaning.

1.6.4 Italic Text

Italic text is used to identify variable names, register field and packet field names, or reference document titles.

1.6.5 Numbering

Numbers that are immediately followed by a lowercase “b” (e.g. 01b) are binary values. Numbers that are immediately followed by an uppercase “B” are byte values. Numbers that are immediately followed by a lowercase “h” (e.g. 3Ah) are hexadecimal values. Numbers not immediately followed by either a “b”, “B”, or “h” are decimal values.

1.6.6 Bit, Byte, DW, and Symbol Conventions

A bit, byte, DW, or Symbol residing in location *n* within an array is denoted as bit(*n*), byte(*n*), DW(*n*), or Symbol(*n*).

A sequence of bits, bytes, DWs, or Symbols residing in locations *n* to *m* (inclusive) within an array is denoted as bit[*m:n*], byte[*m:n*], DW[*m:n*], or Symbol[*m:n*].

1.6.7 Implementation Notes

Implementation Notes are not a normative part of this specification. They are included for clarification and illustration only. Implementation Notes within this specification are marked as such and set apart from the other text.

1.6.8 Connection Manager Notes

Connection Manager Notes provide requirements and recommendations for building a Connection Manager. Connection Manager Notes within this specification are marked as such and set apart from the other text.

Router behavior is undefined if a Connection Manager does not follow the requirements in a Connection Manager Note.

See the Connection Manager Guide for an example Connection Manager implementation.

1.6.9 Pseudocode

Throughout this specification, pseudocode is used to illustrate operating principles. Comments are demarcated by double forward slashes (“//”). The pseudocode conventions include:

```
if/else conditions;
    if (condition)
        // true operations
    else
        // false operations
```

```
for loops:
    for (conditions)
        // operations
```

1.6.10 CRC Algorithms

The CRC algorithms used in the specification are defined according to the following values:

- **WIDTH:** This is the width of the algorithm expressed in bits. This is one less than the width of the POLY.
- **POLY:** This is a binary value that should be specified in a hexadecimal number. The top bit of the polynomial should be omitted. For example, if the polynomial is 10110, the POLY equals 06. An important aspect of this parameter is that it represents the un-reflected polynomial; the bottom bit of this parameter is always the LSB of the divisor during the division regardless of whether the algorithm being modeled is reflected.
- **INIT:** This parameter specifies the initial value of the register when the algorithm starts. This is the value that is to be assigned to the register in the direct table algorithm. In the table algorithm, we may think of the register always commencing with the value zero, and this value being XORed into the register after the Nth bit iteration. This parameter should be specified as a hexadecimal number.
- **REFIN:** This is a Boolean parameter. If it is FALSE, inputs bytes are processed with bit 7 being treated as the most significant bit (MSB) and bit 0 being treated as the least significant bit. If this parameter is TRUE, each byte is reflected before being processed.
- **REFOUT:** This is a Boolean parameter. If it is set to FALSE, the final value in the register is fed into the XOROUT stage directly, otherwise, if this parameter is TRUE, the final register value is reflected first.
- **XOROUT:** This is a W-bit value that should be specified as a hexadecimal number. It is XORed to the final register value (after the REFOUT) stage before the value is returned as the official checksum.

For more information, see *A Painless Guide to CRC Error Detection Algorithms*, by Ross N. Williams, Version 3, August 19, 1993.

1.6.11 FourCC

A FourCC is a sequence of four bytes used to represent ASCII strings. It is limited to ASCII printable characters (one byte per character), with space characters reserved for padding shorter sequences.

For example, the FourCC string “ABC” is represented by a hexadecimal value of 20434241h, where the rightmost byte (41h) represents the first ASCII character (“A”).

1.6.12 Lists

When a list contains numbering and/or lettering, then the ordering of the items follows the numerical and alphabetical ordering of the list. For example, item 1 must occur first, followed by item 2, then item 3, etc. When a list contains multiple levels of ordering, then each substep must be completed before moving on to the next step. For example, in a list with three substeps, steps 1a, 1b, then 1c, must occur before moving on to step 2.

When a list is bulleted, then the ordering of the items does not matter and the listed items may occur in any order.

1.7 Terms and Abbreviations

This section lists and defines the terms and abbreviations used throughout this specification. Note that terms and abbreviations not defined here, use their generally accepted or dictionary meaning.

Term/Abbreviation	Description
Active Cable	A cable with additional electronics to condition the data path signals.
Adapter	An addressable Router interface that includes additional functionality based on type. There are three types of Adapters: Lane Adapter, Protocol Adapter, and Control Adapter.
Adapter Configuration Space	The Configuration Space for Lane Adapters and Protocol Adapters. Control Adapters do not have an Adapter Configuration Space.
Aggregated Link	A USB4 Link that uses two bonded Lanes to transmit and receive data. An Aggregated Link can be a Symmetric Link or an Asymmetric Link.
Asymmetric Link	An Aggregated Link that operates with 3 Transmitters and 1 Receiver on one side of the Link and 3 Receivers and 1 Transmitter on the other side of the Link. Only Gen 4 Links can support operation as an Asymmetric Link.
AT Transaction	A type of Transaction that is used by a Router to read from or write to the SB Register Space of a Link Partner.
Big Endian	A method of storing data that places the most significant byte of multiple-byte values at a lower storage address. For example, a 16-bit integer stored in Big Endian format places the least significant byte at the higher address and the most significant byte at the lower address. See also Little Endian.
Bit Error Rate (BER)	The ratio between the number of incorrect bits received to the total number of received bits.
Byte	A data element that is 8 bits in size.
Cable Re-timer	A Re-timer that is part of an Active Cable.
Captive Device	A Captive Device is device that is plugged directly to a USB Type-C Receptacle. A Captive Device can include a cable at its front-end as an integral part, providing access to a single test point at the connector.
CLx	Refers to any of CL0s, CL1, and/or CL2 Adapter states. Also referred to as Low Power states.
Configuration Layer	The protocol stack layer responsible for configuration tasks and handling Control Packets.
Configuration Space	An address space used by the Connection Manager to access a set of configuration registers. The USB4 architecture defines four Configuration Spaces: Router Configuration Space, Adapter Configuration Space, Path Configuration Space, and Counters Configuration Space.
Connection Manager (CM)	The software-based configuration entity that is responsible for managing a Domain.
Control Adapter	The Adapter within a Router that handles Control Packets and Router configuration tasks. The Control Adapter implements a Transport Layer and a Control Layer. The Control Adapter is assigned Adapter Number = 0.
Control Packet	A type of Transport Layer Packet that is used for configuration-related communication between a Connection Manager and a Router.
Counters Configuration Space	An optional Configuration Space that collects statistics within an Adapter.
Credit	The unit used to track receive buffer space.
Cyclic Redundancy Check (CRC)	A check performed on data to see if an error has occurred in transmitting, reading, or writing the data. The result of a CRC is typically stored or transmitted with the checked data. The stored or transmitted result is compared to a CRC calculated from the data to determine if an error has occurred.
Crosstalk	A situation arising from one transmitted signal inadvertently causing an unwanted effect on another signal. Minimizing or (optimally) preventing cross-talk is a major consideration in maintaining signal integrity.

Term/Abbreviation	Description
Data Dependent Jitter	A specific class of timing jitter. It is a form of deterministic jitter which is correlated with the sequence of bits in the data stream. It is also a form of Inter-Symbol Interference.
dBm	An abbreviation for the power ratio in decibels (dB) of the measured power referenced to one milliwatt (mW).
dequeue	The process of removing a packet from a buffer so that the buffer is free to be used for other packets.
device	A logical or physical entity that performs one or more functions. The entity described depends on the context of the reference. For example, “device” can refer to a single component such as a Router or a Re-timer, or it can refer to a collection of components that perform a particular function such as a USB4 Device.
Device Router	The Router in a USB4 Hub or USB4 Peripheral Device. A Device Router has an Upstream Facing Port and optionally one or more Downstream Facing Ports.
De-Scrambling	Restoring a scrambled bit stream to its original state. See also Scrambling.
De-Skew	The procedure of aligning Symbols received across multiple receivers of a Link with multiple receivers.
Destination Adapter	A Protocol Adapter that is the final recipient of Tunneled Packets routed through the USB4 Fabric. Note that a Protocol Adapter may be a Source Adapter on one Path and a Destination Adapter on another.
Domain	A collection of interconnected Routers managed by a single Connection Manager.
Doubleword, DW	4 bytes.
Down-spread	Spreading a clock frequency downward from a peak frequency. As compared to “center-spread” which evenly splits the frequency around the center frequency.
Downstream	The direction of data flow away from the Connection Manager.
Downstream Facing Port (DFP)	A USB4 Port that is not an Upstream Facing Port. <i>Note: The DFP is not necessarily the power provider. Power roles are determined by USB PD negotiation as defined in the USB PD Specification.</i>
DP	DisplayPort™.
DP Path	A Path that tunnels DP traffic.
DPRX	DisplayPort receiver.
DPTX	DisplayPort transmitter.
Egress Adapter	An Adapter that transmits outgoing traffic.
Electrical Layer	The protocol stack layer that directly interacts with the communication medium between two Routers. The Electrical Layer decouples data transmission electrical specifications from the Logical Layer.
ELT Transaction	Extended LT Transaction. A Type of Transaction that is used by a Router or Re-timer to indicate that an event occurred (such as completion of an operation).
EMI	Electromagnetic interference.
FEC	Forward Error Correction.
Gen 2	Refers to speeds of 10 Gbps (USB4) and/or 10.3125 Gbps (TBT3-Compatibility Mode).
Gen 2 Link	A USB4 Link that is operating at Gen 2 speed.
Gen 2 Router	A Router that supports a maximum of Gen 2 speed.
Gen 3	Refers to speeds of 20 Gbps (USB4) and/or 20.625 Gbps (TBT3-Compatibility Mode).
Gen 3 Link	A USB4 Link that is operating at Gen 3 speed.
Gen 3 Router	A Router that supports a maximum of Gen 3 speed.
Gen 4	Refers to a speed of 40 Gbps.

Term/Abbreviation	Description
Gen 4 Link	A USB4 Link that is operating at Gen 4 speed.
Gen 4 Router	A Router that supports a maximum of Gen 4 speed.
Host Router Clock	The clock that is the ultimate source of time for clock synchronization, either within a single Domain or between multiple interconnected Domains.
Host Router Time	The time as captured from the Host Router Clock.
HopID	A number assigned to a Transport Layer Packet to identify its Path in the context of a Link.
Host	The host computer system that interfaces with a Host Router. A Host includes the host hardware platform (CPU, bus, etc.) and the operating system in use.
Host Interface	The interface between a Host and a Host Router.
Host Router	The Router in a USB4 Host. A Host Router has one or more Downstream Facing Ports. It does not have an Upstream Facing Port (the Host Interface Adapter serves as the Upstream Adapter).
Hub Router	A Device Router with one or more Downstream Facing Port.
Ingress Adapter	An Adapter that receives incoming traffic.
Inter-Domain Link	A USB4 Link that connects two Routers belonging to different Domains.
Internal USB3 Component	Collectively refers to an Internal USB3 Host Controller, Internal USB3 Hub, or Internal USB3 Peripheral.
Internal USB3 Gen T Component	An Internal USB3 Component that supports USB3 Gen T Tunneling.
Internal USB3 Gen X Component	An Internal USB3 Component that supports USB3 Gen X Tunneling.
Internal USB3 Host Controller	The Enhanced SuperSpeed host controller within a USB4 Host.
Internal USB3 Gen T Host Controller	An Internal USB3 Host Controller that supports USB3 Gen T Tunneling.
Internal USB3 Gen X Host Controller	An Internal USB3 Host Controller that supports USB3 Gen X Tunneling.
Internal USB3 Hub	The Enhanced SuperSpeed hub within a USB4 Hub or dock. Only USB3 Gen X Tunneling uses an Internal USB3 Hub.
Internal USB3 Peripheral	The Enhanced SuperSpeed peripheral device within a USB4 Peripheral Device.
Internal USB3 Gen T Peripheral	An Internal USB3 Peripheral that supports USB3 Gen T Tunneling.
Internal USB3 Gen X Peripheral	An Internal USB3 Peripheral that supports USB3 Gen X Tunneling.
Lane	The high speed differential signaling pair that provides communication between two interconnected Routers. The signaling rate at which a Lane operates defines the speed of communication for that Lane.
Lane 0	The Lane associated with the Lane 0 Adapter.
Lane 1	The Lane associated with the Lane 1 Adapter.
Lane Adapter	The Adapter that interfaces to a Lane. A USB4 Port contains two Lane Adapters: a Lane 0 Adapter and a Lane 1 Adapter. A Lane Adapter implements an Electrical Layer, a Logical Layer, and a Transport Layer.
Lane 0 Adapter	The lowest numbered Adapter in a USB4 Port. For example, in a USB4 Port containing Adapters 3 and 4, Adapter 3 is the Lane 0 Adapter.
Lane 1 Adapter	The highest numbered Adapter in a USB4 Port. For example, in a USB4 Port containing Adapters 3 and 4, Adapter 4 is the Lane 1 Adapter.
Lane Bonding	The process of turning two Single-Lane Links into an Aggregated Link. <i>Note: A Gen 4 Link does not explicitly go through a Lane Bonding state. Instead, Lanes are bonded as part of the Lane Initialization process.</i>
Link	See USB4 Link.

Term/Abbreviation	Description
Link Management Packet	A type of Transport Layer Packet that is used to communicate Link-specific information between two Link Partners.
Link Partner	The relationship between the two USB4 Ports on either end of a Link. For example, given two USB4 Ports (Port A and Port B) that are connected by a Link, Port B is the Link Partner of Port A and vice versa.
Little Endian	Method of storing data that places the least significant byte of multiple-byte values at lower storage addresses. For example, a 16-bit integer stored in Little Endian format places the least significant byte at the lower address and the most significant byte at the next address. See also Big Endian.
Local Clock	The free-running clock within a Router. The Local Clock is used for time synchronization purposes.
Local Time	The time as captured from the Local Clock.
Logical Layer	The protocol stack layer below the Transport Layer and on top of the Electrical Layer. The Logical Layer performs Link management tasks and transmission/reception of Symbols over a Link.
LTTPR	LT-tunable PHY Repeater. Defined by the DisplayPort Specification.
LT Transaction	A Type of Transaction that is used by a Router during USB4 Link initialization and to signal a change in Adapter state. See also ELT Transaction.
MFDP	Multi-Function DP. A DisplayPort link which operates as part of a Multi-Function configuration.
Multi-Function	Configuration on the USB Type-C connector that supports USB 3.2 SuperSpeed signaling at the same time as DP Standard signaling.
NVM	Non Volatile Memory.
On-Board Re-timer	A Re-timer that is located between a Router and a USB Type-C connector.
Operation	An action initiated by a Connection Manager using the interface described in Section 8.3. There are two types of Operations: Router Operations and Port Operations. <i>Note: When not capitalized, "operation" has its ordinary meaning.</i>
Passive Cable	A cable that does not incorporate any electronics to condition the data path signals.
Path	The one-way path that carries data either from a Source Adapter to a Destination Adapter or between a Connection Manager and a Control Adapter. A Path traverses one or more Routers, which route traffic along the Path as configured by the Connection Manager.
Path 0	The Path that corresponds to HopID 0. Path 0 is used exclusively for Control Packets.
Path Configuration Space	The Configuration Space for a Path. Each Path has its own Path Configuration registers.
PCB	Printed Circuit Board.
PCIe	PCI Express.
PCIe Host Interface	A Host Interface that is run over a PCIe bus.
PCIe Host Router	A Host Router that implements a PCIe Host Interface.
PCIe Path	A Path that tunnels PCIe traffic.
PLL	Phase Locked Loop.
Platform Integrated Host Router	Host Router silicon that is integrated into the platform, either as part of the platform SoC or as a discrete chip on the motherboard.
Port	See USB4 Port.
Port Operation	A type of Operation that targets individual USB4 Port functionality (e.g. compliance tests and receiver Lane margining tests).
PRBS	Pseudo-Random Bit Sequence.
PRTS	Pseudo-Random Trit Sequence.

Term/Abbreviation	Description
Protocol Adapter	The Adapter that interfaces to a protocol-specific entity. A Protocol Adapter implements a Protocol Adapter Layer and a Transport Layer.
Protocol Adapter Layer	The protocol stack layer above the Transport Layer. The Protocol Adapter Layer encapsulates Tunneled Protocol traffic into Tunneled Packets and hands them off to the Transport Layer. It also receives packets from the Transport Layer and extracts the Tunneled Protocol traffic.
Quality of Service (QoS)	About or relating to the specific bandwidth and latency requirements for a particular protocol or use case.
Receiver	The receiver in a Lane Adapter.
Re-timer Index	A one-based index number that uniquely identifies a Re-timer on a Link between two Routers. The Re-timer Index corresponds to the distance between a Re-timer and a Router where Re-timer index = (number of Re-timers between the Router and Re-timer) + 1. A Re-timer has two Re-timer Indexes – one for each Router on the Link. See Figure 4-3.
Route String	A string that represents the route between the Host Router and another Router.
Router	A component that manages and routes traffic through a USB4 Fabric and ensures time synchronization within the USB4 Fabric.
Router Assembly	A Router and any Re-timers between the USB4 Ports of the Router and their USB Type-C connectors.
Router Configuration Space	The Configuration Space for a Router. Each Router has a Router Configuration Space.
Router Operation	A type of Operation that targets Router-wide functionality (e.g. NVM update and reading Router capabilities).
RT Transaction	A type of Transaction that is used by a Router to communicate with a Re-timer. A Re-timer also uses RT Transactions to communicate with another Re-timer or Router.
Scrambling	The process of changing a bit stream in a pseudo-random way. See also De-Scrambling.
Sideband (SB) Channel	The connection between the USB4 Ports of two interconnected Routers that provides initial communication and Link setup functionality.
Sideband (SB) Registers	A set of registers that are used for Link setup and configuration over the Sideband Channel. A Router uses Transactions to read from and write to the Sideband Registers.
Single-Lane Link	A Link that uses only one Lane to transmit and receive data.
Skew	The presence of misalignment between Symbols across the receivers of a Link with multiple receivers.
SLOS	Symbol Lock Ordered Set. Includes SLOS1 and SLOS2.
Source Adapter	A Protocol Adapter that is the source of Tunneled Packets routed through the USB4 Fabric. Note that a Protocol Adapter may be a Source Adapter on one Path and a Destination Adapter on another.
Spanning Tree	A loop-free Tree Topology used by a Connection Manager to manage a Domain.
Spread Spectrum Clock (SSC)	A method of varying the frequency of the clock over time to reduce EMI.
Standalone AIC Host Router	A Host Router that is added to the platform as an Add-In Card (AIC).
Symbol Time	The time it takes to transmit a 66b Symbol at Gen 2 speed, a 132b Symbol at Gen 3 speed, or a 7t Symbol at Gen 4 speed.
Symmetric Link	An Aggregated Link that operates with 2 Transmitters and 2 Receivers on each side of the Link. The Gen 2 or Gen 3 “Dual-Lane Link” in Version 1.0 of this specification is an example of a Symmetric Link.
TBT3	Thunderbolt™ 3.
TBT3-Compatible	Able to interoperate with TBT3 products.
TBT3-Compatible Active Cable	A USB4 Active Cable that can interoperate with TBT3 and TBT3-Compatible Routers, Re-timers, and Connection Managers.

Term/Abbreviation	Description
TBT3-Compatible Connection Manager	A USB4 Connection Manager that can interoperate with TBT3 and TBT3-Compatible Routers, Re-timers, and Cables.
TBT3-Compatible Router	A Router that implements Chapter 13 of this specification.
Time Management Unit (TMU)	The functional block in each Router that is used to distribute and synchronize time throughout the USB4 Fabric.
TopologyID	A unique topological address representing the position of a Router within a Domain.
Transaction	The unit of communication across the Sideband Channel. A Transaction consists of a set of defined symbols. There are four types of Transactions: LT Transactions, ELT Transactions, AT Transactions, and RT Transactions.
Transport Layer	The protocol stack layer that is responsible for routing traffic through the USB4 Fabric and ensuring flow control and data integrity.
Transport Layer Packet (Packet)	A type of packet that either originates from or is routed by the Transport Layer.
Transmitter	Refers to a USB4 Transmitter.
Tree Topology	The type of network topology in which a central 'root' node (the top level of the hierarchy) is connected to one or more other nodes that are one level lower in the hierarchy with a point-to-point link. There may be more levels of hierarchy but each is connected to the level above via a point-to-point link.
Tunneled Packet	A type of Transport Layer Packet that is used to carry Tunneled Protocol traffic through a USB4 Fabric.
Tunneled Protocol	An I/O protocol tunneled through a USB4 Fabric.
TXFFE	Transmitter Feed Forward Equalization.
Unit Interval (UI)	Given a data stream of a repeating pattern of alternating 1 and 0 values, the Unit Interval is the value measured by averaging the time between voltage transitions, over a time interval long enough to make all intentional frequency modulation of the source clock negligible.
Upstream	The direction of data flow towards the Connection Manager.
Upstream Adapter	The Adapter that a Connection Manager uses to address a Router.
Upstream Facing Port (UFP)	The USB4 Port that faces the Connection Manager in the Spanning Tree topology of the Domain.
USB	Universal Serial Bus.
USB3	USB 3.2 Specification.
USB3 Gen T	A type of USB3 Tunneling architecture where the Enhanced SuperSpeed protocol is extended to allow operation at the maximum bandwidth available on the USB4 Link.
USB3 Gen T Path	A Path that tunnels USB3 traffic between two USB3 Gen T Adapters.
USB3 Gen T Port	A port on an Internal USB3 Gen T Component that supports USB3 Gen T operation.
USB3 Gen X	A type of USB3 Tunneling architecture that uses the existing USB 3.2 Enhanced SuperSpeed protocol.
USB3 Gen X Path	A Path that tunnels USB3 traffic between two USB3 Gen X Adapters.
USB3 Gen X Port	A port on an Internal USB3 Component that supports USB3 Gen X operation.
USB3 Path	A Path that tunnels USB3 traffic. Refers to both a USB3 Gen T Path and a USB3 Gen X Path.
USB4-Based Dock	A USB4-based dock product combines a USB4 Hub (including at least one exposed USB Type-C downstream port) with additional capabilities that either exposes other connector types and/or includes other user-visible functions, e.g. storage, networking, etc. Example of functions that are not considered user-visible include firmware update or device authentication.
USB4 Fabric	One or more interconnected Domains.

Term/Abbreviation	Description
USB4 Link	The logical connection between the USB4 Ports of two interconnected Routers. A USB4 Link may include either one or two Lanes. Unless otherwise noted, the term “Link” without any preceding descriptor refers to a USB4 Link.
USB4 Port	A Router interface consisting of two Lane Adapters and a Sideband Channel. Protocol Adapters and Control Adapters are never part of a USB4 Port.
Ver. 1 Connection Manager	A Connection Manager that predates Version 2.0 of the USB4 Specification.
Ver. 2 Connection Manager	A Connection Manager that supports Version 2.0 of the USB4 Specification.
Ver. 1 Router	A Router that implements Version 1.0 of the USB4 Specification.
Ver. 2 Router	A Router that implements Version 2.0 of the USB4 Specification.
Word	2 bytes.

2 Architectural Overview

This chapter presents an overview of Universal Serial Bus 4 (USB4®) architecture and key concepts. USB4 is similar to earlier versions of USB in that it is a cable bus supporting data exchange between a host computer and a wide range of simultaneously accessible peripherals. However, USB4 also allows a host computer to setup data exchange between compatible peripherals. The attached peripherals share bandwidth as configured by the host computer. The bus allows peripherals to be attached, configured, used, and detached while the host and other peripherals are in operation.

When configured over a USB Type-C® connector interface, USB4 functionally replaces USB 3.2 while retaining USB 2.0 bus operating in parallel. Enhanced SuperSpeed USB, as defined in the USB 3.2 Specification, remains the fundamental architecture for USB data transfer on a USB4 Fabric. The difference with USB4 versus USB 3.2 is that USB4 is a connection-oriented, tunneling architecture designed to combine multiple protocols onto a single physical interface, so that the total speed and performance of the USB4 Fabric can be dynamically shared. USB4 allows for USB data transfers to operate in parallel with other independent protocols specific to display, load/store and host-to-host interfaces. Additionally, USB4 extends performance beyond the 20 Gbps (Gen 2 x 2) of USB 3.2 to 80 Gbps (Gen 4 x 2) over the same dual-lane, dual-simplex architecture.

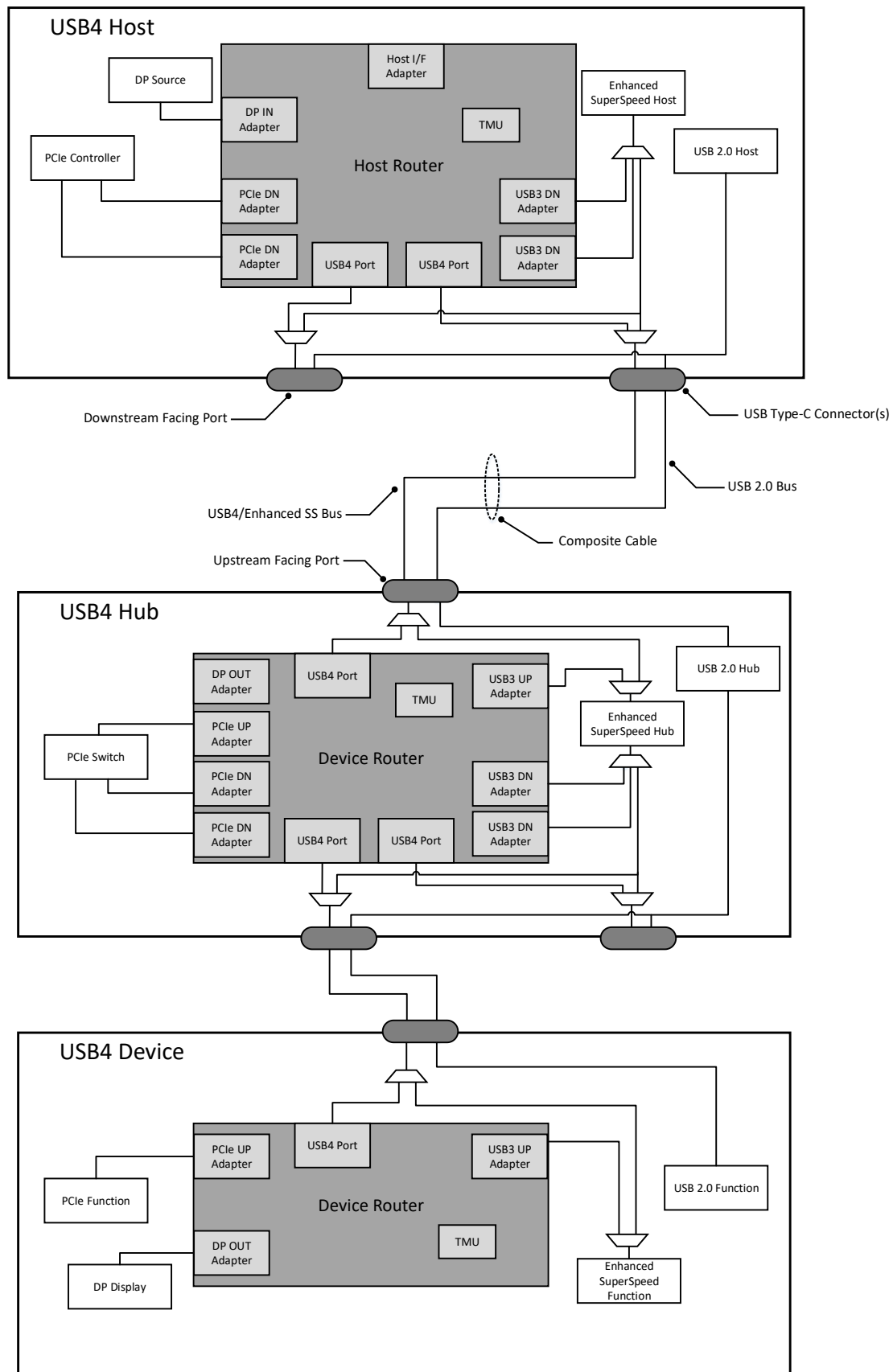
This specification introduces the concept of protocol tunneling to USB bus architecture. Besides tunneling Enhanced SuperSpeed USB (USB3), display tunneling based on DisplayPort (DP) protocol and load/store tunneling based on PCI Express (PCIe) are defined. These protocol tunnels operate independently over the USB4 transport and physical layers. Additionally, USB4 allocates packets for bus configuration and management, and packets can be allocated specifically for host-to-host data connections.

2.1 USB4 System Description

Figure 2-1 illustrates the dual bus architecture of USB 3.2 as augmented by USB4. As architected, backward compatibility is supported with minimum interoperability starting at USB 2.0, working up through USB 3.2, and finally up to USB4 based on the highest common bus level supported across the interconnected components.

Protocol tunnels are interfaced via Protocol Adapters specific to each protocol. For USB 3 Gen X and PCIe protocols, native USB hubs and PCIe switches are required to handle protocol-related packet routing and buffering. For display tunneling, Host-to-Host communication, and USB3 Gen T tunneling, no intermediate protocol-specific logic is required with tunnels being established as an end-to-end link.

Time synchronization across a USB4 Fabric uses distributed time management units (TMUs) associated with each Router.

Figure 2-1. USB4/USB3.2 Dual Bus System Architecture

2.1.1 Architectural Constructs

The following summarizes basic constructs in the USB4 architecture.

2.1.1.1 Routers

The Router is a fundamental building block of the USB4 architecture. A Router maps Tunneled Protocol traffic to USB4 packets and routes packets through the USB4 Fabric. A Router also distributes and synchronizes time throughout the USB4 Fabric via its Time Management Unit (TMU).

A Router is discovered and configured by a Connection Manager located within the USB4 Host. The concept of a Router is not to be confused with a USB4 Hub. The Router includes a flat point-to-point, configurable switch necessary to create the internal paths between Adapters. One Router typically exists within each instance of a USB4 Host, USB4 Hub or USB4 Device.

There are two types of Routers: Host Routers and Device Routers.

2.1.1.2 Adapters

Each Router contains up to 64 Adapters. Adapters provide an interface between a Router and an external entity. There are three types of Adapters: Protocol Adapters, Lane Adapters, and Control Adapters.

2.1.1.2.1 Protocol Adapter

A Protocol Adapter is used to translate between a supported native protocol and a USB4 tunnel. There are four types of Protocol Adapters: USB3 Adapters, DisplayPort (DP) Adapters, PCIe Adapters, and Host Interface (HI) Adapters.

2.1.1.2.2 Lane Adapter

A Lane Adapter provides an interface for a Lane. A USB4 Port has one Lane Adapter per Lane.

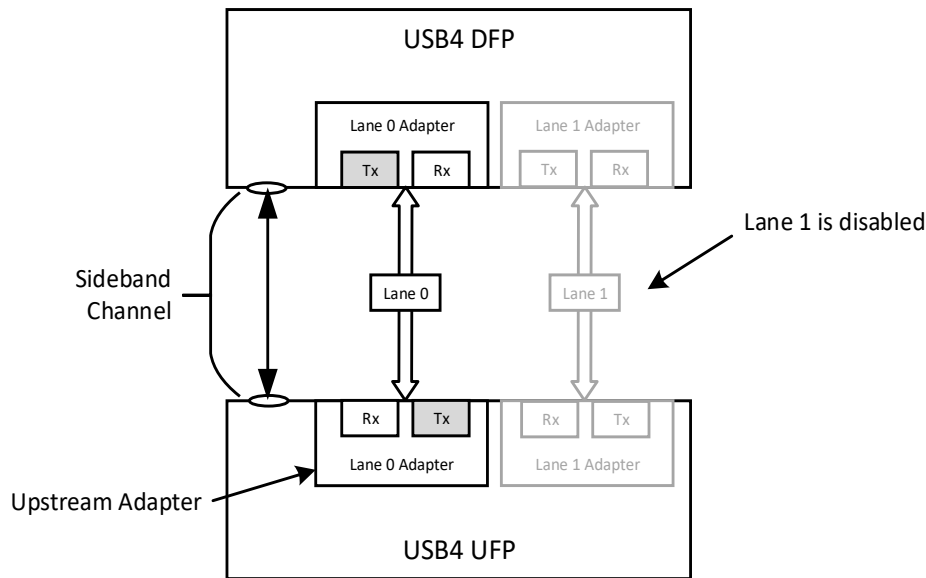
2.1.1.2.3 Control Adapter

A Router contains one Control Adapter. The Control Adapter is a logical Adapter and does not have a physical layer. The Control Adapter is the final consumer of Control Packets that are targeted to the Router. The Control Adapter also generates Control Packets, which are sent to the Connection Manager.

2.1.1.3 USB4 Ports and Links

A USB4 Port is the entity that provides the USB4 functional interface that resides on each end of a USB4 Link. It consists of the transmit and receive Lanes of the USB4 data bus along with a two-wire Sideband (SB) Channel (SBTX/SBRX).

A Link can be either a Single-Lane or an Aggregated Link. When operating as a Single-Lane Link, Lane 1 of the USB4 Port is disabled. When operating as an Aggregated Link, Lanes 0 and 1 are both enabled and are logically bonded together to provide a single data channel. Figure 2-2 shows a Single-Lane Link. Note that only a Gen 2 or Gen 3 Link can be a Single-Lane Link. An Aggregated Link can operate at any speed.

Figure 2-2. Single-Lane USB4 Link

An Aggregated Link can be symmetric or asymmetric. When a Link is symmetric, the USB4 Ports on either end of the Link operate with the same number of transmitters and the same number of receivers. When a Link is asymmetric, the USB4 Port on one side of the Link operates with three transmitters and one receiver while the USB4 Port on the opposite side of the Link operates with three receivers and one transmitter. Gen 2 and Gen 3 Links are always symmetric, while a Gen 4 Link can be either symmetric or asymmetric. Figure 2-3 shows a Symmetric Link.

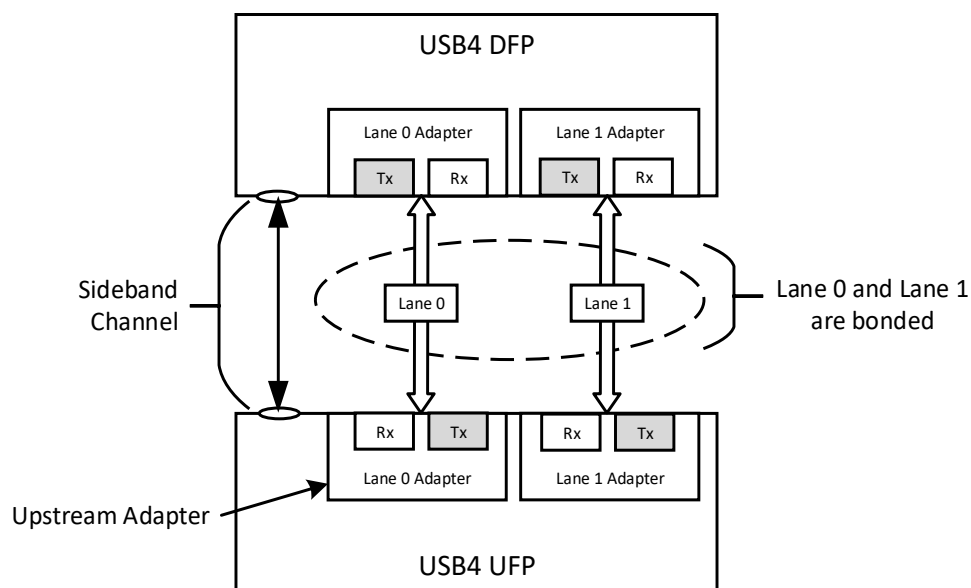
Figure 2-3. Symmetric USB4 Link

Figure 2-4 shows an Asymmetric Link. Note that either the Upstream Facing Port or the Downstream Facing Port can be configured with three transmitters or three receivers.

Figure 2-4. Asymmetric USB4 Link

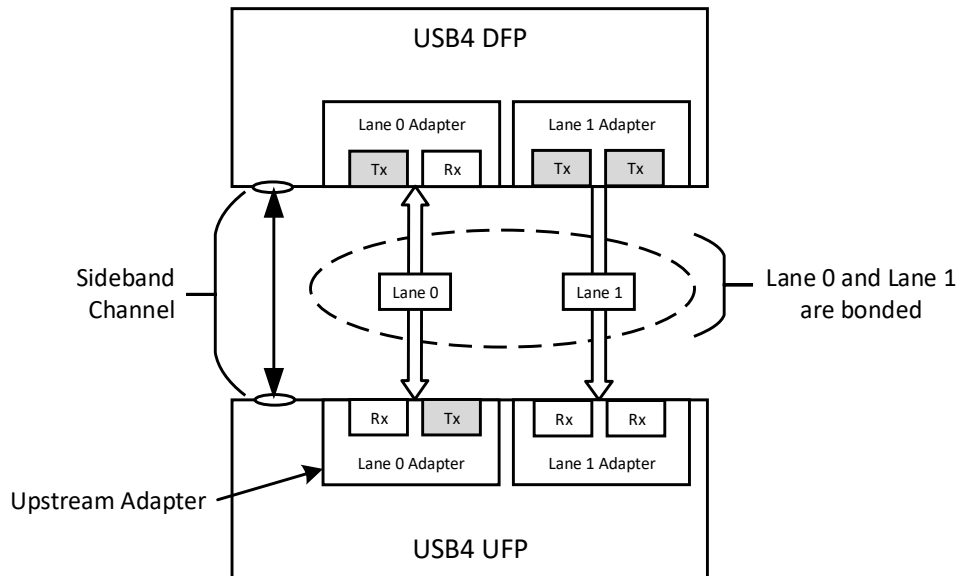
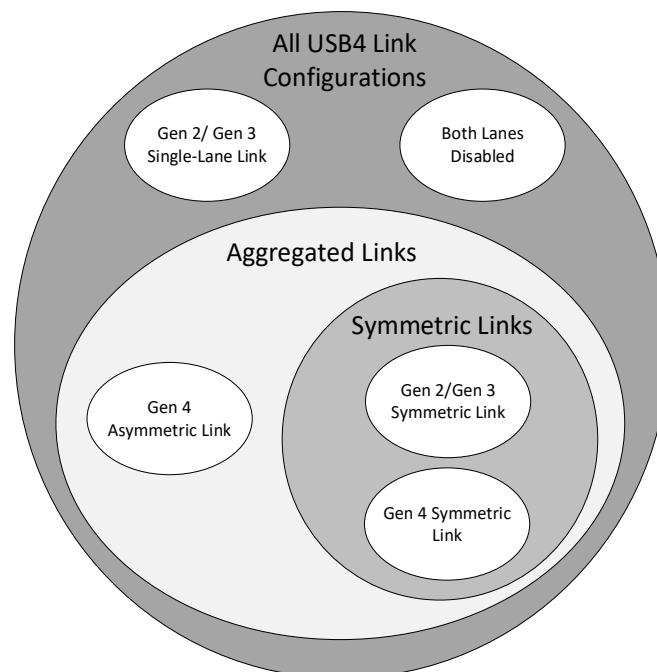


Figure 2-5 shows the different types of USB4 Links and how they are related to one another.

Figure 2-5. USB4 Link Types



The primary communication channel of the USB4 Fabric is over the USB4 Link that interconnects two USB4 Ports. The USB4 Link transports packets for both Tunneled Protocol traffic and bus management traffic between Routers. The Sideband Channel of a USB4 Port is used to initialize and manage the USB4 Link between the USB4 Ports.

For a USB4-enabled USB Type-C port, the complete interface includes a USB4 Port, a USB 2.0 data bus, and the USB Type-C Configuration Channel (CC) along with power/ground (VBUS, VCONN and GND).

2.1.1.4 USB4 Devices

2.1.1.4.1 USB4 Peripheral Device

A USB4 Peripheral Device has a single USB4 Upstream Facing Port. It does not have any USB4 Downstream Facing Ports.

A USB4 Peripheral Device contains a Device Router and can also optionally contain one or more of the following:

- An Enhanced SuperSpeed Function.
- A USB 2.0 Function.
- A PCIe Function.
- A DisplayPort Source or Sink.

A USB4 Peripheral Device supports 20G USB4 operation (Gen 2). It optionally supports 40G USB4 operation (Gen 3) and 80G USB4 operation (Gen 4).

2.1.1.4.2 USB4 Hub

At a high level, a USB4 Hub is functionally similar to a USB 3.2 hub – it consists of one USB4 Upstream Facing Port and one or more USB4 Downstream Facing Ports. USB4 Hub functionally operates as a tree-like structure for enabling one or more Downstream Facing Ports to be served by one Upstream Facing Port, typically for the purpose of port expansion.

In addition to the USB4-specific hub functionality, USB 3.2 and USB 2.0 hub functionality is supported such that the Downstream Facing Ports of a USB4 Hub can support backward-compatibility with USB 3.2 and USB 2.0 devices.

A USB4 Hub contains:

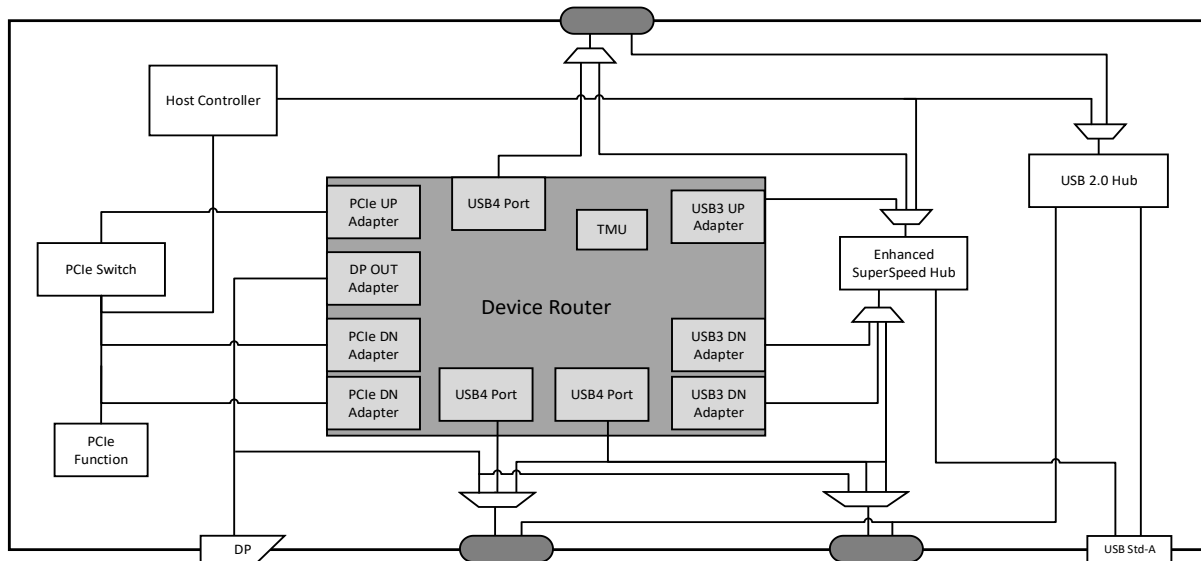
- A Device Router.
- An Enhanced SuperSpeed USB Hub.
- A PCIe Switch.
- A USB 2.0 Hub.

A USB4 Hub supports 20G USB4 operation (Gen 2) and 40G USB4 operation (Gen 3). It may also optionally support 80G USB4 operation (Gen 4).

A USB4 Hub is required to support DisplayPort Alt Mode on all of its Downstream Facing Ports. See the USB Type-C Specification for a full definition of the requirements and details regarding DisplayPort Alt Mode support on a Downstream Facing Port.

2.1.1.4.3 USB4-Based Dock

Figure 2-6 illustrates a USB4-Based Dock with two USB4 Downstream Facing Ports and peripheral device functions for each of the available protocols.

Figure 2-6. Example of a USB4-Based Dock

The requirements for a USB4 Hub apply to a USB4-Based Dock.

2.1.1.5 USB4 Host

A USB4 Host contains:

- A Host Router.
- A USB 2.0 Host.
- An Enhanced SuperSpeed Host.
- A DisplayPort Source.

A USB4 Host can also optionally contain a PCIe controller or PCIe switch.

A USB4 Host supports 20G USB4 operation (Gen 2). It optionally supports 40G USB4 operation (Gen 3) and 80G USB4 operation (Gen 4).

A USB4 Host is required to support DisplayPort Alt Mode on all of its Downstream Facing Ports. See the USB Type-C Specification for a full definition of the requirements and details regarding DisplayPort Alt Mode support on a Downstream Facing Port.

2.1.1.6 Re-timers

A USB4 product can contain up to two On-Board Re-timers per USB4 Port. USB4 Re-timers are described in the USB4 Re-Timer Specification.

2.1.1.7 Connection Manager

The Connection Manager is the software entity that is responsible for enumerating, configuring, and managing a Domain. The Connection Manager performs tasks such as Path setup/teardown, Hot plug/unplug, and bandwidth management. The Connection Manager is part of the USB4 Host system.

2.1.2 USB4 Mechanical

The electro-mechanical specifications for USB cables and connector assemblies that support USB4 are documented by the USB Type-C Specification.

USB4 Hubs and USB4 Peripheral Devices have an upstream connection. USB4 Hosts and USB4 Hubs have one or more downstream connections. For USB Type-C connectors, upstream and downstream behaviors are established using the configuration features of the USB Type-C functional architecture.

2.1.3 USB4 Power

Power for USB4 operation is established and managed as defined in the USB Type-C Specification and the USB PD Specification. Unlike USB 2.0 and USB 3.2, USB4 does not define its own VBUS-based power model.

2.1.4 USB4 System Configuration

USB4 connections between hosts, hubs and devices are established and managed as defined in the USB Type-C Specification. Once a USB4 connection is established, the USB4 Host configures and manages USB4 operation using a software-based Connection Manager.

2.1.5 Thunderbolt™ 3 (TBT3) Compatibility Support

A USB4 Host or USB4 Peripheral Device can optionally support interoperability with Thunderbolt 3 (TBT3) products.

A USB4 Hub is required to support interoperability with Thunderbolt 3 products on all of its Downstream Facing Ports. A USB4 Hub may optionally support TBT3-Compatibility on its Upstream Facing Port.

When interoperating with a TBT3 product, Thunderbolt Alt Mode is established on the link between products. The USB Type-C Specification describes how a USB4 product negotiates and enters Thunderbolt Alt Mode.

Chapter 13 describes the additional requirements for a Router that supports TBT3-compatible interoperability.

2.1.6 USB Type-C Alternate Mode Compatibility Support

A USB4 product can optionally support interoperability with USB Type-C Alternate Modes as defined by the USB Type-C Specification.

2.2 USB4 Fabric Architecture

The USB4 Fabric is designed to meet the needs of multiple transport protocols. Its main features are:

- Signaling rates that support high throughput interconnects:
 - 10 Gbps (for Gen 2), 20 Gbps (for Gen 3), and 40 Gbps (for Gen 4).
 - Optional support for Thunderbolt 3-compatible rates of 10.3125 Gbps (for Gen 2) and 20.625 Gbps (for Gen 3).
- Hop-by-hop, credit-based flow control.
- Bandwidth management and prioritization.
- A programming model that allows a Connection Manager to initialize and manage a USB4 Domain in a manner that is transparent to the Tunneled Protocols and their software.
- A time synchronization protocol to synchronize real-time clocks across one or more USB4 Domains.
- Error detection, correction, and recovery.
- Link-level Power Management.

2.2.1 USB4 Functional Stack

Figure 2-7 shows the USB4 functional stack layers.

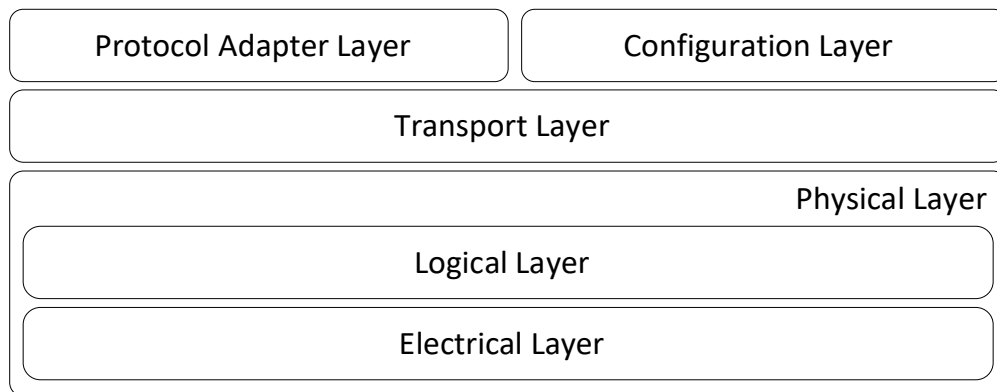
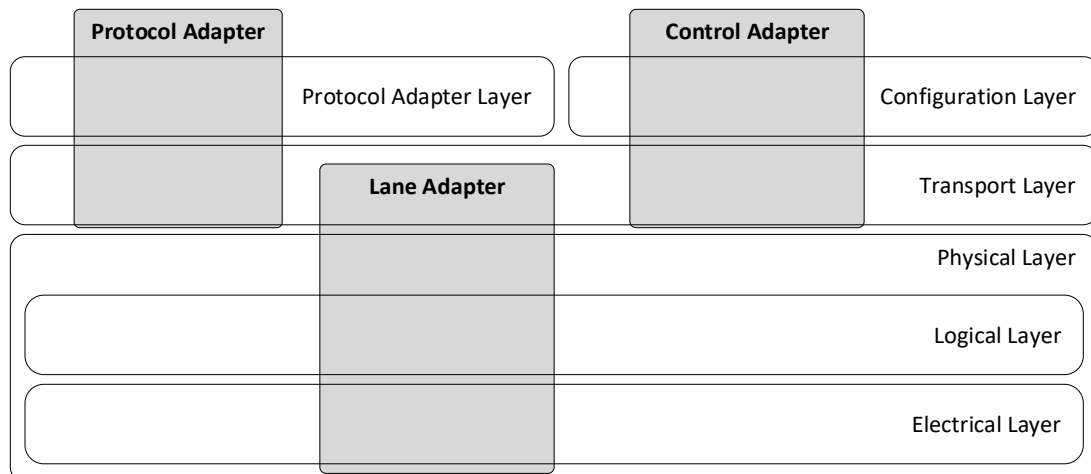
Figure 2-7. USB4 Functional Stack Layers

Figure 2-8 identifies which layers are implemented by USB4 Ports (Lane Adapter), Protocol Adapters and the Control Adapter.

Figure 2-8. USB4 Port (Lane Adapter), Protocol Adapter, and Control Adapter across Functional Layers

2.2.1.1 Electrical Layer

The Electrical Layer defines electrical signaling characteristics of a USB4 Link including scrambling, encoding, jitter, and voltage.

2.2.1.2 Logical Layer

The Logical Layer establishes a USB4 Link between two Routers and provides services to transmit and receive streams of bytes between them.

The Logical Layer resides on top of the Electrical Layer and below the Transport Layer. It treats the traffic to and from the Transport Layer as a byte stream.

The services provided by the Logical Layer are:

- Establishment and maintenance of a USB4 Link with a Link Partner.
- Performance scalability via different speeds and widths.
- Error detection and recovery mechanisms.
- Operation with different media such as passive cable, active cable, and Re-timers.

- Support for mechanisms such as clocking compensation, data scrambling, and Forward-error-correcting codes.
- Power management.

A USB4 Link is assisted and managed by a companion Sideband Channel that:

- Configures parameters of the USB4 Link.
- Interacts with Re-timers (if present) and performs USB4 Link TxFFE handshake.
- Ensures a correct power down/wake up sequence of the USB4 Link transceivers and Re-timers.

2.2.1.3 Transport Layer

The Transport Layer forwards Tunneled Packets and Control Packets through the bus. It defines packet format, routing, Quality-of-Service (QoS) support, flow control, and time synchronization. The Transport Layer is where protocol MUXing is performed.

2.2.1.4 Configuration Layer

The Configuration Layer performs Router configuration tasks and handles incoming Control Packets. The Configuration Layer provides an addressing scheme for Control Packets within the Domain, processes Control Packets, and delivers a reliable transport mechanism for Control Packets.

Control Packets provide the Connection Manager with access to the Configuration Spaces of a Router.

2.2.1.5 Protocol Adapter Layer

The Protocol Adapter Layer performs mapping between Tunneled Protocol traffic and USB4 Transport Layer Packets. A Protocol Adapter Layer is defined by the type of Tunneled Protocol traffic it sends and receives. See Section 2.2.10 for more details of the different types of Protocol Adapter Layers.

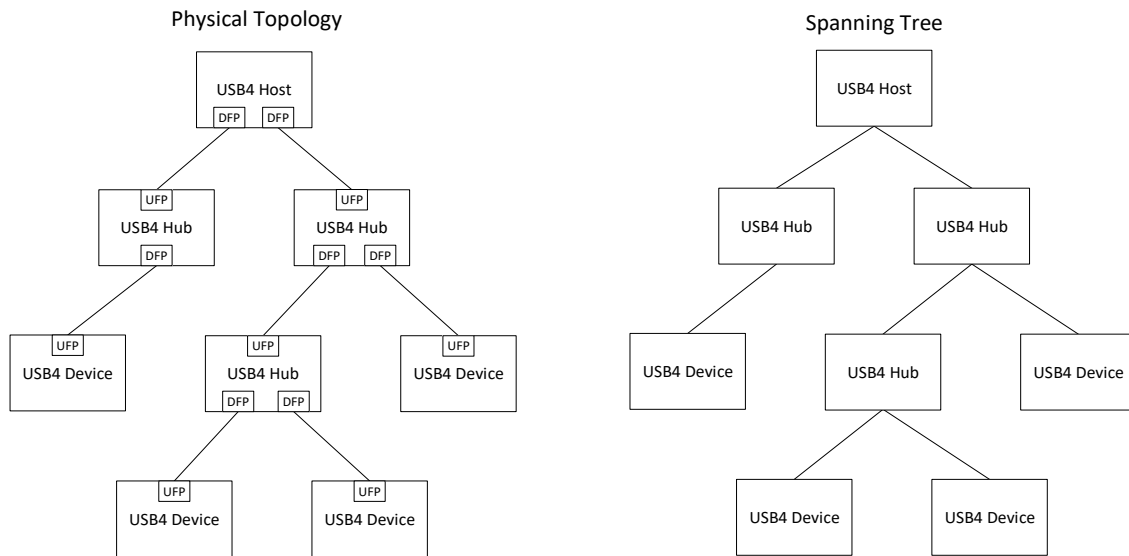
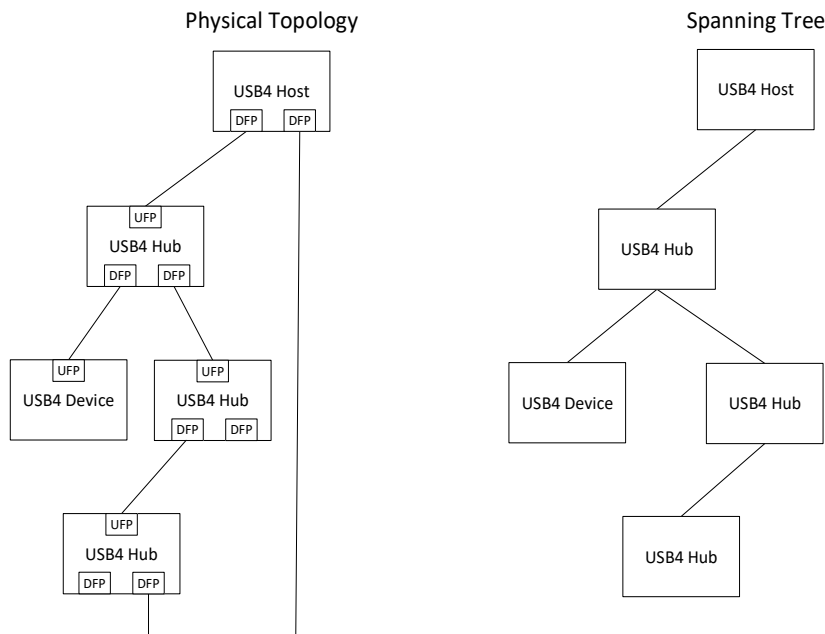
2.2.2 USB4 Fabric Topology

The physical topology of a USB4 Fabric is an interconnected graph. The physical topology will typically resemble a tree with a USB4 Host at the root and a set of USB4 Hubs and/or USB4 Peripheral Devices connected downstream, in series and/or in parallel. However, loops can occur if there are multiple connections to a USB4 Host. If the Connection Manager detects a loop in the physical topology of its Domain, it uses a subset of the interconnected graph in the form of a Spanning Tree, which removes any loops. If there are no loops in the physical topology, the Spanning Tree is the same as the physical tree. See the Connection Manager Guide for more information on how a Connection Manager detects and handles loops.

The Host Router is at the top of the Spanning Tree. The Spanning tree can have up to six levels, meaning that a Device Router can be up to 5 hops away from the Host Router along the Spanning Tree.

The Connection Manager accesses a Domain through the Host Router. Control Packets are only routed along Links that belong to the Spanning Tree. Tunneled Protocol traffic is not limited to the Spanning Tree.

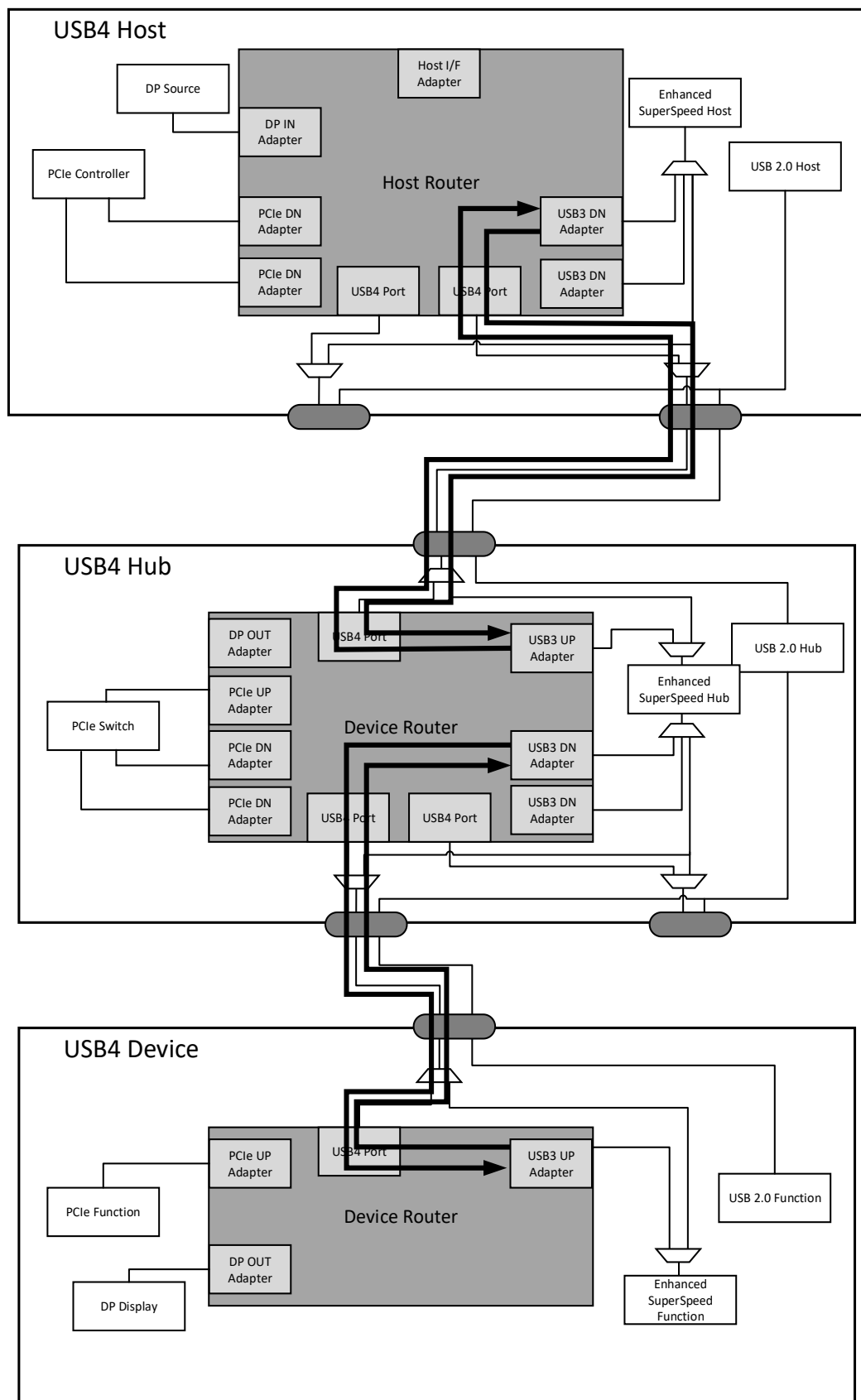
Figure 2-9 shows an example of a Spanning Tree for a USB4 Fabric with no loops in its physical topology. Figure 2-10 shows an example of a Spanning Tree for a USB4 Fabric with a loop in its physical topology.

Figure 2-9. Example USB4 Physical Topology (No Loop) and Spanning Tree**Figure 2-10. Example USB4 Physical Topology (with Loop) and Spanning Tree**

2.2.3 Paths

A Path represents a directional logical connection over the USB4 Fabric. A Path is defined either between two Protocol Adapters or between the Connection Manager and a Control Adapter.

A Path can be end-to-end (as is the case for USB3 Gen T, Display and Host-to-Host Tunneling) or it can traverse a single USB4 Link (as is the case for USB3 Gen X tunneling and PCIe Tunneling). Figure 2-11 shows an example of a set of Paths that tunnel USB3 Gen X traffic between a USB4 Host and a USB4 Device.

Figure 2-11. Paths Across a USB4 Fabric

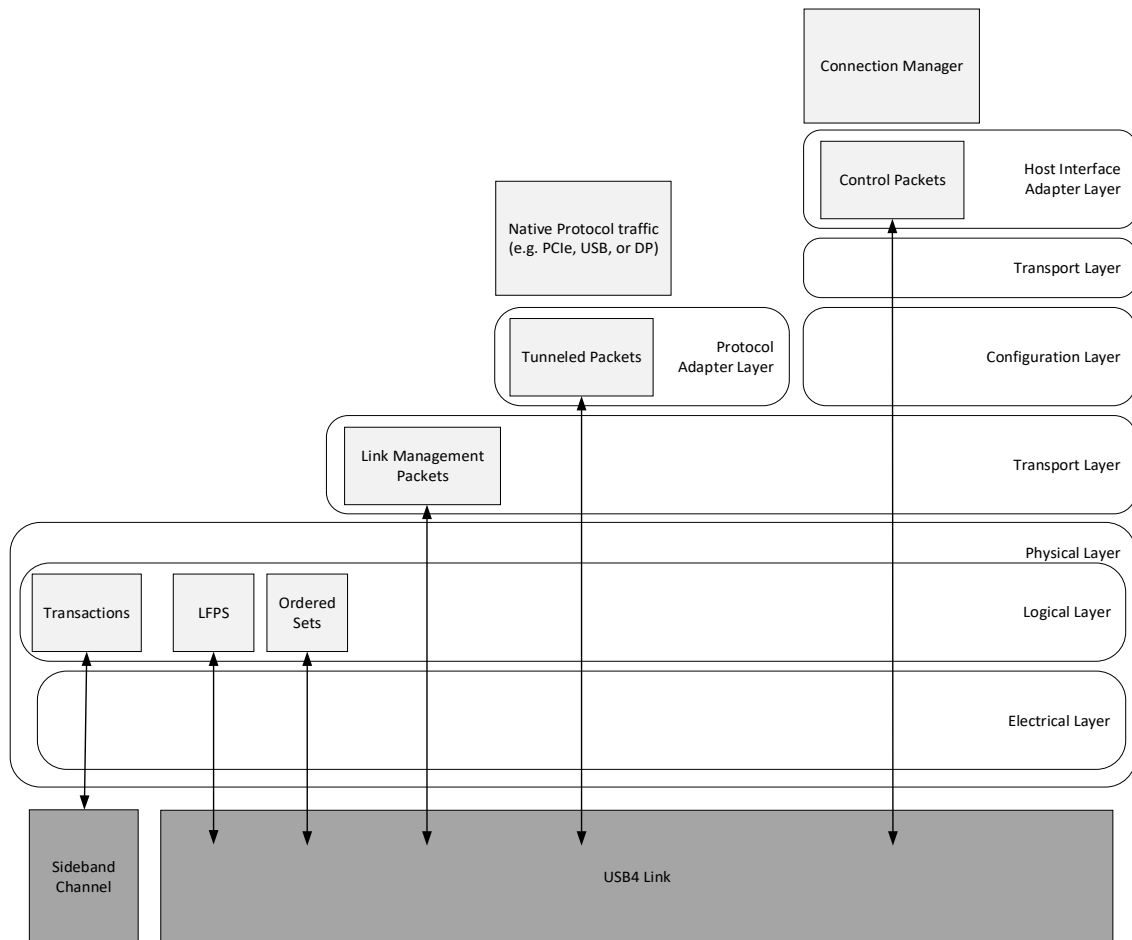
A Tunnel is configured end-to-end before data transfer can take place.

Each packet carries an identifier (called a HopID) that identifies the Path in the context of a given Link. The HopID is configured by a Connection Manager and can vary across each Link in the Path. When a Router receives a packet, it uses the HopID to determine the packet's next HopID and which Egress Adapter to forward the packet to.

2.2.4 Communication Constructs

Figure 2-12 shows the various constructs that are used for communication over the USB4 Fabric.

Figure 2-12. USB4 Communication by Functional Layer



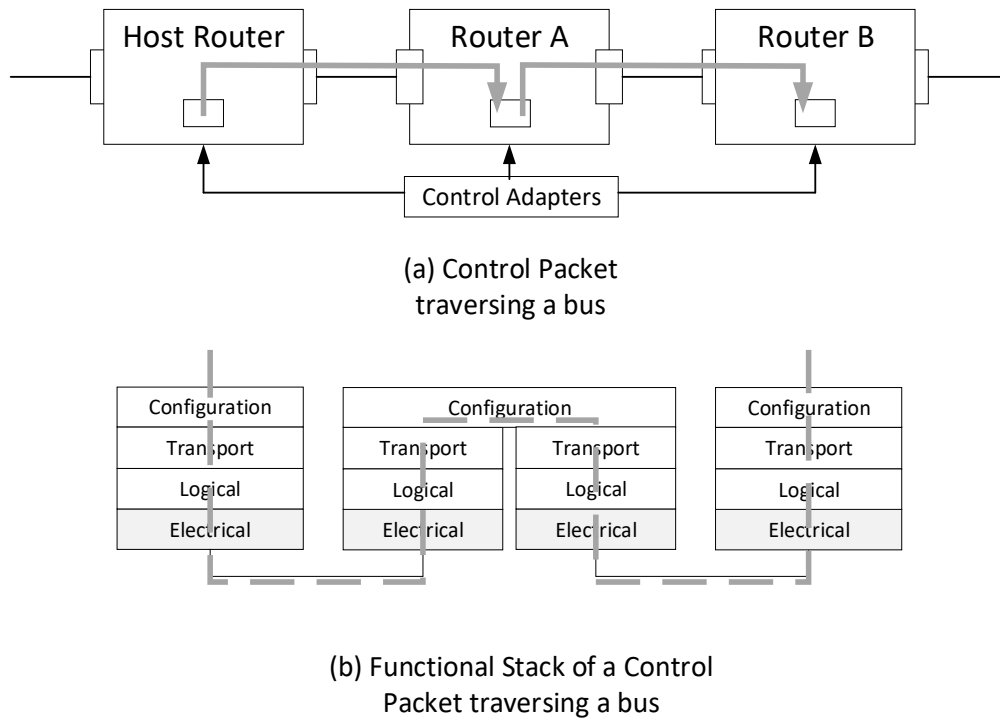
2.2.4.1 USB4 Link

The USB4 Link uses the packets and Ordered Sets described in this section.

2.2.4.1.1 Control Packets

Control Packets are used by a Connection Manager to configure and manage the Routers across the bus. They are also used by a Router to communicate with a Connection Manager. Control Packets are routed over the bus based on a Route String that identifies a Router's position in the Spanning Tree. When a Control Packet originates from the Connection Manager, the Route String identifies the Router that the packet is targeted to. When a Control Packet originates from a Router, the Router String identifies the Router that sent the packet.

Figure 2-13 shows an example of a Control Packet that traverses several Routers. The Control Adapter in a non-target Router forwards the packet to a USB4 Port. The Control Adapter of the target Router consumes the Control Packet.

Figure 2-13. Example Control Packet Traversing Several Routers**2.2.4.1.2 Tunneled Packets**

Tunneled Protocol traffic is encapsulated and tunneled over the USB4 Fabric in Tunneled Packets. Tunneled Packets traverse the USB4 Fabric along one or more Paths.

2.2.4.1.3 Link Management Packets

Link Management Packets are confined to a single USB4 Link. Link Management Packets originate in the Transport Layer of the Router at one end of the Link and terminate in the Transport Layer of the Router at the other end of the Link.

The following Link Management Packets are defined:

- Time Sync Packets – Used to synchronize the clocks of the Routers on the bus.
- Flow Control Packets – Used to prevent buffer overflow.
- Idle Packets – Ensure a steady byte stream is fed to the Logical Layer when no other Transport Layer Packets are being transmitted.

2.2.4.1.4 Ordered Sets

The Logical Layer uses Ordered Sets for tasks such as Symbol synchronization, Link training, and de-skew between Lanes. An Ordered Set is composed of a number of Symbols that are specific to the task being performed.

2.2.4.2 Sideband Channel

The Sideband Channel handles the following events:

- Lane Initialization.
- Connection or disconnect on a USB4 Port.
- Lane disable or enable.
- Entry or exit from sleep state.

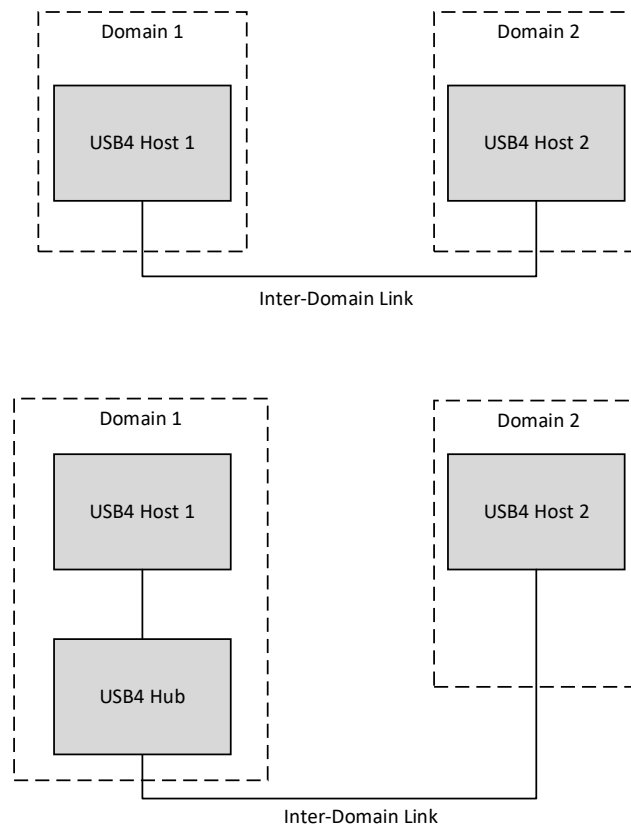
The Sideband Channel is a packet-based channel. Sideband Channel packets are called Transactions to distinguish them from USB4 Link packets.

Each USB4 Port implements a set of Link configuration registers called Sideband (SB) Register Space. Routers use Transactions to access the SB Register Space of another Router or Re-timer.

2.2.5 USB4 Host-to-Host Communications

Multiple Domains can be connected over a USB4 Fabric under certain conditions. Figure 2-14 illustrates two possible Inter-Domain connections. An Inter-Domain Link connects two Routers that reside in different Domains.

Figure 2-14. Example USB4 Host-to-Host Connections



The Connection Managers in two connected Domains communicate with each other using Host Interface Tunneled Packets. The most common use of Host-to-Host Tunneling is to allow two Connection Managers to exchange information through their respective Host Interfaces. For example, two USB4 Hosts can exchange IP (Internet Protocol) packets over USB4 using Host-to-Host Tunneling.

2.2.6 Programming Model

2.2.6.1 Connection Manager

A Connection Manager is the entity responsible for managing and configuring a Domain. The Connection Manager communicates with Routers in a Domain using Control Packets.

The Connection Manager executes the following configuration tasks within a Domain:

- Router initialization.
- Scanning and setting Adapter configurations.
- Setting and removing Paths.

- Configuration of QoS behavior in the USB4 Fabric including flow control and bandwidth allocation.
- Management across Domains.

2.2.6.2 Configuration Spaces

Routers are configured via configuration registers that reside in one of four Configuration Spaces:

- Router Configuration Space – Contains the Router-level configuration parameters. Each Router has a Router Configuration Space.
- Adapter Configuration Space – Contains capabilities, configuration, and error statistics for an Adapter. Protocol Adapters and Lane Adapters have an Adapter Configuration Space. Control Adapters do not have an Adapter Configuration Space.
- Path Configuration Space – Contains information used for Path setup. Protocol Adapters and Lane Adapters have a Path Configuration Space. Control Adapters do not have a Path Configuration Space. A Path Configuration Space includes an entry for each supported Path.
- Counters Configuration Space – Contains performance statistics for a set of selected Paths. Counters Configuration Space is optional. Protocol Adapters and Lane Adapters can optionally have a Counters Configuration Space. Control Adapters do not have a Counters Configuration Space.

2.2.6.3 Operations

A Router supports an interface, which allows a Connection Manager to initiate various Operations. There are two types of Operations: Router Operations and Port Operations.

Router Operations initiate Router-wide tasks such as NVM read/write and DisplayPort resource management. Router Operations are initiated by writing to Router Configuration Space.

Port Operations can be used to do the following:

- Initiate a read or write to the SB Register Space of a Router, Link Partner, or a Re-timer in the Link between a Router and its Link Partner.
- Initiate Port-level tasks such as compliance tests and receiver Lane margining tests.

Port Operations are initiated by writing to the Port Capability in Adapter Configuration Space.

2.2.7 Time Synchronization

A USB4 Fabric provides time synchronization services between the Routers on the bus. Time synchronization is provided both within a single Domain and across multiple Domains.

Each Router tracks its time and frequency shift relative to a Host Router Clock on the bus. A Time Management Unit (TMU) in each Router is responsible for time synchronization operations within the Router.

2.2.8 USB4 Fabric Data Integrity

The USB4 Fabric defines the following data Integrity mechanisms to ensure that channel errors are detected and possibly corrected:

- Cyclic Redundancy Codes (CRC) are used to identify and correct packet errors. CRC are in the payload of AT Transactions and RT Transactions, in the header of Transport Layer Packets, in the payload of Control Packets, in the payload of Time Sync Packets, and in the payload of DisplayPort AUX Packets.
- Forward Error Correction (FEC) is used in the USB4 Link to reduce the BER of the channel.
- A Connection Manager may retransmit a Control Packet if a response is not received in time.

- A Router can retransmit an AT Transaction or an RT Transaction if a response is not received in time.
- Packets are checked for structure and contents.
- A Link-level flow control mechanism ensures that critical traffic is not lost due to buffer overflow. Link flow control operates independently of any flow control deployed by a Tunneled Protocol. Flow control deployed by a Tunneled Protocol is handled by the respective Tunneled Protocol stack.

2.2.9 Global Life of a Router

The following steps give a high level overview of what happens to a Router from the time it is hot-plugged into a bus until the time it is removed from the bus:

1. Router sets default values into the Configuration Space registers.
2. Router is hot-plugged into a Domain via its Upstream Facing Port.
3. Upstream Facing Port negotiates USB4 as described in the USB PD Specification.
4. Router participates in Lane Initialization to bring the USB4 Links into Active state (Section 4.1.2).
5. Router enables Control Packet routing and scheduling.
6. Connection Manager performs its first access to the Router, enumerating it.
7. Connection Manager configures the Router using Read Requests (Section 6.4.2.3) and Write Requests (Section 6.4.2.5). Router configuration includes setting up any Paths through the Router.
8. Router is ready to route and process Tunneled Protocol traffic.
9. If another Router is plugged into a Downstream Facing Port:
 - Downstream Facing Port negotiates USB4 as described in the USB PD Specification.
 - Router participates in Lane Initialization on the plugged Port.
 - After the USB4 Link is Active, the Router sends a Hot Plug Event Packet to the Connection Manager and waits for a Hot Plug Acknowledgment Packet (Section 6.8.1).
10. If a Downstream Router is unplugged:
 - Router discards any packets that would otherwise be routed to the unplugged Router.
 - Router sends a Hot Plug Event Packet to the Connection Manager and waits for a Hot Plug Acknowledgment Packet (Section 6.8.2).
 - Router inactivates Downstream Link (Section 4.4.5).
11. If the Router is disconnected from bus, it goes through Disconnect (Section 4.4.5).

2.2.10 Protocol Tunneling

A USB4 Host supports USB3 Gen X Tunneling, DisplayPort Tunneling, and Host-to-Host Tunneling. A USB4 Host can also optionally support PCIe Tunneling and/or USB3 Gen T Tunneling.

A USB4 Hub supports USB3 Tunneling, DisplayPort Tunneling, PCIe Tunneling, and Host-to-Host Tunneling. There are multiple ways that a USB4 Hub supports DisplayPort Tunneling:

- The USB4 Hub acts as a “pass through” for DisplayPort Tunneling (i.e. the USB4 Hub routes tunneled traffic directly between two of its USB4 Ports).
- The USB4 Hub contains a DP OUT Adapter that receives Tunneled DisplayPort traffic from a USB4 Port and sends it to a DisplayPort Sink.

- The USB4 Hub optionally contains a DP IN Adapter that sends DisplayPort traffic from a DisplayPort Source to a USB4 Port, which transmits Tunneled DisplayPort Traffic.

A USB4 Hub acts as a “pass through” for Host-to-Host Tunneling and for USB3 Gen T Tunneling. A USB4 Hub does not contain a Host Interface Adapter. A USB4 Hub can optionally contain a USB3 Gen T Adapter. In this case, the USB4 Hub can also act as an endpoint for USB3 Gen T traffic.

A USB4 Device optionally supports USB3 Tunneling, DisplayPort Tunneling, and/or PCIe Tunneling. A Device Router does not support Host-to-Host Tunneling.

2.2.10.1 USB3 Tunneling

There are two ways that USB3 traffic can be tunneled: USB3 Gen X Tunneling and USB3 Gen T Tunneling. USB3 Gen X Tunneling is described in Section 2.2.10.1.1. USB3 Gen T Tunneling is described in Section 2.2.10.1.2.

USB3 Gen X Tunneling utilizes the existing USB 3.2 protocol to tunnel USB traffic through a USB4 Domain.

USB3 Gen T uses a modified version of the USB 3.2 protocol to more efficiently utilize the higher USB3 bandwidth that is available within a USB4 Domain. The changes and optimizations to the USB 3.2 protocol are based on typical topologies expected to be encountered in real world usage. In these topologies, most USB4 Domains involve two hub tiers, which is the basis for all subsequent timing, link, protocol, and framework changes.

A Router that supports Version 1.0 of this specification only supports USB3 Gen X Tunneling.

2.2.10.1.1 USB3 Gen X Tunneling

A USB4 Host supports USB3 Gen X tunneling by incorporating an Internal USB3 Host Controller with one or more USB3 Gen X Ports (Enhanced SuperSpeed Host depicted in Figure 2-15).

Figure 2-15 depicts a USB4 Host that supports USB3 Gen X Tunneling.

Figure 2-15 Example of a USB4 Host with USB3 Gen X Tunneling Highlighted

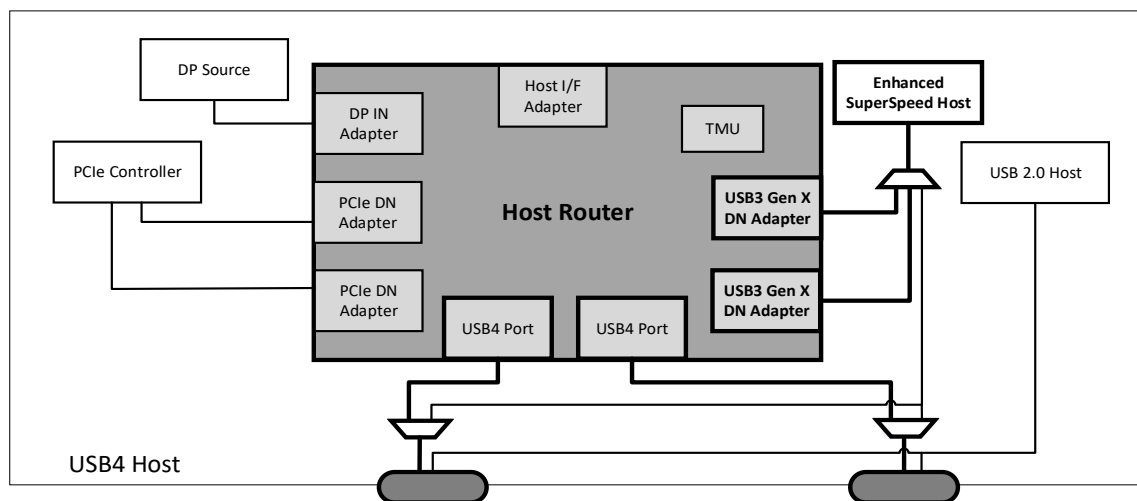
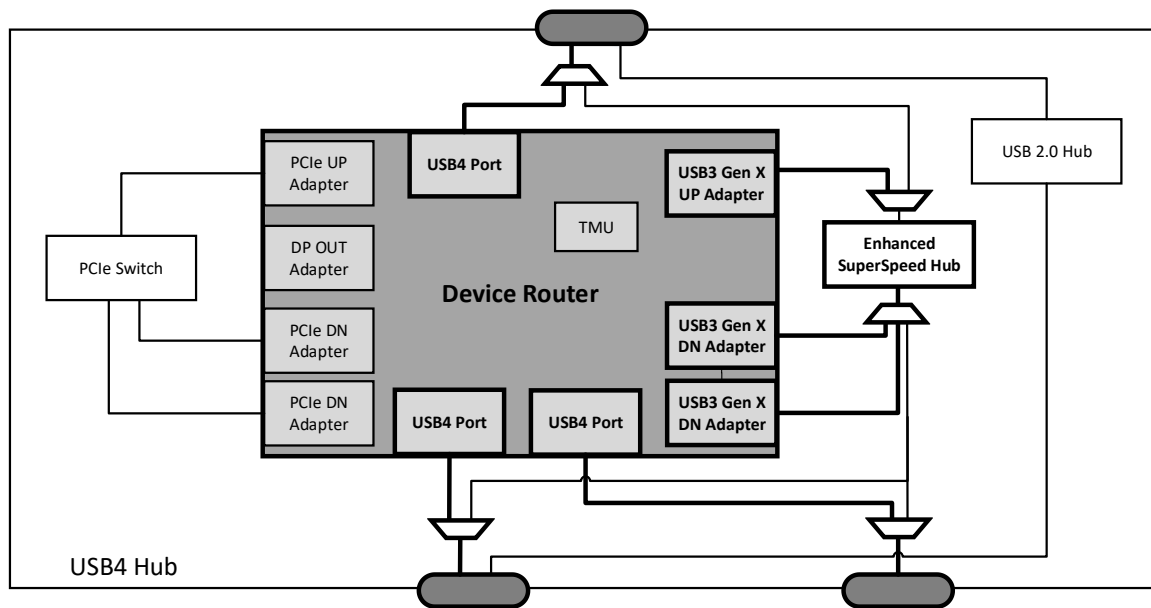
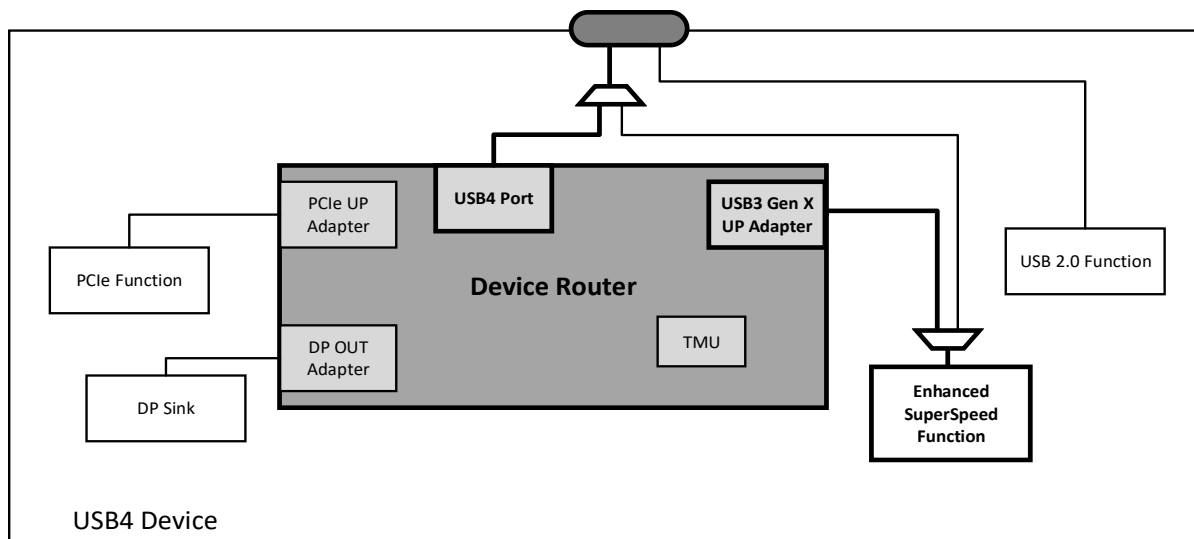


Figure 2-16 depicts a USB4 Hub. A USB4 Hub contains an internal Enhanced SuperSpeed Hub. The internal Enhanced SuperSpeed Hub exposes one or more downstream USB3 Gen X Ports, which can be connected to a USB Endpoint or downstream USB3 Gen X Protocol Adapter. The upstream port of the internal Enhanced SuperSpeed Hub interfaces with an Upstream USB3 Gen X Protocol Adapter that forwards packets to the Upstream Facing Port of the USB4 Hub.

Figure 2-16. Example of a USB4 Hub with USB3 Gen X Tunneling Highlighted

A USB4 Peripheral Device can contain an internal Enhanced SuperSpeed Function. Figure 2-17 depicts a USB4 Peripheral Device with an internal USB peripheral device. The internal Enhanced SuperSpeed Function interfaces with the Router via a USB3 Gen X Protocol Adapter.

Figure 2-17. Example of a USB4 Peripheral Device with USB3 Gen X Tunneling Highlighted

A USB4 Peripheral Device can optionally implement multiple internal Enhanced SuperSpeed Functions and/or expose external downstream facing USB3 Gen X Ports. In that case, an internal Enhanced SuperSpeed Hub can replace the Enhanced SuperSpeed Function shown in Figure 2-17 and a selection of functions would then connect to the downstream ports on that internal hub.

Figure 2-18 shows the USB3 Protocol stack as it applies to USB3 Gen X Protocol Adapter. The Link and Protocol Layers in the internal USB hub or the internal USB peripheral device implement a subset of the Link Layer defined in the USB 3.2 Specification.

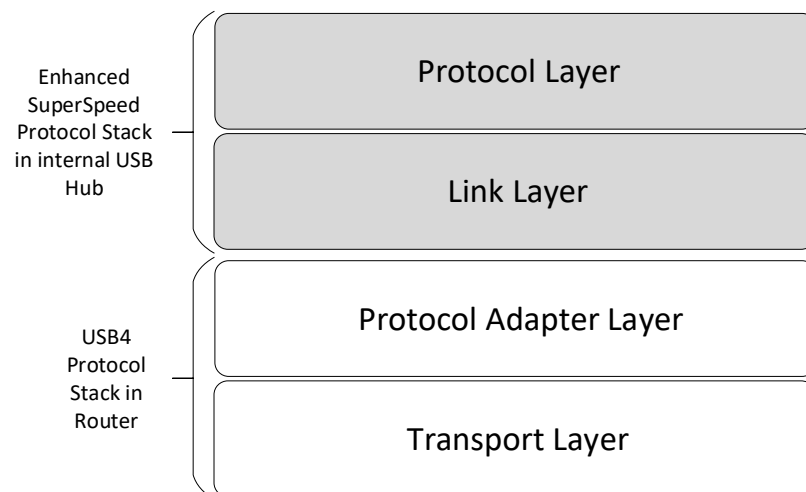
Figure 2-18. Protocol Stack for USB3 Tunneling

Figure 2-19 shows an example flow that tunnels USB3 traffic over a USB4 Fabric.

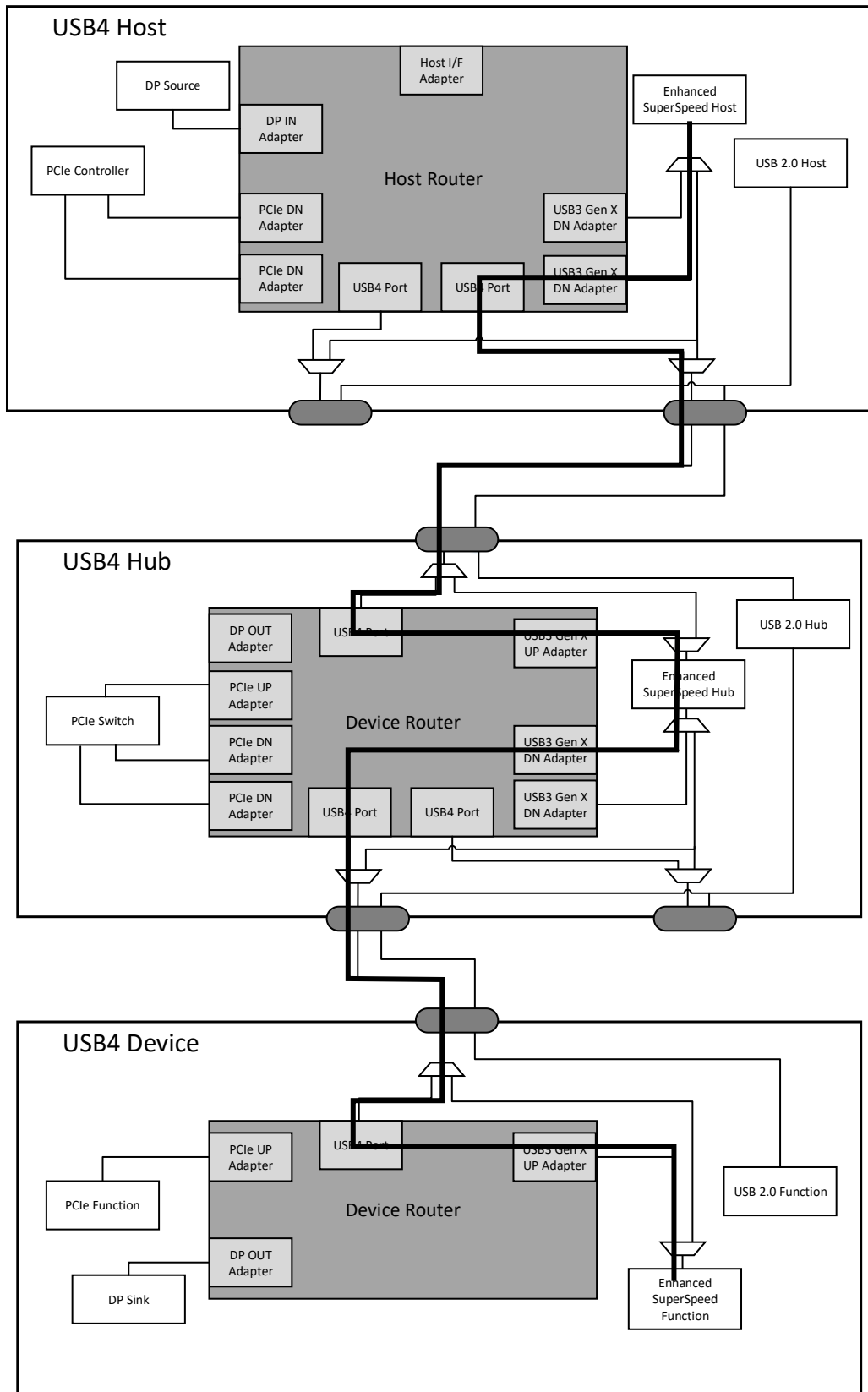
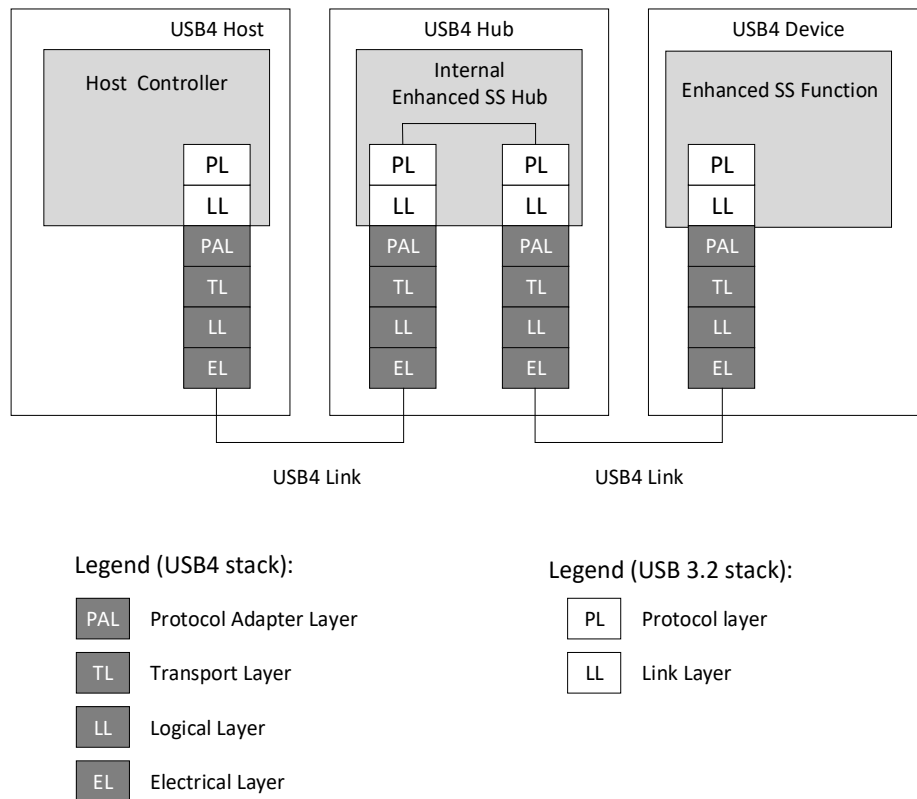
Figure 2-19. Example of a USB4 Fabric with USB3 Gen X Tunneling

Figure 2-20 shows the protocol stacks traversed along the tunnel between the Enhanced SuperSpeed Host and the Enhanced SuperSpeed function in Figure 2-19.

Figure 2-20. Protocol Stacks along a USB3 Gen X Tunnel

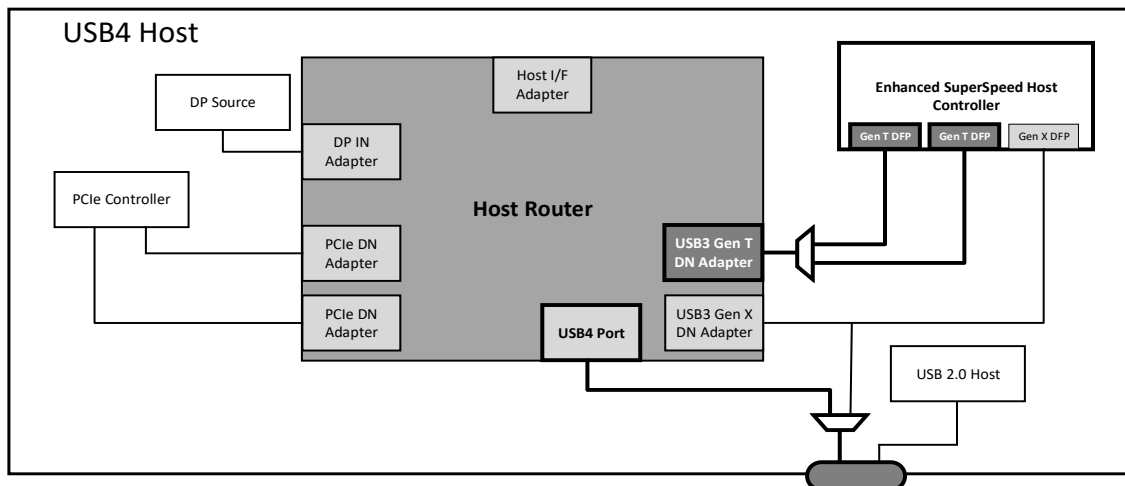


2.2.10.1.2 USB3 Gen T Tunneling

A USB4 Host supports USB3 Gen T tunneling by incorporating an Internal USB3 Host Controller with one or more USB3 Gen T downstream facing ports (Enhanced SuperSpeed Host depicted in Figure 4-20).

Figure 4-20 depicts a USB4 Host that supports USB3 Gen T Tunneling.

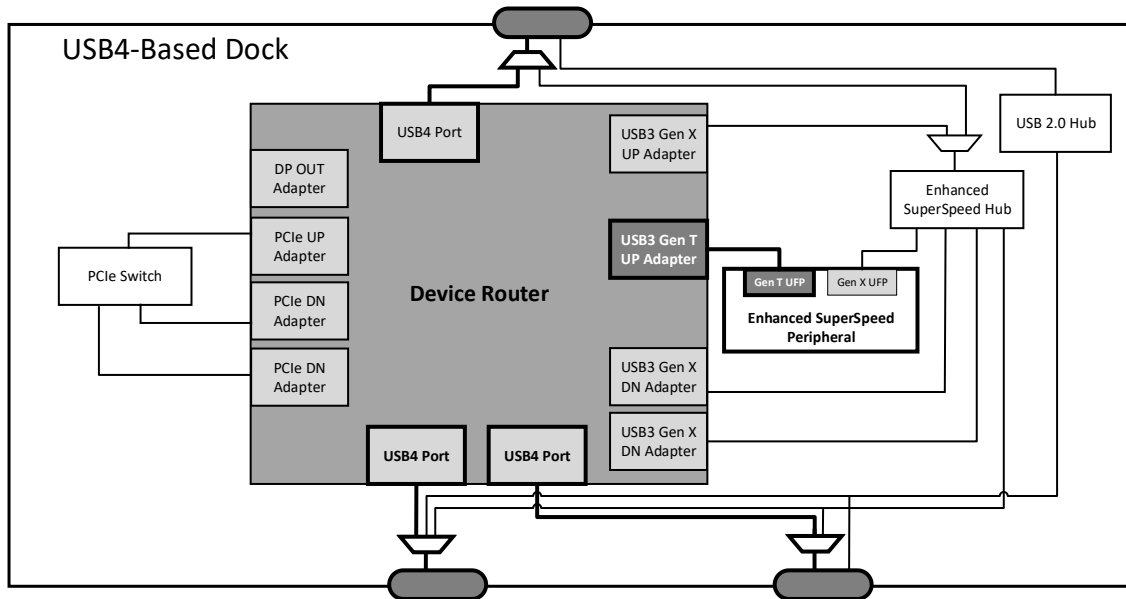
Figure 2-21 Example of a USB4 Host with USB3 Gen T Tunneling Highlighted



A USB4 Hub supports USB3 Gen T Tunneling as a “pass through”, meaning that USB3 Gen T traffic is routed directly between the Upstream Facing Port of the USB4 Hub and a Downstream Facing Port of the USB4 Hub without passing through any additional Protocol Adapters or USB3 components.

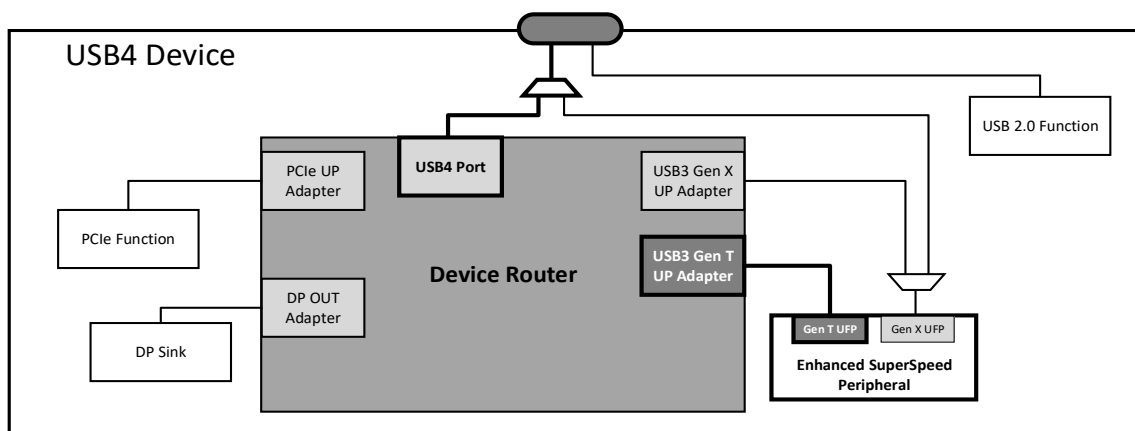
A USB4-Based Dock can also optionally contain an internal Enhanced SuperSpeed Peripheral with a USB3 Gen T upstream port. The upstream port of the internal Enhanced SuperSpeed Peripheral interfaces with an Upstream USB3 Gen T Protocol Adapter that forwards packets to the Upstream Facing Port of the USB4-Based Dock. Figure 2-22 depicts a USB4-Based Dock that contains an internal Enhanced SuperSpeed peripheral.

Figure 2-22. Example of a USB4-Based Dock with USB3 Gen T Tunneling Highlighted



A USB4 Peripheral Device can contain an internal Enhanced SuperSpeed Peripheral with a USB3 Gen T upstream port. Figure 2-23 depicts a USB4 Peripheral Device with an internal Enhanced SuperSpeed Peripheral. The internal Enhanced SuperSpeed Peripheral interfaces with the Router via a USB3 Gen T Protocol Adapter.

Figure 2-23. Example of a USB4 Peripheral Device with USB3 Gen T Tunneling Highlighted



A USB4 Peripheral Device can optionally implement multiple internal Enhanced SuperSpeed Peripherals. In that case, each Peripheral interfaces directly with the USB3 Gen T Protocol Adapter.

The USB3 Protocol stack for a USB3 Gen T Protocol Adapter is the same as for a USB3 Gen X Protocol Adapter (see Figure 2-18). The Link and Protocol Layers in the internal Enhanced SuperSpeed Peripheral implement a subset of the Link Layer defined in the USB 3.2 Specification. The Link and Protocol Layers in the internal Enhanced SuperSpeed Peripheral implement a subset of the Link Layer defined in the USB 3.2 Specification with the modifications defined in this specification.

Figure 2-24 shows an example flow that tunnels USB3 Gen T traffic over a USB4 Fabric. In Figure 2-24, the USB4 Hub acts as a pass through between the USB4 Host and USB4 Device.

Figure 2-24. Example of a USB4 Fabric with USB3 Gen T Tunneling (USB4 Device as Endpoint)

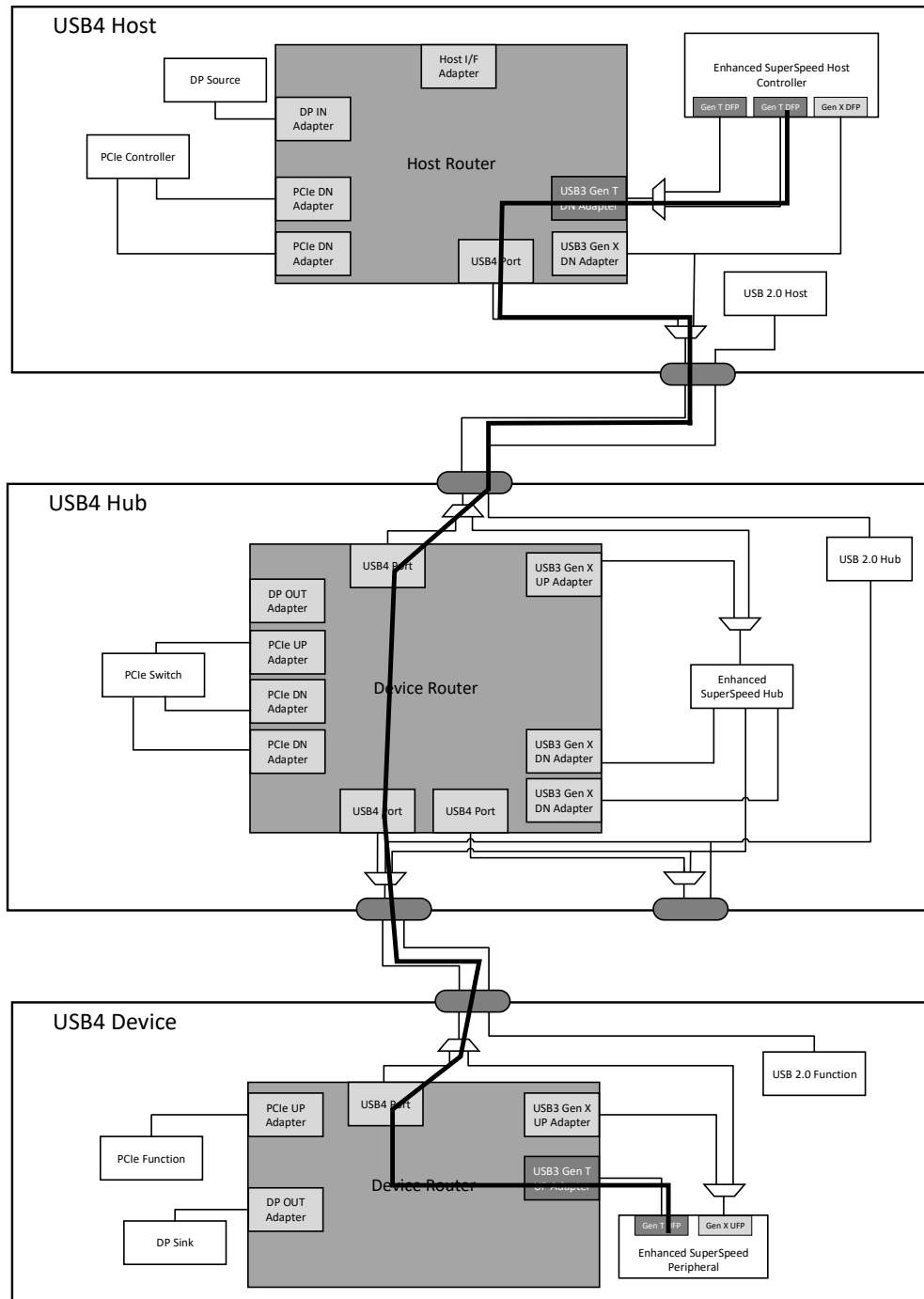
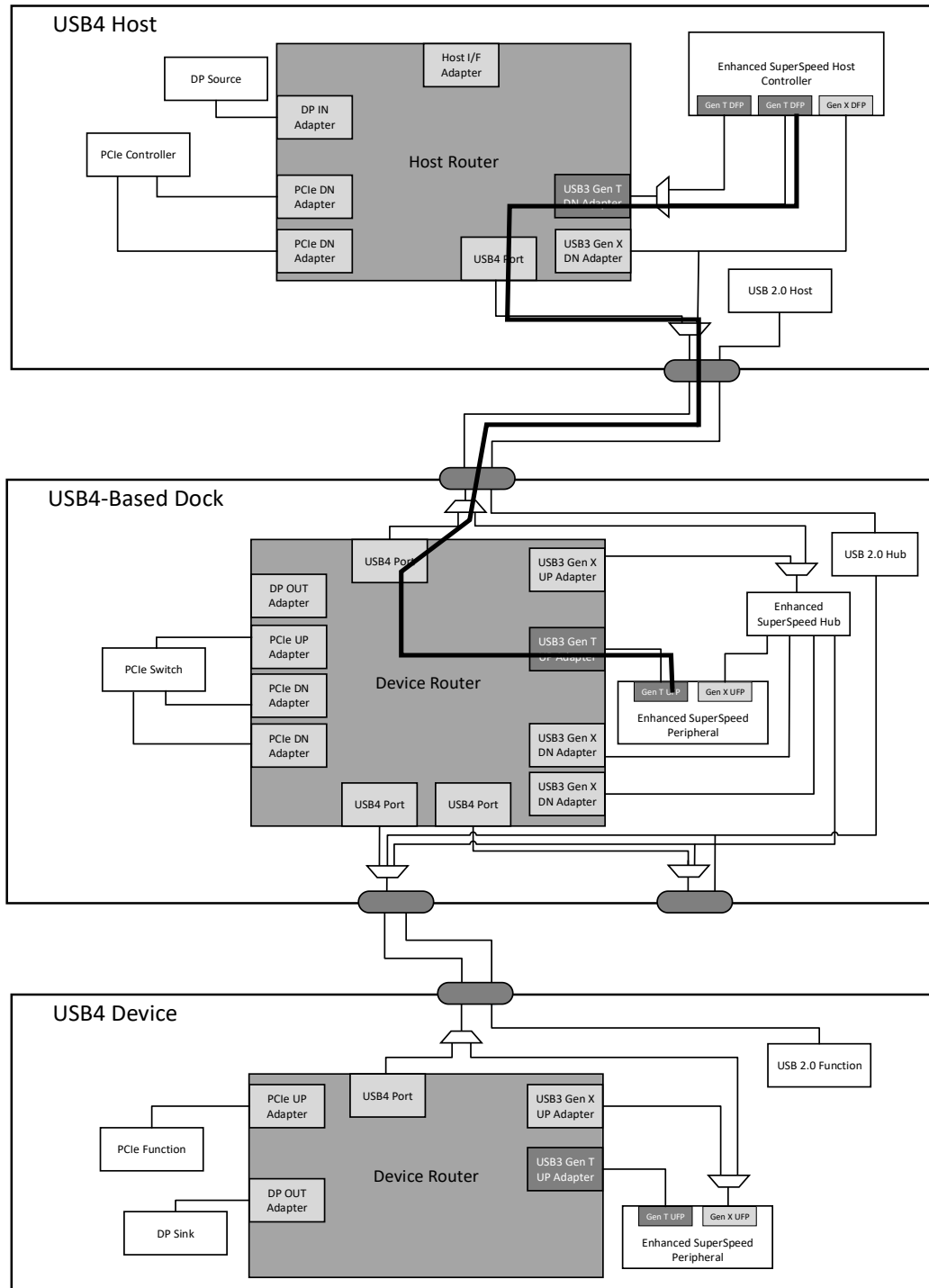


Figure 2-25 shows a second example flow that tunnels USB3 Gen T traffic over a USB4 Fabric. In Figure 2-25, the USB4-Based Dock contains a USB3 Gen T endpoint.

Figure 2-25. Example of a USB4 Fabric with USB3 Gen T Tunneling (USB4-Based Dock as Endpoint)



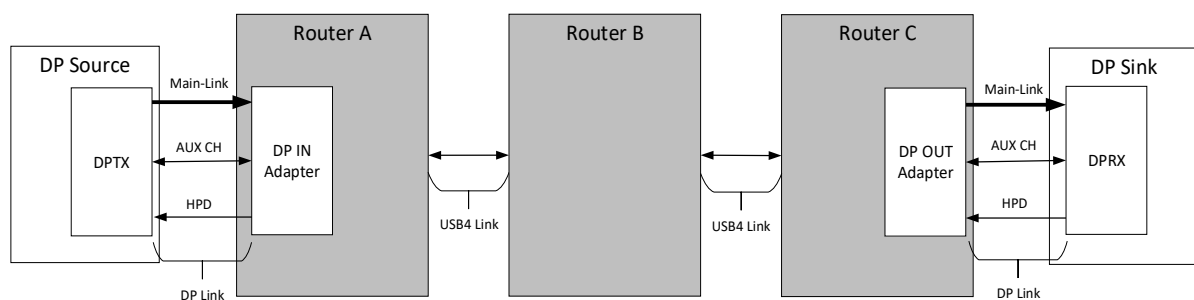
2.2.10.2 Display Tunneling

The USB4 Display Tunneling protocol is based on the DisplayPort Specification.

There are two types of DisplayPort™ Protocol Adapters: DP IN Protocol Adapters and DP OUT Protocol Adapters. A DP IN Protocol Adapter interfaces with a DisplayPort Source via a DP link. A DP OUT Protocol Adapter interfaces with a DisplayPort Sink via a DP link. A Router may contain one or more DP IN Protocol Adapters, one or more DP OUT Protocol Adapters, or a combination of DP IN and DP OUT Protocol Adapters. The DisplayPort tunnel over the USB4 Fabric has no directionality constraint other than starting at a DP IN Protocol Adapter and ending at a DP OUT Protocol Adapter.

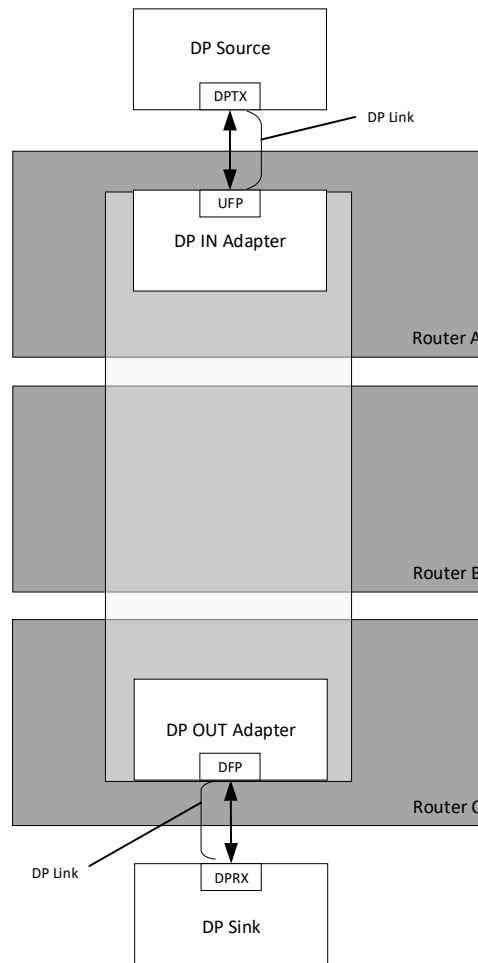
Figure 2-26 shows the general topology of a system that tunnels DisplayPort traffic over the USB4 Fabric.

Figure 2-26. Example Topology for DisplayPort Tunneling

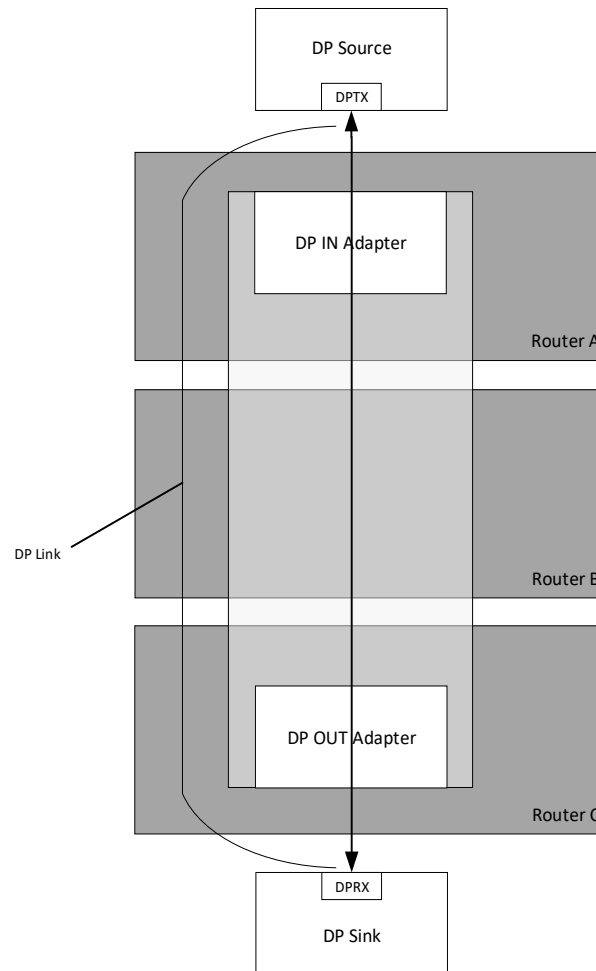


A DP Protocol Adapter can either operate in LTTPR Non-Transparent mode, LTTPR Transparent mode, or Non-LTTPR mode. In LTTPR Non-Transparent and LTTPR Transparent modes, the DP OUT Protocol Adapter and DP IN Protocol Adapter behave as a single LTTPR. In Non-LTTPR mode, the DP OUT Protocol Adapter and DP IN Protocol Adapter behave such that DPRX appears to be directly attached to DPTX.

Figure 2-27 shows the system in Figure 2-26 from a DisplayPort perspective when the DP IN and DP OUT Protocol Adapters are in Non-Transparent and LTTPR Transparent modes. Figure 2-28 shows the system in Figure 2-26 from a DisplayPort perspective when the DP IN and DP OUT Protocol Adapters are in Non-LTTPR Mode.

Figure 2-27. DP IN and OUT Protocol Adapters in LTTPr Non-Transparent and LTTPr Transparent Modes

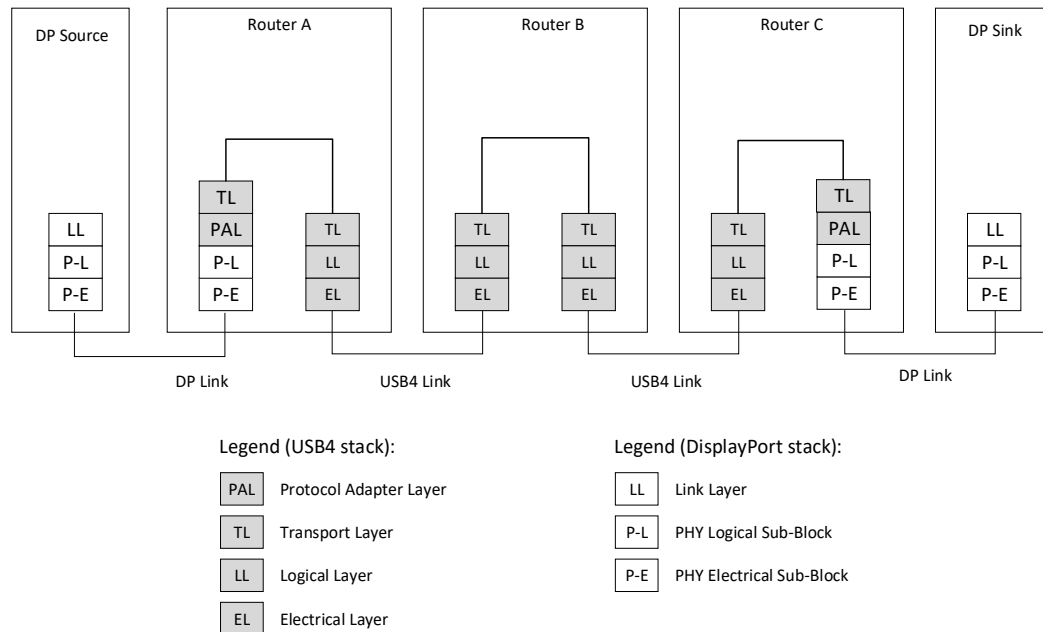
Note: A DP Tunnel appears as a single LTTPr. While there may be up to 8 LTTPrs between a DPTX and a DPRX, there can be no more than one DP Tunnel between a DPTX and a DPRX.

Figure 2-28. DP IN and OUT Protocol Adapters in Non-LTTPR Mode

A DP Protocol Adapter supports three Paths:

- An AUX Ingress Path for receiving AUX channel packets.
- An AUX Egress Path for sending AUX channel packets.
- A MAIN-Link Path for sending (in the case of a DP IN Protocol Adapter) or receiving (in the case of a DP OUT Protocol Adapter) Main-Link packets.

Figure 2-29 shows the protocol stacks traversed along a Path between the DP Source and DP Sink in Figure 2-26. The DisplayPort Link Layer, Physical Layer Logical Sub-Block, and Physical Layer Electrical Sub-Block are described in the DisplayPort Specification.

Figure 2-29. Protocol Stacks along a DisplayPort Tunneled Path

A Router can incorporate an MST branch splitter in order to provide additional DisplayPort fanout. The methods for incorporating an MST branch splitter are outside the scope of this specification.

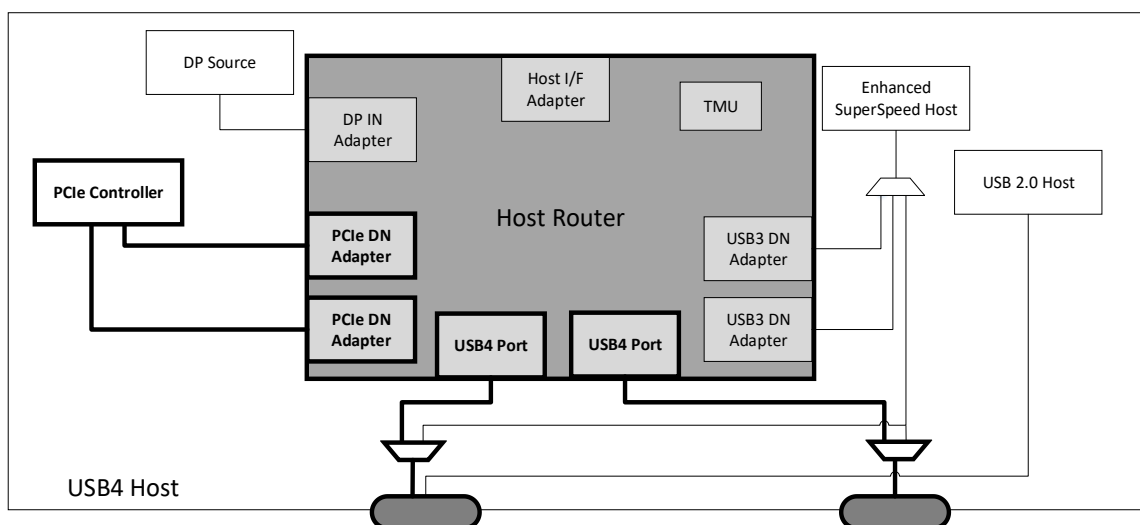
2.2.10.3 PCIe Tunneling

PCIe Tunneling is based on the PCI Express (PCIe) specification.

A USB4 Host supports PCIe tunneling by any of the following methods:

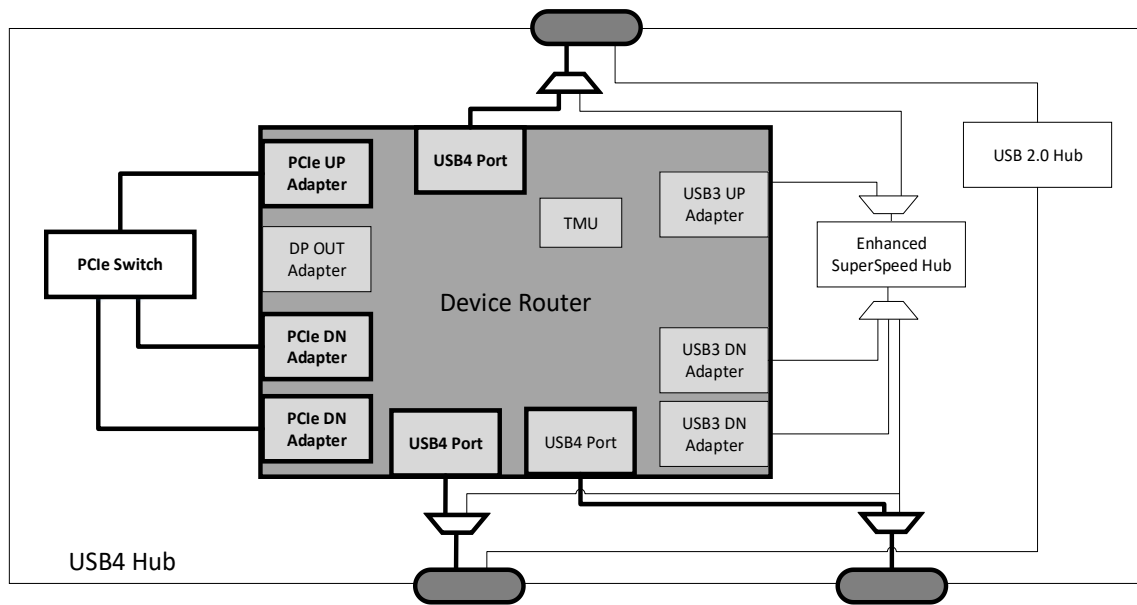
- Incorporating an internal PCIe Switch.
- Connecting to a PCIe Root Complex via PCIe Root Ports.

Figure 2-30 depicts a USB4 Host connected to PCIe Root Ports.

Figure 2-30. Example Structure of a USB4 Host with PCIe Tunneling Highlighted

A USB4 Hub that tunnels PCIe traffic contains an internal PCIe Switch to forward PCIe traffic to its Downstream Facing Ports. Figure 2-31 depicts a USB4 Hub highlighting the PCIe tunneling features. The internal Switch interfaces with the Router via PCIe Protocol Adapters. The PCIe Switch exposes one or more Downstream PCIe Ports, which can be connected to a PCIe Endpoint, PCIe Switch, or Downstream PCIe Protocol Adapter. The upstream port of the internal Switch interfaces with an Upstream PCIe Protocol Adapter that forwards packets to the Upstream Facing Port.

Figure 2-31. Example USB4 Hub with PCIe Tunneling Highlighted



A USB4 Device may tunnel PCIe traffic by incorporating an internal PCIe Endpoint or an internal PCIe switch. Figure 2-32 depicts a USB4 Device with an internal PCIe Endpoint.

Figure 2-32. Example USB4 Device with PCIe Tunneling Highlighted

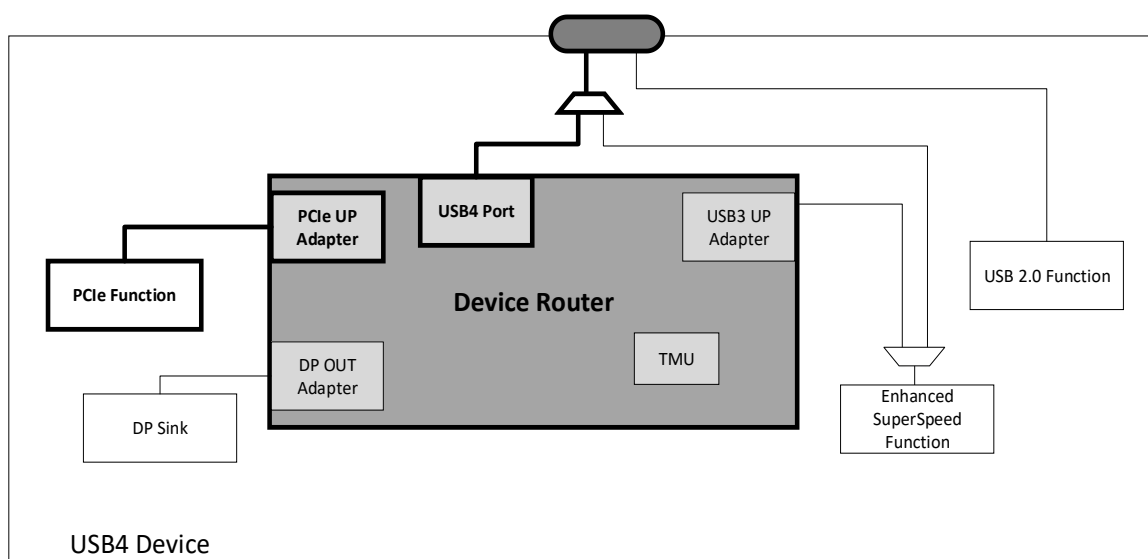


Figure 2-33 shows the PCIe Protocol stack as it interfaces with a PCIe Protocol Adapter. The Transaction Layer, Data Link Layer, and Physical Layer Logical sub-block in the internal PCIe Switch or the internal PCIe Endpoint implement a subset of the PCIe Specification.

Figure 2-33. Protocol Stack for PCIe Tunneling

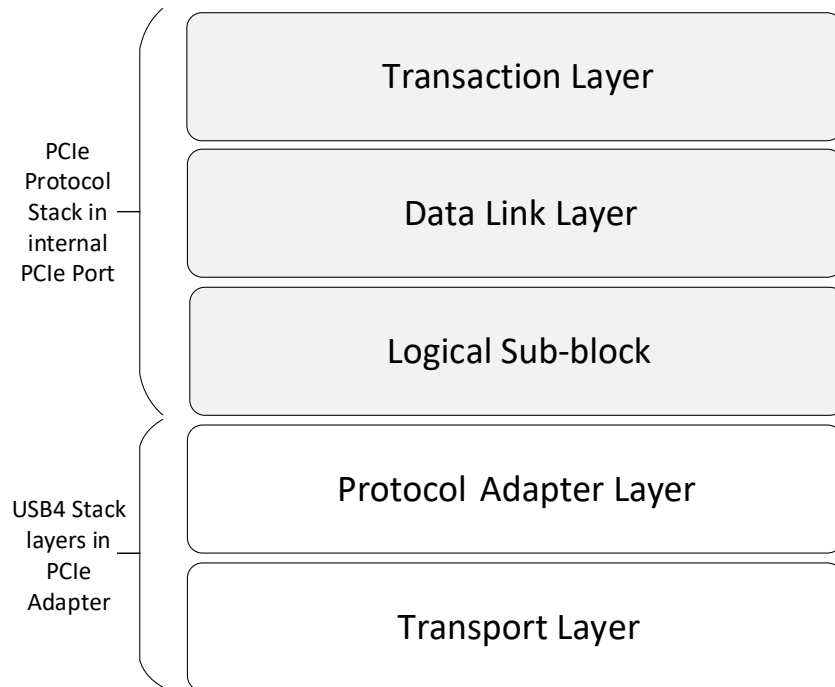


Figure 2-34 shows an example flow that tunnels PCIe traffic over a USB4 Fabric.

Figure 2-34. Example of a USB4 Fabric with PCIe Tunneling

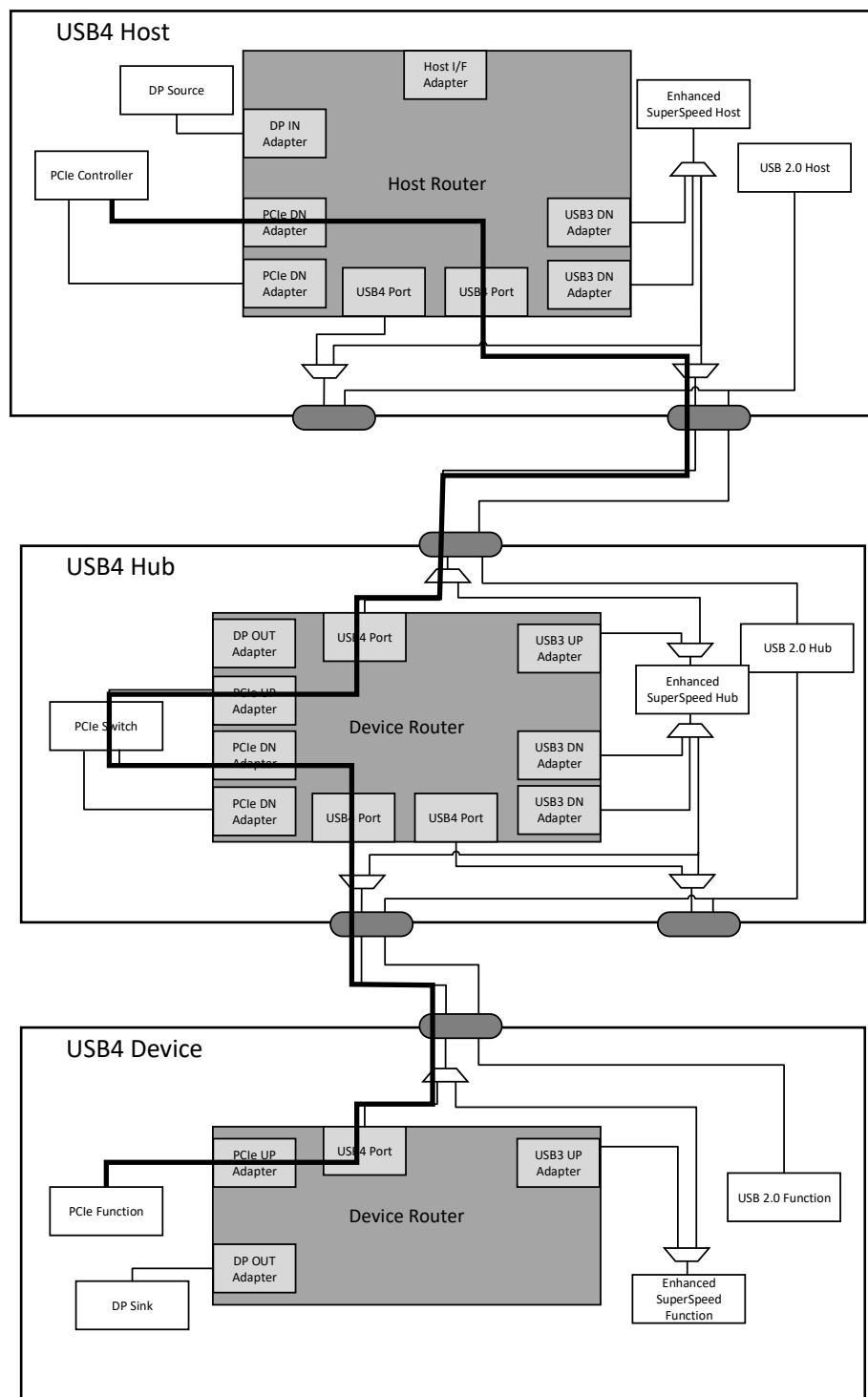
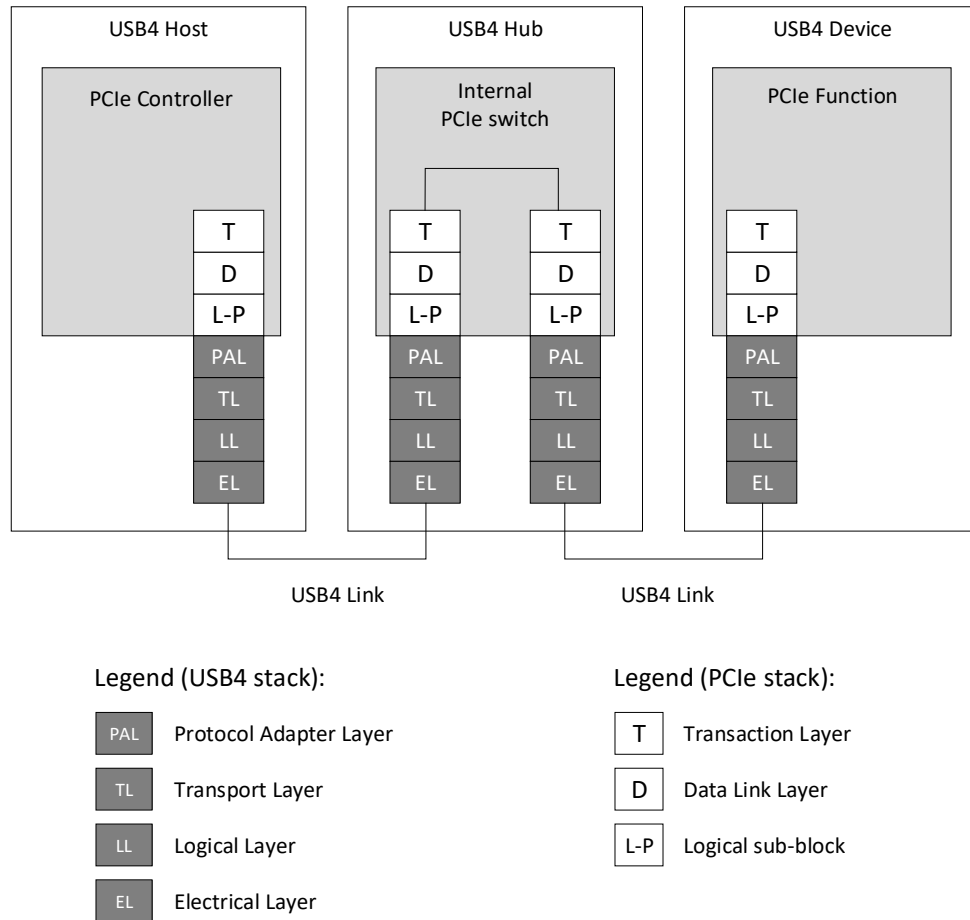


Figure 2-35 shows the protocol stacks along the tunnel in Figure 2-34.

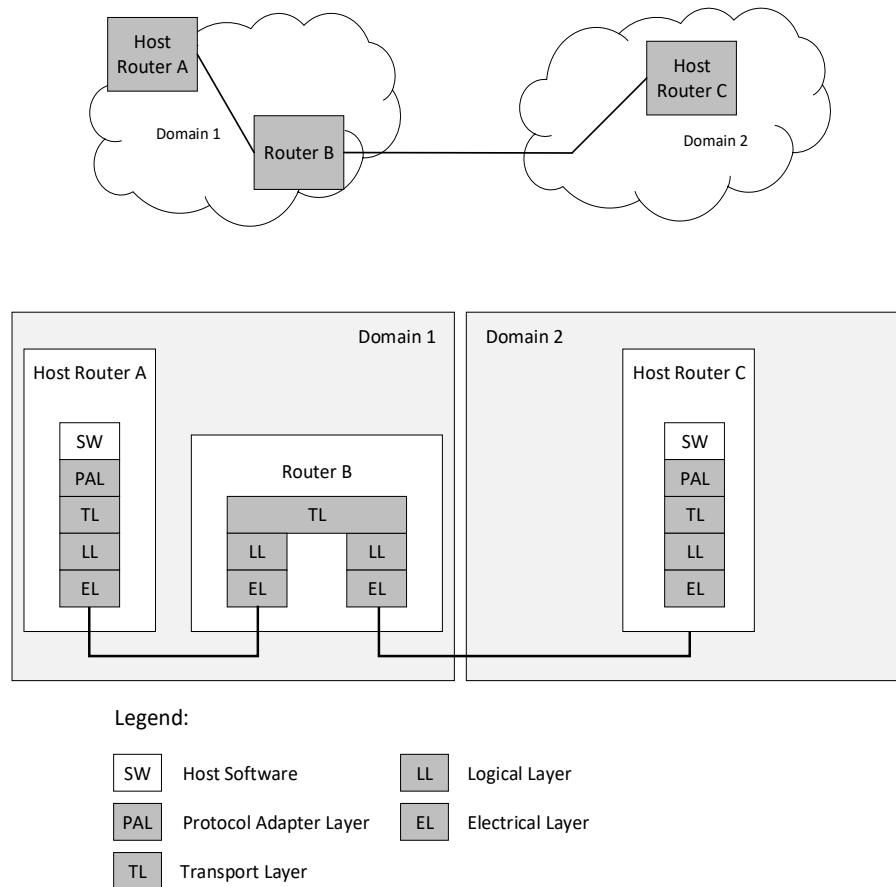
Figure 2-35. Protocol Stacks along a PCIe Tunnel



2.2.10.4 Host Interface Adapter

A Connection Manager interfaces with a Domain through the Host Interface Adapter in a Host Router. A Connection Manager sends Control Packets to and receives Control Packets from the Routers in its Domain via the Host Interface Adapter. A USB4 Host can also communicate with another USB4 Host via the Host Interface Adapter using USB4 Host-to-Host communication.

Figure 2-36 shows the protocol stacks traversed along a Path between two USB4 Hosts.

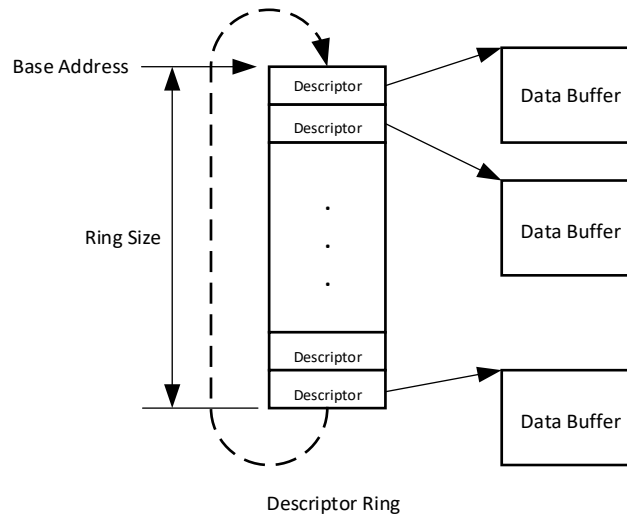
Figure 2-36. Protocol Stacks along a Path between Hosts

Two Modes of data transfer can be selected for Host-to-Host Tunneling:

- **Raw Mode** – When sending data, a USB4 Host posts the payload of a Tunneled Packet into a Host Memory buffer. The Host Interface Adapter Layer fetches the payload, encapsulates it in a Tunneled Packet, and forwards it to the Transport Layer within the Host Router. When receiving data, the Host Interface Adapter Layer posts the payload of received Tunneled Packets into Host Memory buffers.
- **Frame Mode** – When sending data, a USB4 Host posts a Frame of up to 4096 bytes into a Host Memory buffer. The Host Interface Adapter Layer fetches the Frame, segments it, and encapsulates each segment into a separate Tunneled Packet. When receiving data, the Host Interface Adapter Layer assembles Tunneled Packets received from the USB4 Fabric into the original Frame and posts the Frame to a Host Memory buffer.

A USB4 Host and a Host Interface Adapter interact via Descriptor Rings. Descriptor Rings reside in Host Memory. As depicted in Figure 2-37, a Descriptor Ring is a circular set of structures called Descriptors. Each Descriptor contains a reference to a Data Buffer in Host Memory and additional fields used to manage the transmit or receive flow.

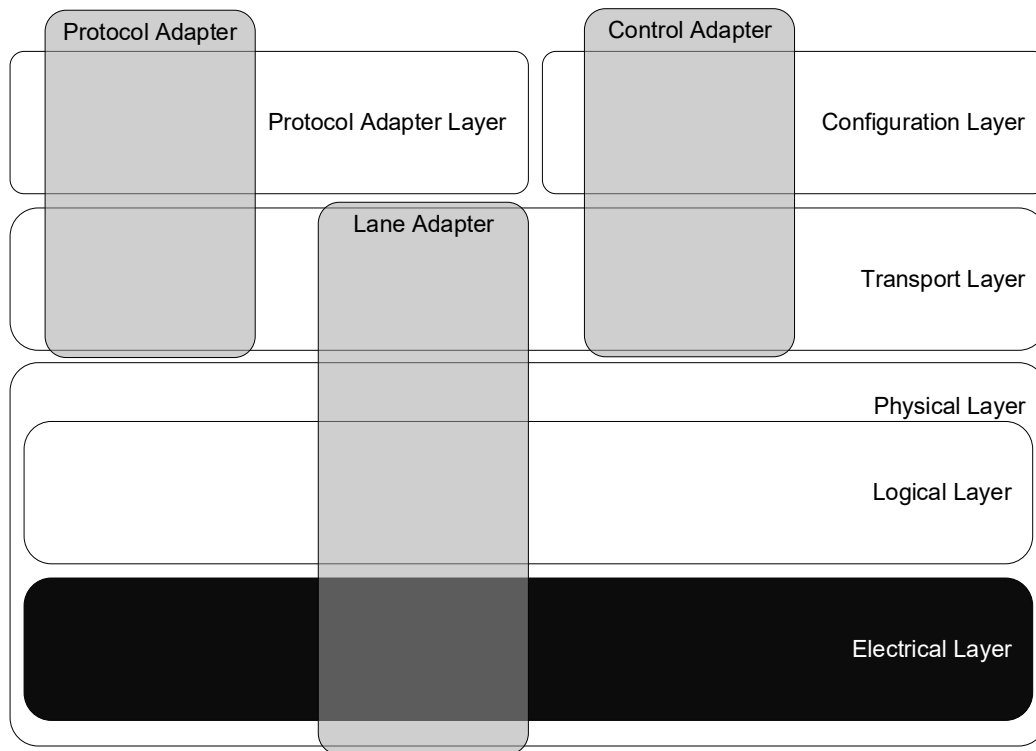
A Host Interface Adapter Layer supports the same number of Transmit Descriptor Rings and Receive Descriptor Rings. Each Transmit Descriptor Ring is assigned to one egress Path. Each Receive Descriptor Ring is assigned to one ingress Path.

Figure 2-37. Descriptor Ring and Data Buffers

The Host Interface Adapter Layer employs an end-to-end (E2E), credit-based flow control mechanism to prevent overflow of a Receive Descriptor Ring. Flow control is managed individually for each Transmit Descriptor Ring together with the Receive Descriptor Ring that is the destination for packets sent from the Transmit Descriptor Ring.

This specification defines in detail a PCIe-based Host Interface Adapter Layer interface that uses PCI device headers, a Memory BAR space, and PCI interrupts. A Host Router that is not PCIe-based can implement a different interface that provides equivalent functionality.

3 Electrical Layer



3.1 Gen 2 and Gen 3 Modes of Operation

This section describes the Electrical Layer specifications for a Router Assembly that supports the Gen 2 and Gen 3 modes of operation.

All Router Assemblies shall support Gen 2 speed (10 Gbps per Lane). A Router Assembly that is part of a USB4® Hub shall support Gen 3 speed (20 Gbps per Lane). A Router Assembly that is part of a USB4 Host or USB4 Device may optionally support Gen 3 speed (20 Gbps per Lane).

The Electrical Layer specifications detail the requirements and testing methodologies required for achieving reliable communication and obtaining interoperability of USB4 interconnects employing Passive or Active Cables. The Electrical Layer shall meet target Bit Error Ratio (BER) of 1E-12 or lower without applying Forward Error Correction. A USB4 Port shall use Spread-Spectrum-Clocking (SSC) to clock a USB4 Link. A USB4 Port employing dual transmitters shall use single clocking for both transmitters.

Note: The clock sources of two Link Partners are asynchronous with one another.

A Router Assembly is comprised of a Router and up to two Re-timers placed between the Router and the USB Type-C® connector. A Router Assembly may contain Linear Re-drivers between the Router and a Re-timer or between two Re-timers. If a Router Assembly contains Linear Re-drivers, a Re-timer shall be placed between the Linear Re-driver and the USB Type-C connector in order to meet the requirements in this section.

3.1.1 Gen 2 and Gen 3 Electrical Ecosystem**3.1.1.1 Insertion-Loss Considerations (Informative)**

The insertion-loss of the physical media is a key factor for facilitating USB4 electrical compliance. It is recommended that a Router Assembly limit the total insertion-loss from the USB Type-C® receptacle to the USB4 transceiver as follows:

- The total insertion-loss for a Router Assembly supporting Gen 2 is less than or equal to 5.5 dB at 5 GHz, including the receptacle tongue, the PCB trace, the integrated circuit's package and die load.
- The total insertion-loss for a Router Assembly that supports Gen 3 is less than or equal to 7.5 dB at 10 GHz, including the receptacle tongue, the PCB trace, the integrated circuit's package and die load.

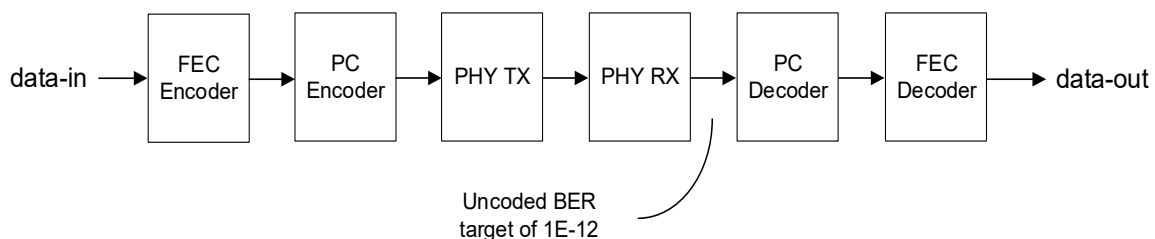
For a Captive Device that employs a passive attached cable, it is recommended that the device limit the total insertion-loss from the USB Type-C plug to the USB4 transceiver as follows:

- The total insertion-loss for a Captive Device supporting Gen 2 is less than or equal to 17.5 dB at 5 GHz, including the plug, the cable, the on-board connector, the PCB trace, the integrated circuit's package, and die load.
- The total insertion-loss for a Captive Device supporting Gen 3 is less than or equal to 15 dB at 10 GHz, including the plug, the cable, the on-board connector, the PCB trace, the integrated circuit's package, and die load.

3.1.1.2 Coded Bit-Error-Ratio Considerations (Informative)

The USB4 protocol employs a combination of Forward Error Correction (FEC) and Pre-Coding (PC) applied per Lane to provide enhanced data integrity. Figure 3-1 shows an example of this scheme.

Figure 3-1. Combined Forward-Error-Correction and Pre-Coding Scheme



The FEC scheme is based on Reed-Solomon RS(198,194) over GF(2⁸) code with two correctable errors per block. The Pre-Coder is designed for converting bursts of consecutive bit-errors into two errors at the beginning and end of the burst, supported by the RS-FEC. The combination of these two mechanisms provides high immunity for bursts of errors dominated by Decision Feedback Equalizers (DFE). Therefore, the coded BER performance is primarily impacted by the random bit-errors probability and not by long bursts of errors.

There is another effect that can cause more than two symbol errors in an RS-FEC block: If a multi-tap DFE is used in the receiver, when a burst of errors ends and the first DFE tap is fed by correct decision, errors still exist in the DFE pipeline, associated with the second tap and above. This increases the probability of having more bit errors until the pipeline is clean. As the first DFE tap is typically the most dominant tap, it is expected that the probability for additional errors is low, but still high as compared to the probability for random-errors, which correspond to the case where the DFE pipeline is clean. The probability that a burst will restart is dominated by the magnitude of the DFE taps with feedback delays of 2 UI or more. Therefore, any DFE taps after the first DFE tap need to be carefully controlled (or totally avoided) in order to minimize their impact on the coded performance.

Because direct measurement of the coded BER is not feasible due to the large measurement windows needed, an alternative indirect method is applied for validating the expected performance. Therefore, targets are specified for the random-errors probability and for the error burst restart probability, ensuring that the coded BER assumptions are met.

3.1.2 Gen 2 and Gen 3 Electrical Compliance Methodology

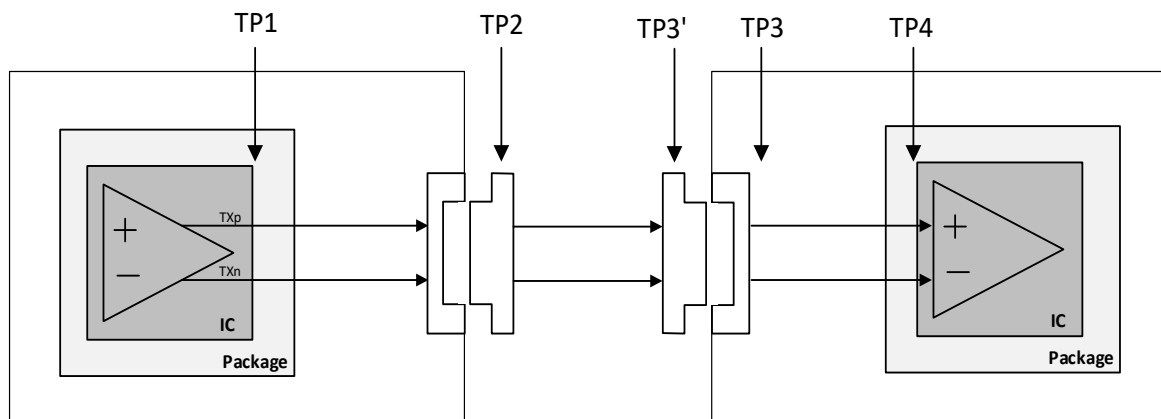
3.1.2.1 System Compliance Test Point Definitions

All measurements shall be referenced to the electrical compliance test points in Table 3-1. Calibration shall be applied in cases where direct measurement is not feasible.

Table 3-1. Electrical Compliance Test Points

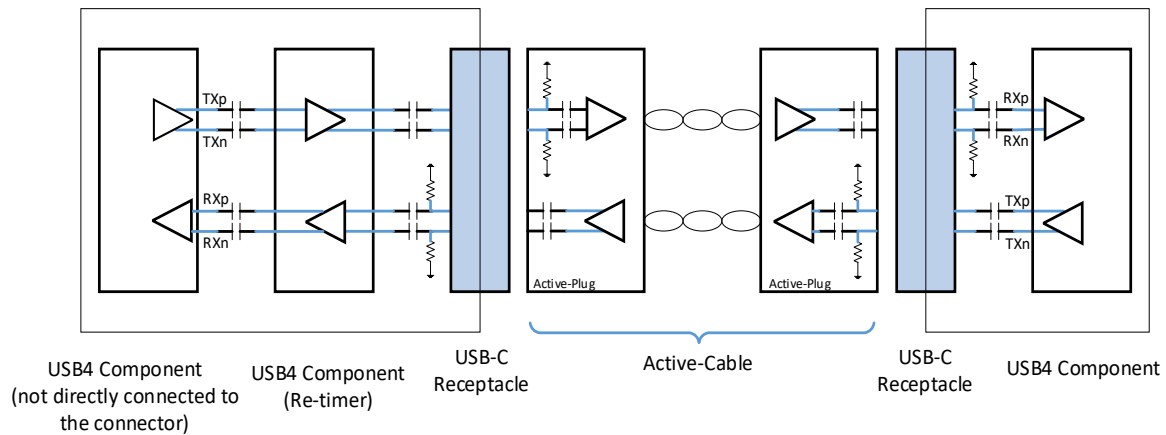
Test Point	Description	Comments
TP1	Transmitter IC output	Not used for electrical testing.
TP2	Transmitter port connector output	Measured at the plug side of the connector.
TP3	Receiver port connector output	Measured at the receptacle side of the connector. All the measurements at this point shall be done while applying reference equalization function.
TP3'	Receiver port connector input	Measured at the plug side of the connector.
TP4	Receiver IC input	Not used for electrical testing.

Figure 3-2. Compliance Points Definition



3.1.2.2 AC Coupling Capacitors

All of the Lane 0 and Lane 1 electrical interfaces of a Router Assembly shall be AC-coupled. The SBTX and SBRX lines shall not be AC-coupled. All Lane 0 and Lane 1 transmit paths of a Router Assembly shall include AC-coupling capacitance between 135 nF and 265 nF. All Lane 0 and Lane 1 receive paths of a Router Assembly that are directly connected to a USB Type-C connector shall include AC-coupling capacitance between 300 nF and 363 nF, together with discharge resistors between 200 K Ω and 242 K Ω . AC-coupling capacitors (with discharge resistors) may be also placed at the receive paths of a Router Assembly that are not directly connected to USB Type-C connector.

Figure 3-3. Examples for AC-Coupling Capacitor Placement**3.1.2.3 Reference Clock-and-Data-Recovery (CDR) Function**

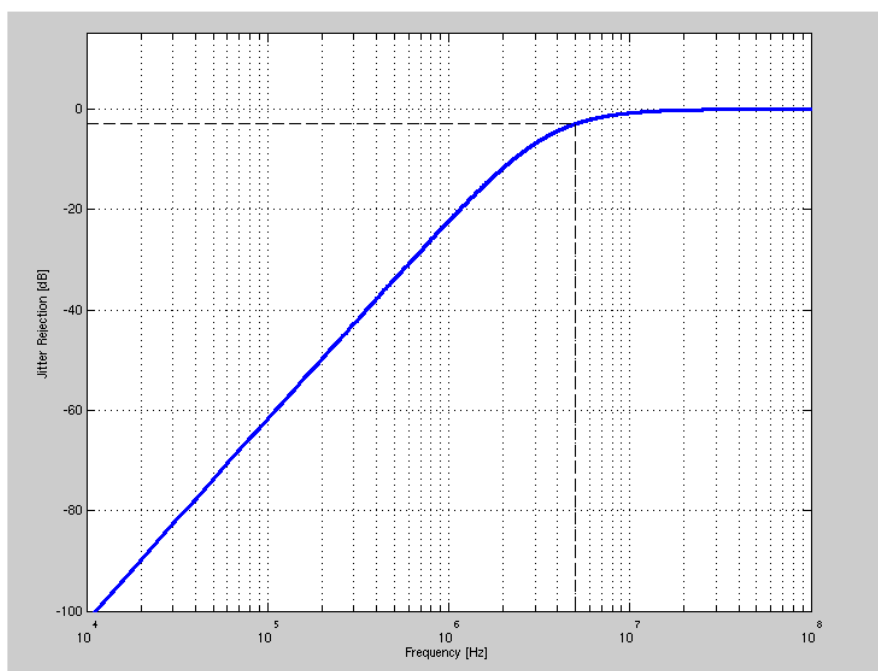
All jitter and eye diagram measurements shall be performed while applying a reference clock-and-data-recovery (CDR) function. The reference CDR is modeled by a 2nd order PLL response (type II), which derives the following jitter transfer function, described in Laplace domain:

$$H_{jitter}(s) = \frac{s^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2}$$

where:

- s is the frequency in Laplace domain
- ζ is the damping factor
- ω_n is the natural frequency of the system

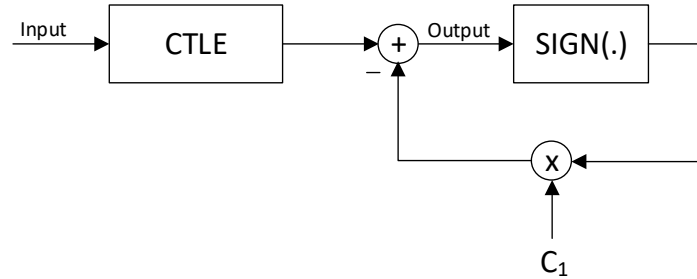
The damping factor and natural frequency used for compliance testing shall be 0.94 and 2.2E7 rad/sec respectively, forming High-Pass-Filter (HPF) mask with 3 dB bandwidth at 5 MHz.

Figure 3-4. Jitter Transfer Function

3.1.2.4 Reference Equalization Function

All the measurements at TP3 compliance point shall be performed while applying a reference receiver equalization function. The reference receiver equalization function is comprised of parametric Continuous-Time-Linear-Equalizer (CTLE) and Decision-Feedback-Equalizer (DFE), as described in Section 3.1.2.4.1 and Section 3.1.2.4.2 respectively.

A measurement that is referenced to TP3 shall use equalization parameters that optimize the calculated eye-diagram.

Figure 3-5. Reference Receiver Equalization**3.1.2.4.1 Reference CTLE**

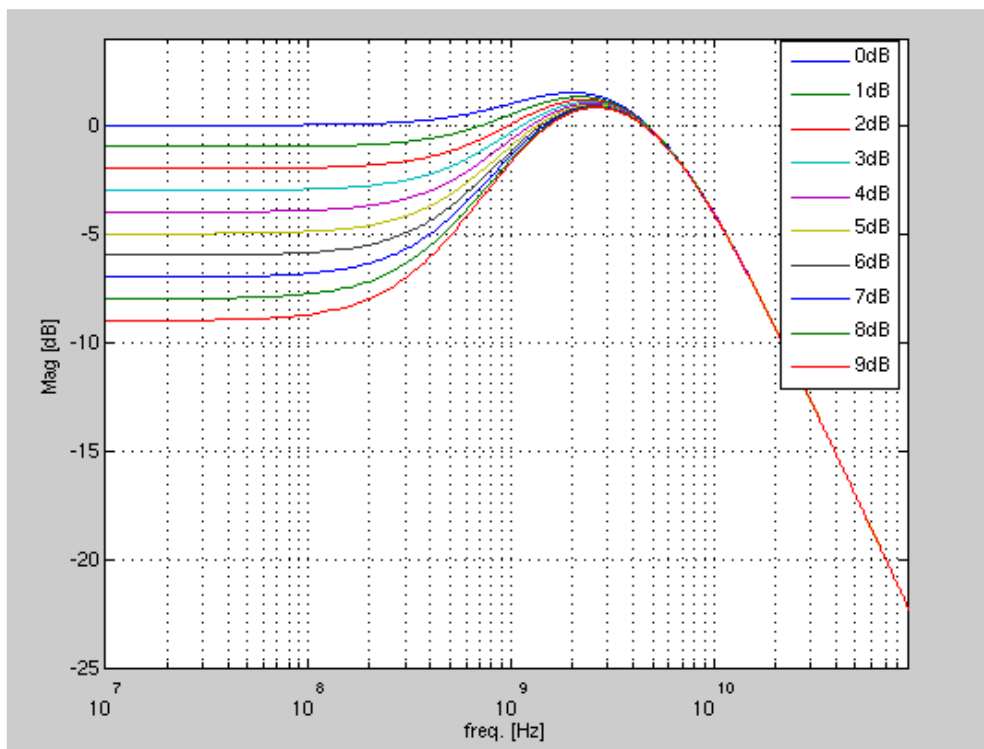
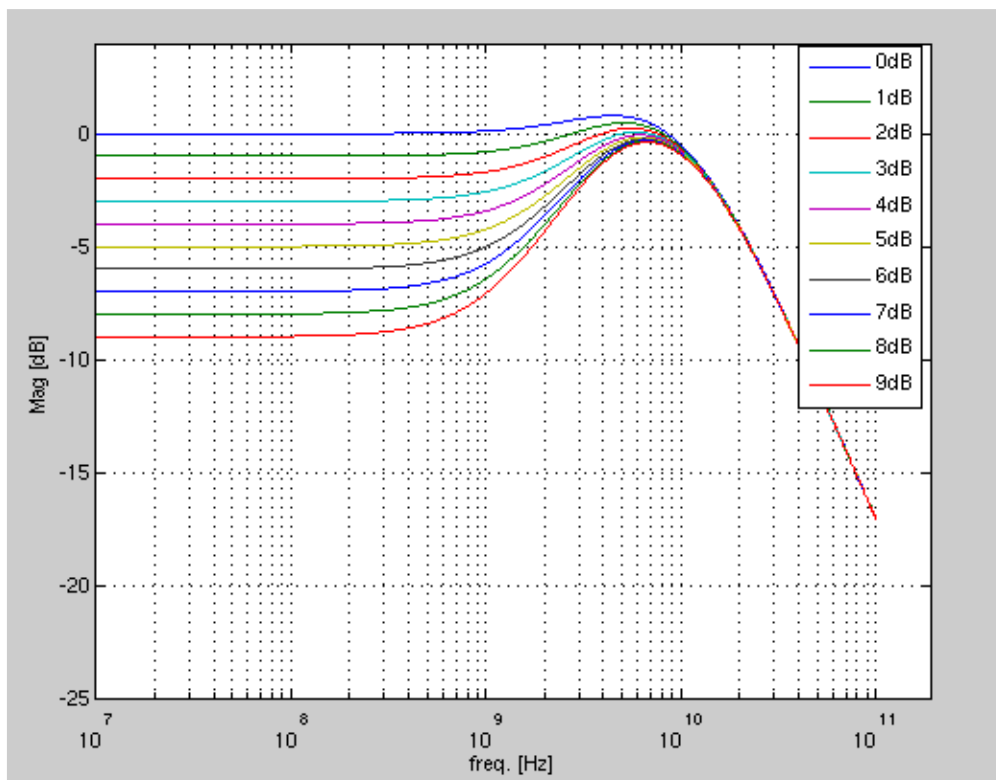
The following equation describes the frequency response for the USB4 reference CTLE that shall be used for compliance testing:

$$H(s) = 1.41 \cdot \omega_{p2} \cdot \frac{s + \frac{A_{DC}}{1.41} \cdot \omega_{p1}}{(s + \omega_{p1}) \cdot (s + \omega_{p2})}$$

where:

- A_{DC} is the DC gain
- s is the frequency in Laplace domain
- $\omega_{p1} = \begin{cases} 2 \cdot \pi \cdot 1.5e^9 \frac{rad}{sec} & Gen\ 2 \\ 2 \cdot \pi \cdot 5e^9 \frac{rad}{sec} & Gen\ 3 \end{cases}$
- $\omega_{p2} = \begin{cases} 2 \cdot \pi \cdot 5e^9 \frac{rad}{sec} & Gen\ 2 \\ 2 \cdot \pi \cdot 10e^9 \frac{rad}{sec} & Gen\ 3 \end{cases}$

Ten different CTLE configurations shall be applied such that A_{DC} is one of $\left\{10^{\frac{-x}{20}} : x = 0, 1, \dots, 9 [dB]\right\}$.

Figure 3-6. Frequency Response of Gen 2 Reference CTLE**Figure 3-7. Frequency Response of Gen 3 Reference CTLE**

3.1.2.4.2 Reference DFE

A 1-tap feedback filter is defined as part of the reference receiver equalizer used in the compliance testing. The DFE formula is described in the following equation:

$$Y_n = X_n - C_1 * \text{sign}(Y_{n-1})$$

where:

- Y_n is the DFE output at time instant n
- X_n is the DFE input (incoming signal after applying CTLE) at time instant n
- C_1 is the DFE coefficient, which shall be limited to a range of 0 mV to 50 mV

3.1.2.5 Time Domain Measurements

Time domain measurements shall be performed using a real-time oscilloscope (or equivalent equipment) with an input bandwidth of 21 GHz \pm 1 GHz and a single-ended impedance of 50 Ω . The time domain measurement equipment shall support the USB4 reference CDR defined in Section 3.1.2.3 and the reference Equalization function defined in Section 3.1.2.4, which both shall be applied as required for the measurements.

3.1.2.6 Compliance Boards

3.1.2.6.1 Compliance Plug Test Board

A high quality USB Type-C plug-to-SMA/SMP test fixture shall be used to enable Router Assembly compliance testing. The fixture shall be comprised of a USB Type-C plug and a short paddle card that can be connected to a coaxial cable with a SMA/SMP connector at its end. The reference points TP2 and TP3' are defined such that the insertion-Loss from the connector pads to the compliance points is 0.5 dB \pm 0.25 dB at 5 GHz and 1 dB \pm 0.25 dB at 10 GHz, and the fixture's insertion-Loss shall be calibrated accordingly. Extra loss and distortion elements shall be compensated by physical and/or mathematical means.

The target single-ended impedance of the fixture shall be 42.5 Ω .

3.1.2.6.2 Compliance Receptacle Test Board

A high quality USB Type-C receptacle-to-SMA/SMP test fixture shall be used to enable Router Assembly testing. The fixture shall be comprised of a high quality USB Type-C receptacle and a short PCB trace that may be connected to coaxial cable with SMA/SMP connector at its end. The reference point TP3 is defined such that the insertion-loss from the connector pads to the compliance point is 0.5 dB \pm 0.25 dB at 5 GHz and 1 dB \pm 0.25 dB at 10 GHz. Extra loss and distortion elements shall be compensated by physical and/or mathematical means.

The target single-ended impedance of the fixture shall be 42.5 Ω .

3.1.3 Gen 2 and Gen 3 Router Assembly Transmitter Compliance

Transmitter compliance testing for a Router Assembly is defined at two measurement point:

- The output of a compliance plug fixture at the TP2 reference point.
- The output of a compliance receptacle fixture at the TP3 reference point.

Compliance Plugs and Compliance Receptacles are defined in Section 3.1.2.6.1 and Section 3.1.2.6.2 respectively.

Unless otherwise specified, a transmitter shall drive PRBS31 pattern during compliance testing. All tests shall be performed with Spread-Spectrum-Clocking (SSC) enabled and while all neighboring transceivers are active.

3.1.3.1 Transmitter Specifications for Gen 2 and Gen 3

Table 3-2 defines the transmitter parameters that shall apply for both Gen 2 and Gen 3 modes of operation.

Table 3-2. Transmitter Specifications for Gen 2 and Gen 3 (at TP2)

Symbol	Description	Min	Max	Units	Conditions
RL_DIFF	Differential Return Loss, 0.05–12 GHz	--	See Section 3.1.3.1.2	dB	
RL_COMM	Common Mode Return Loss, 0.05–12 GHz	--	See Section 3.1.3.1.3	dB	
TX_EQ	Transmitter Equalization Setting	--	See Section 3.1.3.1.4		
SSC_DOWN_SPREAD_RANGE	Dynamic range of SSC down-spreading during steady-state	0.4	0.5	%	See Note 3, Note 4, and Figure 3-9.
SSC_DOWN_SPREAD_RATE	SSC down-spreading modulation rate during steady-state	30	33	KHz	See Note 4 and Figure 3-9.
SSC_PHASE_DEVIATION	Phase jitter associated with the SSC modulation during steady-state	2.5	22	ns pp	See Note 1, Note 4, and Figure 3-9.
SSC_SLEW_RATE	SSC frequency slew rate (df/dt) during steady-state	--	1250	ppm/ μs	See Note 2, Note 4, and Figure 3-9.
TX_FREQ_VARIATIONS_TRAINING	TX frequency variation during Link training, before obtaining steady-state	--	See Section 3.1.3.1.1	ppm	See Note 4.
LANE_TO_LANE_SKEW	Skew between dual transmit signals of the same USB4 Port	--	26	ns	See Note 5.
RISE_FALL_TIME	TX rise/fall time measured between 20–80% levels	10	--	ps	Test pattern shall be SQ128 (see Table 8-66).
V_ELEC_IDLE	Peak voltage during transmit electrical idle (one-sided voltage opening of the differential signal)	--	20	mV	See Note 6.
V_TX_DC_AC_CONN	Instantaneous DC+AC voltages at the connector side of the AC coupling capacitors	-0.5 (min1) -0.3 (min2)	1.0	V	See Note 7.

Notes:

1. SSC phase deviation shall be extracted from the transmitted signal. During this test, the transmitter shall be configured to send PRBS31 pattern. The SSC phase deviation shall be extracted from the signal phase after applying a 2nd order low-pass filter with 3 dB point at 5 MHz.
2. The SSC slew rate shall be extracted from the transmitted signal over measurement intervals of 0.5 μ s. The SSC slew-rate shall be extracted from the signal phase after applying a 2nd order low-pass filter with 3 dB point at 5 MHz.
3. SSC_DOWN_SPREAD_RANGE specifies the required SSC modulation depth, represented by the difference of the maximum and minimum modulated frequencies, referenced to the Link speed.
4. Steady-state clocking is applied from the point that SLOS training pattern is sent by the transmitter.
5. Total Lane-to-Lane skew measured at TP2 including the skew introduced by the physical media, by the Router IC TX, and by up to 2 Re-timers placed on the board. Informative Lane-to-Lane skew budget: Router IC TX pins: 8 ns, each Re-timer input-to-output: 8 ns, physical media mismatches: 2 ns.
6. V_ELEC_IDLE shall be extracted after applying first order low-pass filter with 3 dB point at 1.25 GHz.
7. The absolute single-ended voltage seen by the receiver. This requirement applies to all Link states, and during power-on and power-off. (min1, max) is measured with a 200 K Ω receiver load, and (min2, max) is measured with a 50 Ω receiver load. The ground offset between a DFP and UFP does not contribute to V_TX_DC_AC_CONN.

3.1.3.1.1 Transmitter Frequency Variations during Link Training**3.1.3.1.1.1 Background (Informative)**

A USB4 Link can include up to 6 Re-timers, which forward data from one end of the Link to the other end. During Link training, the transmitters at both ends of the Link send SLOS pattern. The SLOS pattern is clocked with SSC down spreading as specified in Table 3-2.

Re-timer transmitters on the Link are all enabled in parallel. Initially, the Re-timer transmitters do not forward the incoming data and just send CL_WAKE1.X Ordered Sets clocked at a local constant frequency (without SSC modulation). In the later stages of the Link training, the Re-timer transmitters sequentially switch to forwarding the incoming data at the incoming frequency. As soon as all the Re-timer transmitters complete the switching process, steady-state is obtained and SLOS pattern clocked with SSC is forwarded from one end of the Link to the other.

If a Link does not include any Re-timers, the transmitter frequency modulation is at its steady-state from the beginning of the Link training period, as clock switching does not take place.

3.1.3.1.1.2 Transmitter Specifications for Gen 2 and Gen 3

Table 3-3 specifies the limits on the transmitter frequency variation during Link training of a Router Assembly that includes one or more Re-timers.

Table 3-3. Transmitter Frequency Variation Limits During Link Training Before Obtaining Steady-State

Symbol	Description	Min	Max	Units	Conditions
INIT_FREQ_VARIATION	Initial non-modulated transmit frequency applied while sending CL_WAKE1.x pattern	-300	300	ppm	See Note 1.
DELTA_FREQ_200ns	Frequency variation during Link training over 200 ns measurement windows	--	1400	ppm	See Note 1.
DELTA_FREQ_1000ns	Frequency variation during Link training over 1 μ s measurement windows	--	2200	ppm	See Note 1.

Symbol	Description	Min	Max	Units	Conditions
FREQ_OVERSHOOT	Maximum transient frequency offset from the Link baseline rate, including the clock source accuracy, dynamic clock switching effects and frequency variations induced by low frequency jitter	--	1400	ppm	See Note 1.
Notes: 1. Measurement shall be performed over the transmitted signal. The signal phase shall be extracted while applying a 2nd order low-pass filter with 3 dB point at 5 MHz. 2. INIT_FREQ_VARIATION corresponds to the transmitter average frequency offset from the Link baseline rate (10.0 Gbps for Gen 2 or 20.0 Gbps for Gen 3), without including low frequency jitter variations, which shall be filtered out by averaging the extracted frequency variation waveform over a window of at least 30 μ s.					

Figure 3-8 shows the transmit frequency variation during training for a Router Assembly. The transmit frequency variation following the clock-switching event shall be measured over time intervals of 200 ns and 1 μ s.

Figure 3-8. Router Assembly Transmitter Frequency Variation During Training

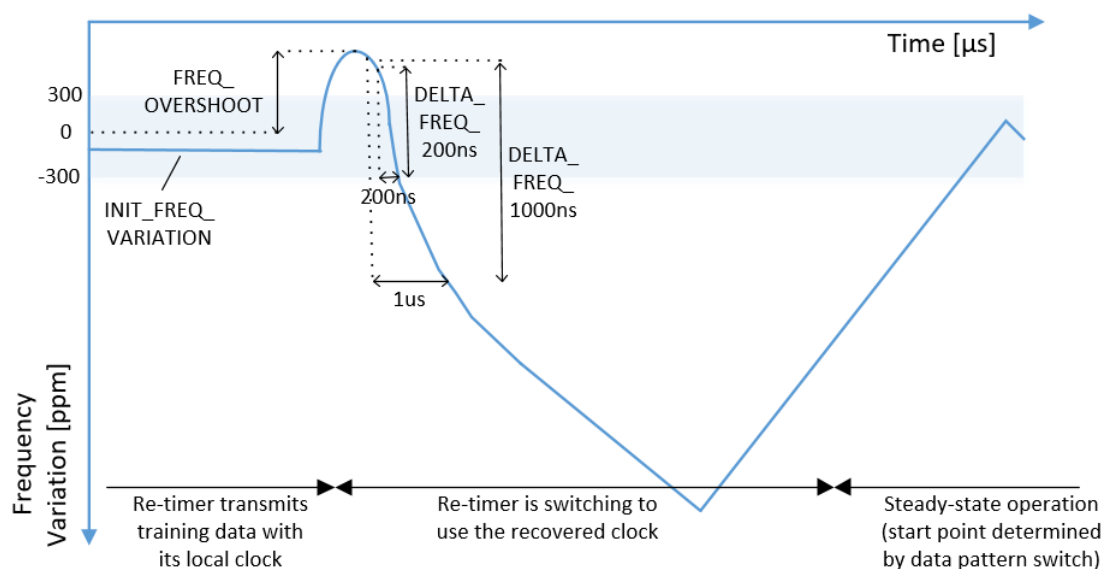
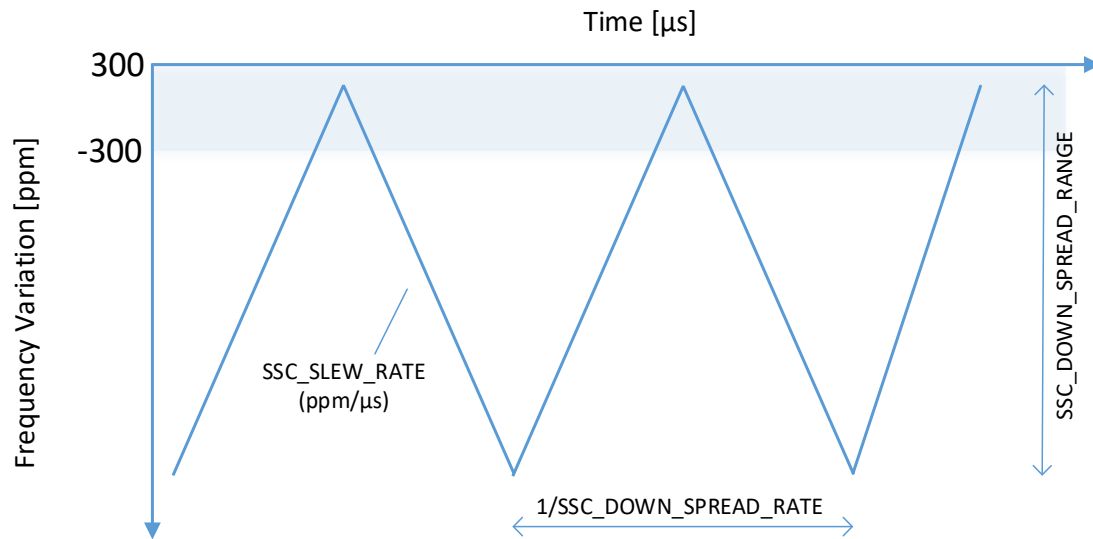
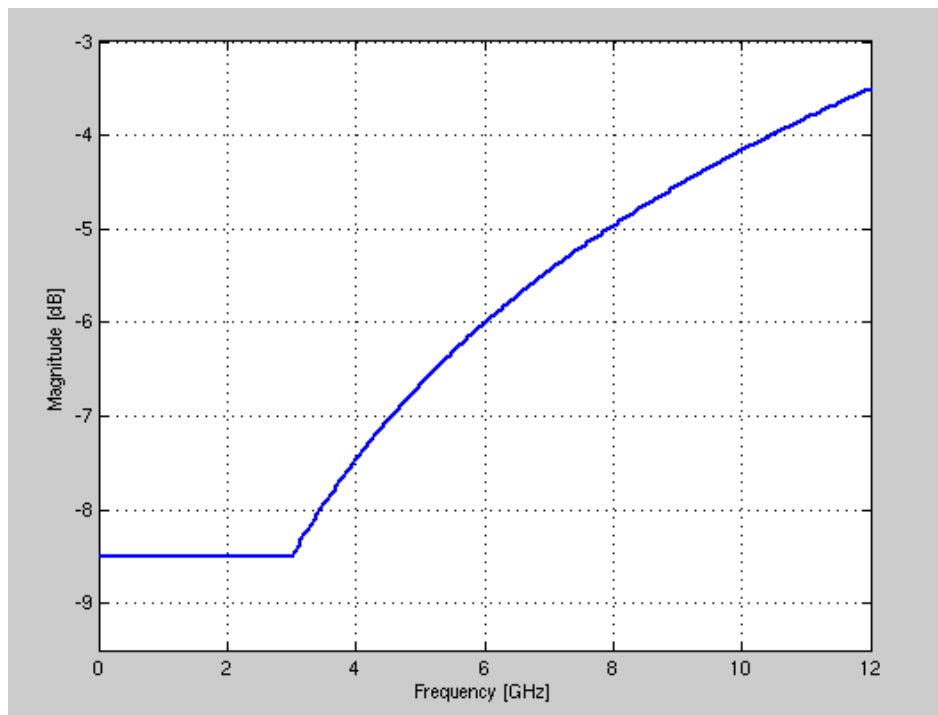


Figure 3-9. Example Transmitter Frequency During Steady-State**3.1.3.1.2 Transmitter Differential Return Loss**

Transmitter differential return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω. When measured at TP2, the differential mode return loss shall not exceed the limits given in the following equation:

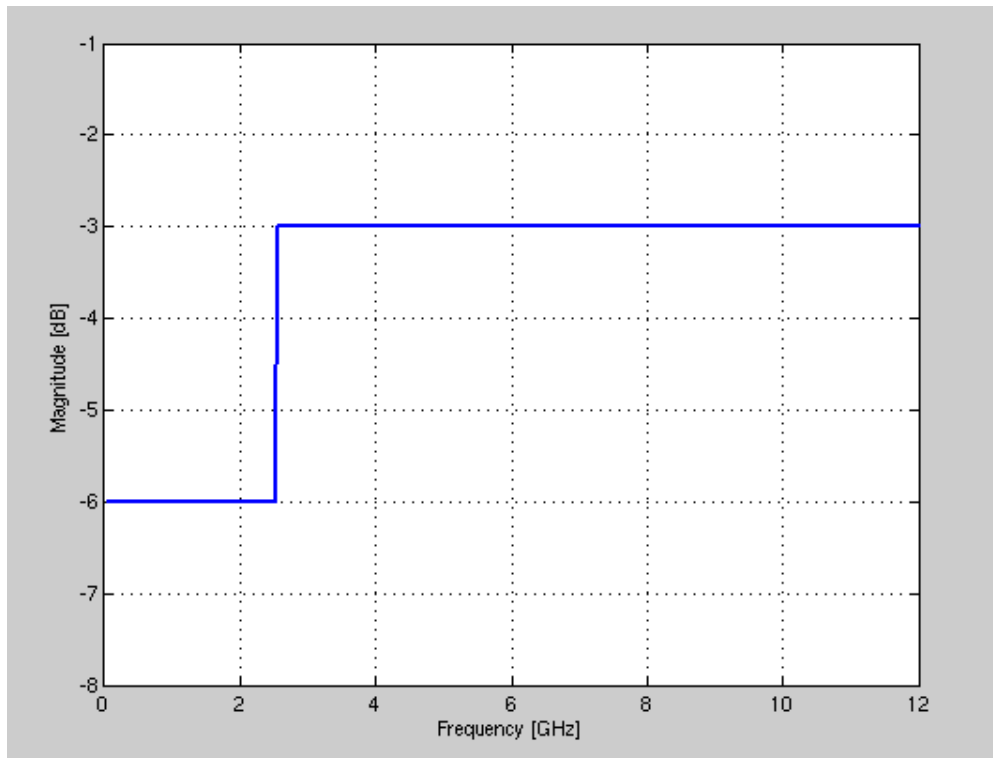
$$\text{SDD22}(f) = \begin{cases} -8.5 & 0.05 < f_{\text{GHz}} \leq 3 \\ -3.5 + 8.3 \cdot \log_{10} \left(\frac{f_{\text{GHz}}}{12} \right) & 3 < f_{\text{GHz}} \leq 12 \end{cases}$$

Figure 3-10. TX Differential Return Loss Mask

3.1.3.1.3 Transmitter Common Mode Return Loss

Transmitter common-mode return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω. When measured at TP2, the common-mode return loss shall not exceed the limits given in the following equation:

$$SCC22(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

Figure 3-11. TX Common-Mode Return Loss Mask**3.1.3.1.4 Transmit Equalization**

A Router Assembly shall support coefficient-based equalization at its transmitter output. The equalizer's structure is based on a 3-tap UI-spaced finite-impulse-response (FIR) filter as shown in Figure 3-12. The transmitted level corresponding to the n th symbol shall be generated as follows:

$$tx_out_n = \sum_{k=-1}^1 data_in_{n-k} \cdot C_k$$

where:

- tx_out_n is the transmitted level at time instant n
- $data_in_{n-k}$ is the data symbol at time instant $n-k$ (may be +1 or -1)
- C_k is the k^{th} coefficient of the FIR filter

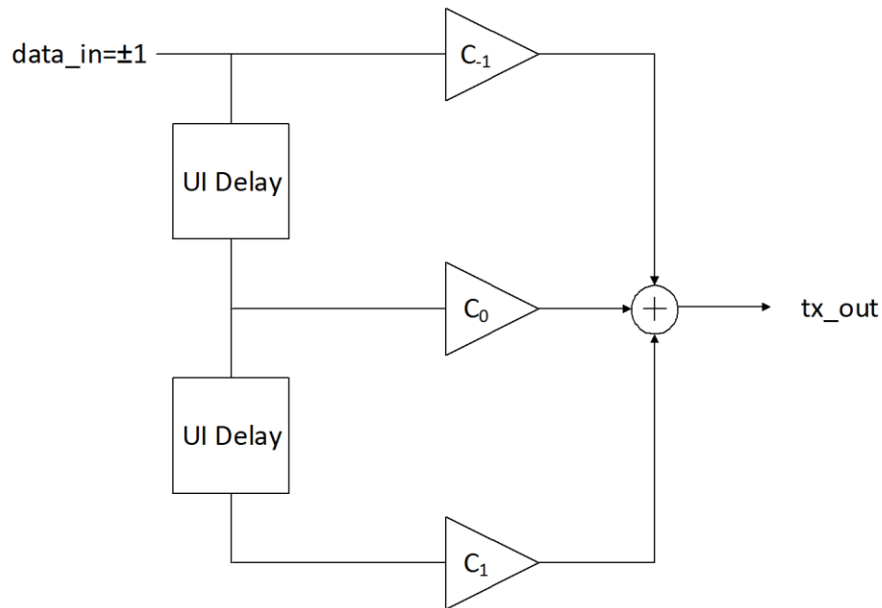
Figure 3-12. Transmitter Equalizer Structure

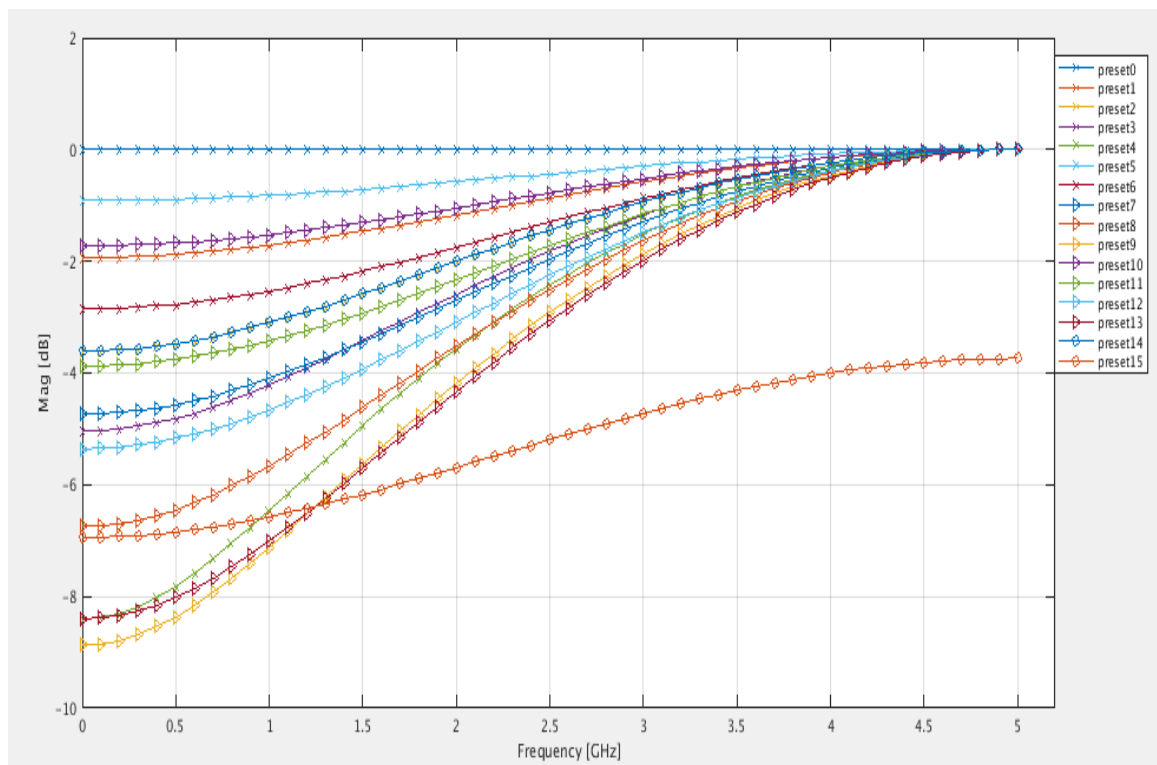
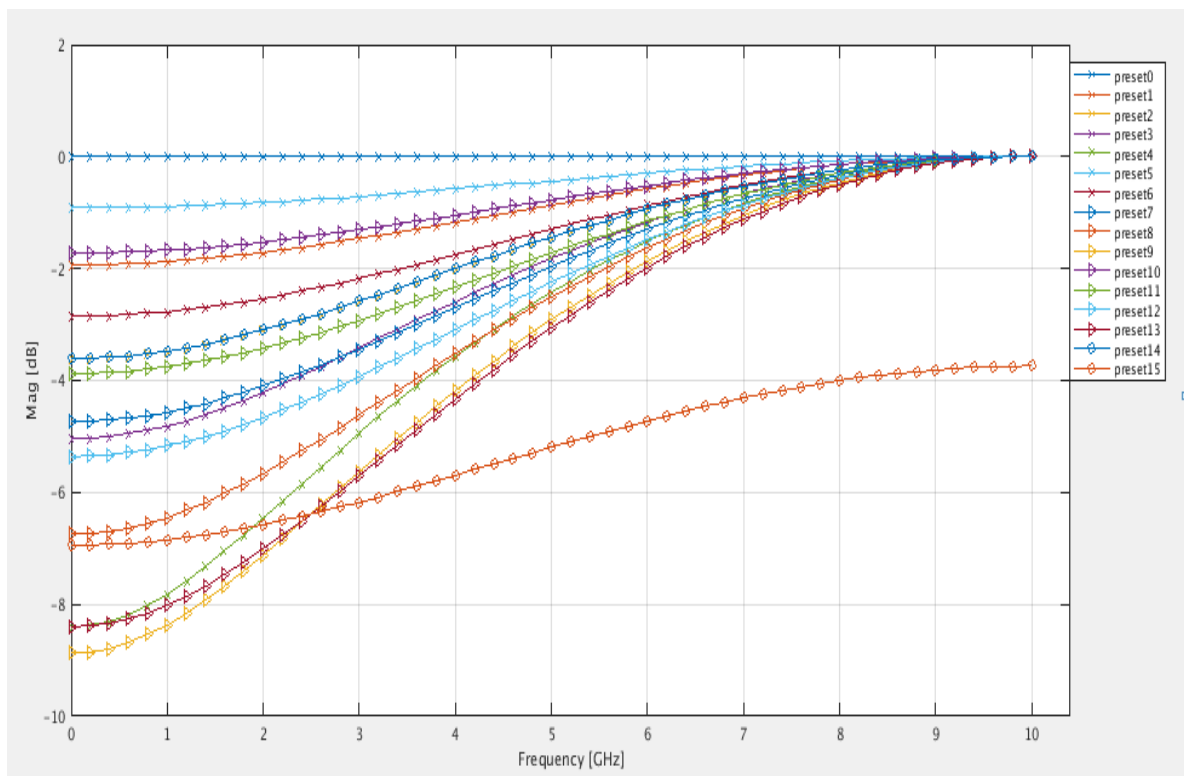
Table 3-4 lists the pre-shoot and de-emphasis transmitter equalization Presets that a transmitter shall support. It also includes the corresponding informative coefficients values provided as a reference. Preset configurations 0-14 represent operation mode with full-swing transmitter output, while configuration 15 represent low swing mode. When configuration 15 is selected, the transmitter's output swing shall be attenuated by 3.5 ± 1 dB compared to its full-swing operation. The required tolerance of the pre-shoot and de-emphasis specifications is ± 1 dB.

For each Preset, the pre-shoot and de-emphasis shall be measured at TP2 using SQ128 pattern (see Table 8-66). The pre-shoot shall be calculated as the ratio of the steady-state voltage obtained when configuring the transmitter equalizer such that the pre-cursor tap's magnitude is moved to the main tap, divided by the steady-state voltage with the standard transmit filter configuration. The de-emphasis shall be calculated as the ratio of the steady-state voltage obtained with the standard filter configuration, divided by the steady-state voltage when configuring the transmitter equalizer such that the post-cursor tap's magnitude is moved to the main tap.

Table 3-4. Transmit Equalization Presets

Preset Number	Pre-shoot [dB]	De-emphasis [dB]	Informative Filter Coefficients		
			C ₋₁	C ₀	C ₁
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.6	0	-0.17	0.83	0
15	1.7	-1.7	-0.05	0.55	-0.05
Notes: 1. The coefficients are normalized such that C ₋₁ + C ₀ + C ₁ corresponds to full output swing. Preset configuration 15 represents operation mode with lower transmitter swing. 2. Preshoot and de-emphasis are calculated as follows: $Preshoot = 20 \cdot \log_{10} \left(\frac{-C_{-1} + C_0 + C_1}{C_{-1} + C_0 + C_1} \right) \quad De - emphasis = 20 \cdot \log_{10} \left(\frac{C_{-1} + C_0 + C_1}{C_{-1} + C_0 - C_1} \right)$					

Figure 3-13 and Figure 3-14 depict the frequency responses of the different transmit equalization Presets for Gen 2 and Gen 3 modes of operation, respectively.

Figure 3-13. Transmitter Equalization Frequency Response for Gen 2 Systems**Figure 3-14. Transmitter Equalization Frequency Response for Gen 3 Systems**

3.1.3.2 Transmitter Compliance Specifications for Gen 2

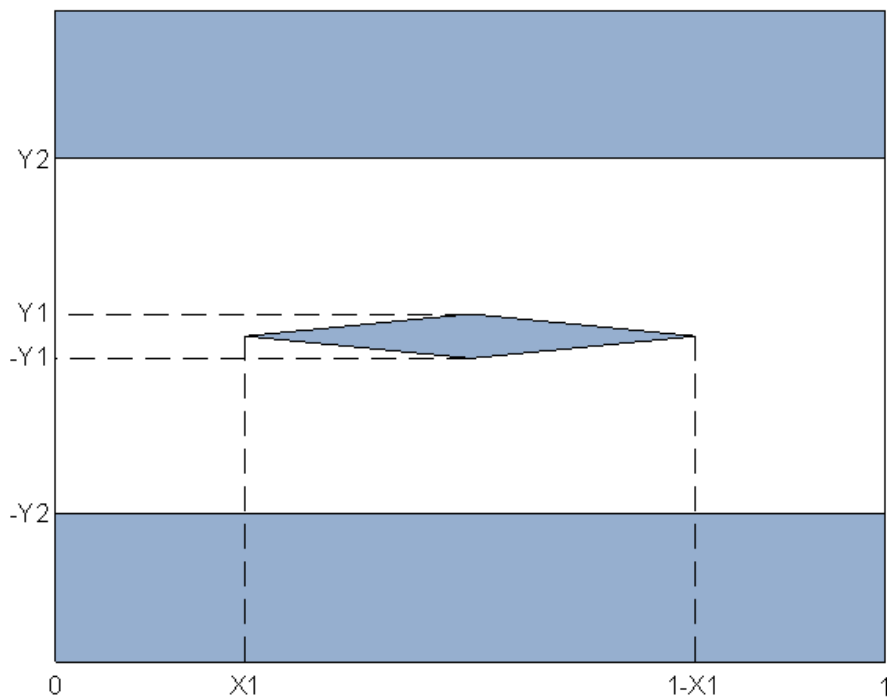
A transmitter operating in Gen 2 mode shall meet the specifications in Table 3-2, Table 3-5, and Table 3-6.

Table 3-5. Gen 2 Transmitter Specifications at TP2

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	99.97	100.03	ps	The minimum UI value corresponds to the Link baseline speed of 10.0 Gbps with an uncertainty range of -300 ppm to 300 ppm. See Note 4.
AC_CM	TX AC Common Mode voltage	--	100	mV pp	
TJ	Total Jitter	--	0.38	UI pp	See Note 2 and Note 3.
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	--	0.31	UI pp	See Note 2.
DDJ	Data-Dependent Jitter	--	0.15	UI pp	See Note 5.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.17	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	--	0.04	UI pp	See Note 6.
DCD	Even-odd jitter associated with Duty-Cycle-Distortion	--	0.03	UI pp	
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	140	--	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	--	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Notes: 1. TX voltage is differential. 2. Measured while applying the reference CDR described in Section 3.1.2.3. Note that the measured jitter includes residual SSC jitter passing the reference CDR. 3. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top). 4. UI shall be calculated dynamically using a uniform moving average filter with window size of 3000 symbols. 5. The transmit equalization shall be set such that the data dependent jitter is minimized. 6. UDJ_LF is the uncorrelated deterministic jitter measured after applying a 2 nd order Low-Pass-Filter with 3 dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR function described in Section 3.1.2.3.					

Table 3-6. Gen 2 Transmitter Specifications at TP3

Symbol	Description	Min	Max	Units	Comments
TJ	Total Jitter	--	0.60	UI pp	See Note 2, Note 3.
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	--	0.31	UI pp	Note 2.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.17	UI pp	
X1	TX eye horizontal deviation	--	0.23	UI	Measured for 1E6 UI. See Note 2, Note 4, and Figure 3-15.
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	53	--	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	--	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Notes: 1. TX voltage is differential. 2. Measured while applying the reference CDR described in Section 3.1.2.3 and the reference equalizer defined in Section 3.1.2.4. Note that the measured jitter includes residual SSC jitter passing the reference CDR. 3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top). 4. X1 specification is informative but shall be assumed as a valid reference if direct TJ measurement cannot be reliably performed.					

Figure 3-15. TX Mask Notations

3.1.3.3 Transmitter Compliance Specifications for Gen 3 Interconnects

A transmitter operating in Gen 3 mode shall meet the specifications in Table 3-2, Table 3-7, and Table 3-8.

Table 3-7. Gen 3 Transmitter Specifications at TP2

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	49.985	50.015	ps	The minimum UI value corresponds to the Link baseline speed of 20.0 Gbps with an uncertainty range of -300 ppm to 300 ppm. See Note 4.
AC_CM	TX AC Common Mode voltage	--	100	mV pp	
TJ	Total Jitter	--	0.46	UI pp	See Note 2, Note 3.
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	--	0.31	UI pp	See Note 2.
DDJ	Data-Dependent Jitter	--	0.21	UI pp	See Note 5.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.17	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	--	0.07	UI pp	See Note 6.
DCD	Even-odd jitter associated with Duty-Cycle-Distortion	--	0.03	UI pp	
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	120	--	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	--	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Notes: 1. TX voltage is differential. 2. Measured while applying the reference CDR described in Section 3.1.2.3. Note that the measured jitter includes residual SSC jitter passing the reference CDR. 3. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top). 4. UI shall be calculated dynamically using a uniform moving average filter with window size of 6000 symbols. 5. The transmit equalization shall be set such that the data dependent jitter is minimized. 6. UDJ_LF is the uncorrelated deterministic jitter measured after applying a 2 nd order Low-Pass-Filter with 3 dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR function described in Section 3.1.2.3.					

Table 3-8. Gen 3 Transmitter Specifications at TP3

Symbol	Description	Min	Max	Units	Comments
TJ	Total Jitter	--	0.60	UI pp	See Note 2, Note 3.
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	--	0.31	UI pp	Note 2.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.17	UI pp	
X1	TX eye horizontal deviation	--	0.23	UI	Measured for 1E6 UI. See Note 2, Note 4, and Figure 3-15.
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	49	--	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	--	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Notes: 1. TX voltage is differential. 2. Measured while applying the reference CDR described in Section 3.1.2.3 and the reference equalizer defined in Section 3.1.2.4. Note that the measured jitter includes residual SSC jitter passing the reference CDR. 3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top). 4. X1 specification is informative but shall be assumed as a valid reference if direct TJ measurement cannot be reliably performed.					

3.1.4 Gen 2 and Gen 3 Router Assembly Receiver Compliance**3.1.4.1 Receiver Specifications Applied for All Speeds**

Table 3-9 defines the receiver parameters that shall apply for both Gen 2 and Gen 3 modes of operation.

Table 3-9. Common Receiver Specifications at TP3'

Symbol	Parameters	Min	Max	Units	Comments
RL_DIFF	Differential Return Loss, 0.05 – 12 GHz	--	See Section 3.1.4.1.1	dB	
RL_COMM	Common Mode Return Loss, 0.05 – 12 GHz	--	See Section 3.1.4.1.2	dB	
LANE_TO_LANE_SKEW	Skew between dual incoming signals of the same USB4 Port	--	44	ns	See Note 1.
RX_INIT_FREQ_VARIATION	Initial non-modulated signal frequency applied during training before obtaining steady-state operation	-300	300	ppm	See Notes 2, 3, 4.
RX_DELTA_FREQ_200ns	Incoming signal's frequency variation during Link training over 200 ns measurement windows	--	1400	ppm	See Notes 2, 3.

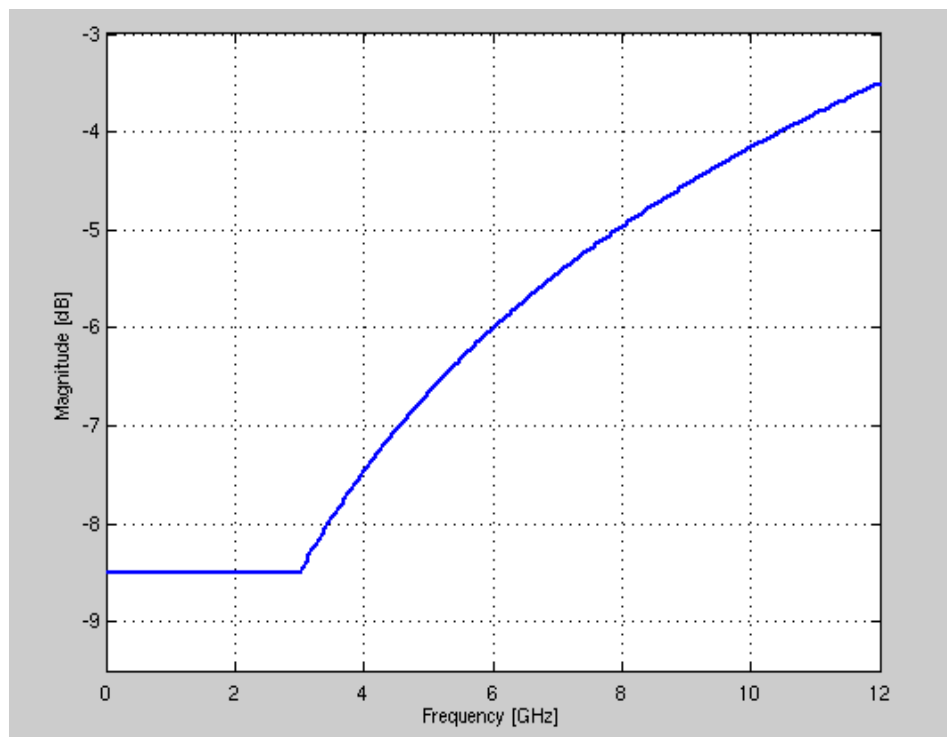
Symbol	Parameters	Min	Max	Units	Comments
RX_DELTA_FREQ_1000ns	Incoming signal's frequency variation during Link training over 1 μ s measurement windows	--	2200	ppm	See Notes 2, 3.
RX_FREQ_OVERSHOOT	Incoming signal's maximum frequency offset from the Link baseline rate during training	--	1600	ppm	See Notes 2, 3.
V_MAX	Peak Voltage	--	650	mV	
Notes: 1. LANE_TO_LANE_SKEW specifies the maximum skew at the connector. On top of the skew measured at TP3', the following informative budget is assumed between the connector and the Router RX IC: <ul style="list-style-type: none"> Each Re-timer input-to-output skew: 8 ns. Physical media mismatches: 2 ns. 2. The clocking configuration during the different stages of the Link initialization is described in Section 3.1.3.1.1 and Figure 3-8. 3. Extracted while applying a 2nd order low-pass filter with 3 dB point at 5 MHz over the signal phase. 4. RX_INIT_FREQ_VARIATION corresponds to the incoming nominal frequency offset from the Link baseline rate (10.0 Gbps for Gen 2 or 20.0 Gbps for Gen 3), without including low frequency jitter induced variations.					

3.1.4.1.1 Receiver Differential Return Loss

Receiver differential return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω . When measured at TP3', the differential mode return loss shall not exceed the limits given in the following equation:

$$SDD11(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log_{10}\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

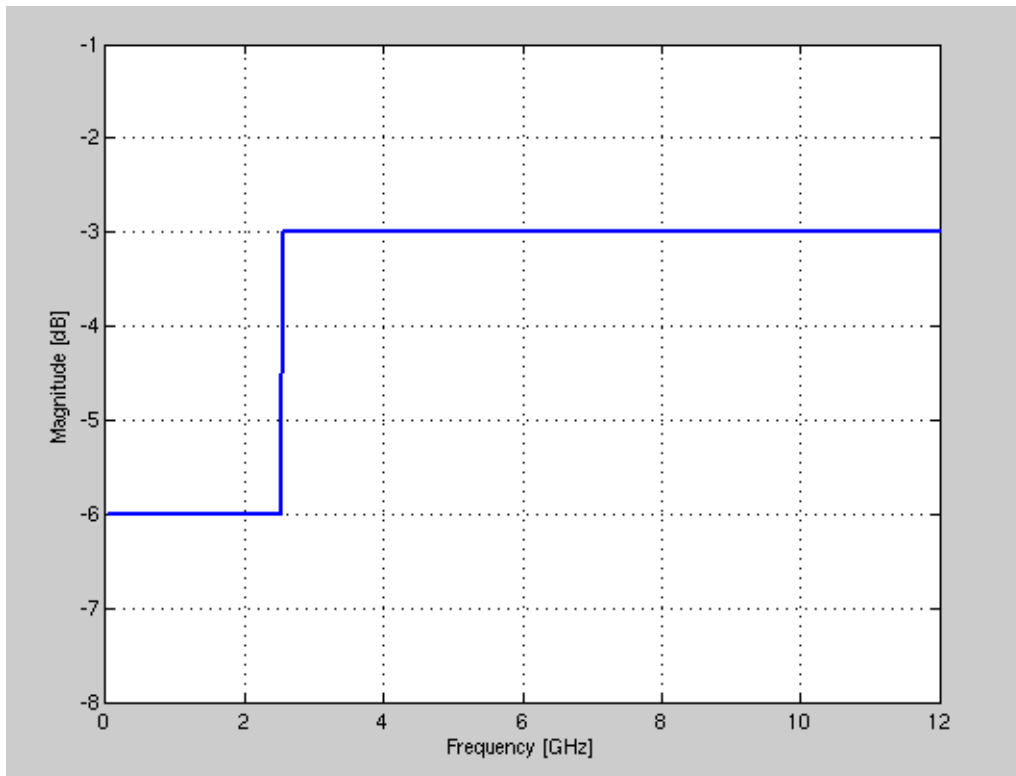
Figure 3-16. RX Differential Return-Loss Mask



3.1.4.1.2 Receiver Common Mode Return Loss

Receiver common-mode return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω. When measured at TP3', the common-mode return loss shall not exceed the limits given in the following equation:

$$SCC11(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

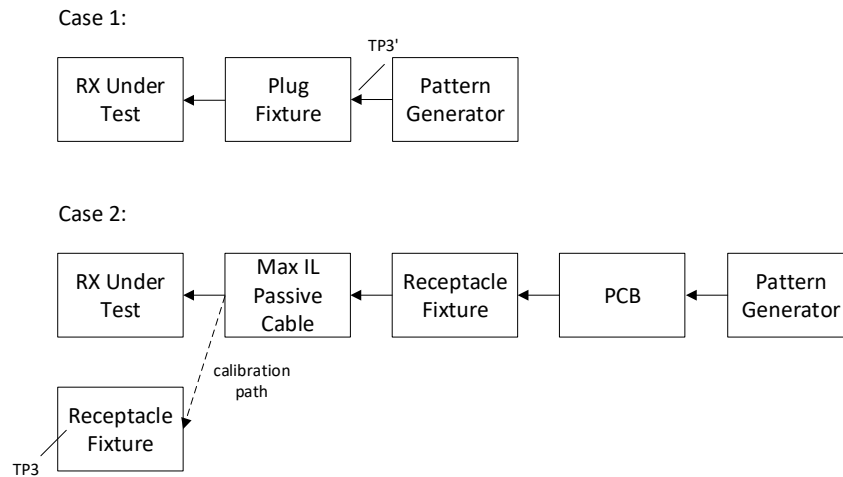
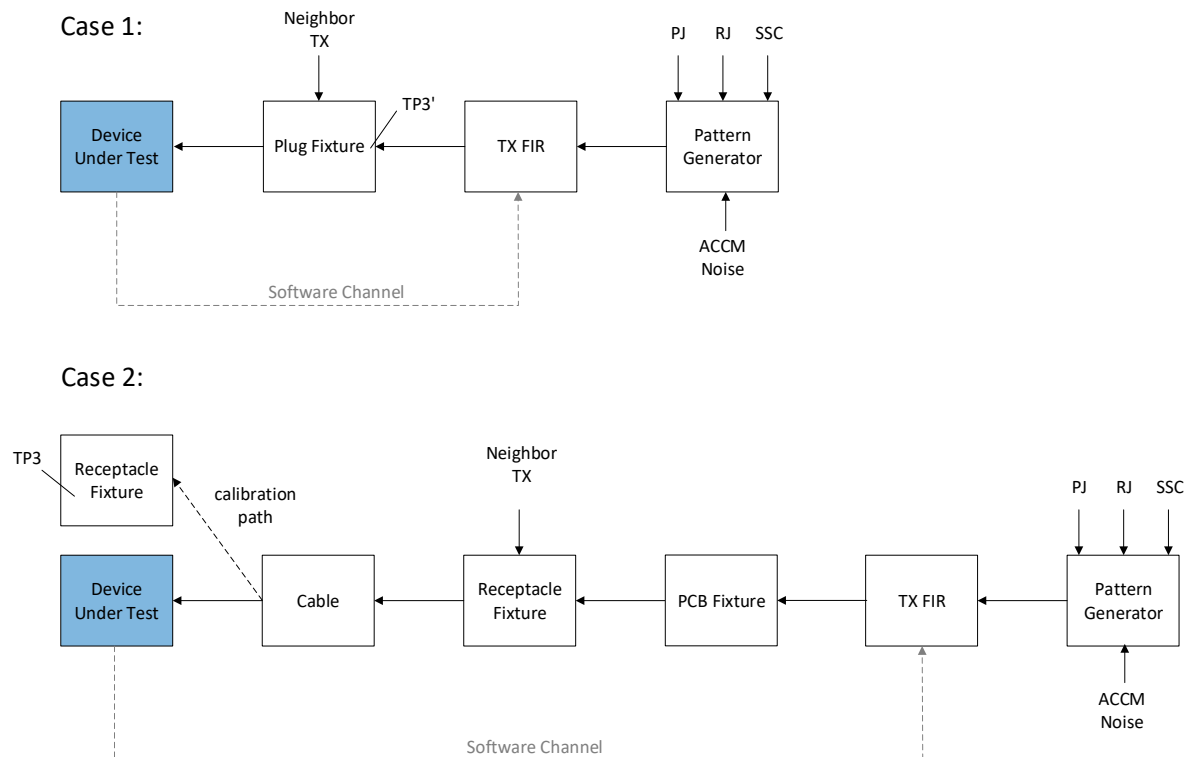
Figure 3-17. RX Common Mode Return-Loss Mask**3.1.4.2 Receiver Uncoded BER Tolerance Testing**

A receiver shall operate at BER of 1E-12 or lower with neither Forward Error Correction nor Pre-Coding applied when a stressed signal is driven at its input. Tolerance testing shall be performed with down-spreading of the clock enabled and while all USB4 Ports are active.

There are two test setups for evaluating the receiver tolerance:

- “Case 1”, which addresses installations with low Insertion-Loss.
- “Case 2”, which addresses installations with maximum Insertion-Loss. For this setup, the following end-to-end insertion loss from the pattern-generator output to TP3 calibration point is assumed:
 - Gen 2: 18 dB at 5 GHz (including 2m USB-C™ passive cable as part of the setup).
 - Gen 3: 16 dB at 10 GHz (including 0.8m USB-C passive cable as part of the setup).

Figure 3-18, Figure 3-19, Table 3-10 and Table 3-11 describe the test topologies and setups for Case 1 and Case 2.

Figure 3-18. Receiver Tolerance Test Topologies**Figure 3-19. Receiver Tolerance Test Setups****Table 3-10. Stressed Signal for Gen 2 Receiver Compliance Testing**

Test Case	Inner Eye Voltage [mV peak]	Random Jitter (RJ) [UI peak-to-peak]	Periodic Jitter [UI peak-to-peak]	Total Jitter [UI peak-to-peak]
1 (at TP3')	350	0.14	0.17	0.35
2 (at TP3)	53	0.14	0.17	0.60

Notes:

1. The Total jitter and Random jitter shall be referenced to 1E-12 statistics. The Inner Eye Voltage shall be measured over 1E6 UI.

Table 3-11. Stressed Signal for Gen 3 Receiver Compliance Testing

Test Case	Inner Eye Voltage [mV peak]	Random Jitter (RJ) [UI peak-to-peak]	Periodic Jitter [UI peak-to-peak]	Total Jitter [UI peak-to-peak]
1 (at TP3')	350	0.14	0.17	0.38
2 (at TP3)	49	0.14	0.17	0.60

Notes:

1. The Total jitter and Random jitter shall be referenced to 1E-12 statistics. The Inner Eye Voltage shall be measured over 1E6 UI.

A receiver shall be tested by injecting several different periodic jitter components, one at a time. The testing shall include sinusoidal jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. In all cases, the incoming signal shall include SSC modulation on top of the sinusoidal jitter component at the range of 5600ppm. PRBS31 pattern shall be used for receiver compliance testing, however, calibration of the stressed signal source may be performed with a periodic pattern shorter than PRBS31. AC common-mode noise shall be added at the pattern-generator output to ensure worst-case transmitter characteristics. The total common-mode noise shall be 100 mV peak-to-peak at the pattern-generator output, while the added noise profile shall be sine-wave at a frequency not smaller than 400 MHz. The periodic jitter, random jitter and the common-mode noise values shall be calibrated for Case 1 setup at TP3'. Case 2 shall follow with the same pattern-generator settings for these components.

All specified jitter values shall be calibrated while applying the reference CDR defined in Section 3.1.2.3. The parameters specified at TP3 shall be calibrated after applying the reference equalizer defined in Section 3.1.2.4.

A receiver may configure its Link Partner's TX equalizer during the USB4 Link establishment. The pattern generator shall support tunable 3-tap FIR at its output, which may be adjusted during the test by the receiver under test through out-of-band software channel. Case 1 shall be calibrated first and Case 2 shall follow with the same TX FIR configuration as an initial setting.

3.1.4.3 Receiver Multi Error-Bursts Testing

When a receiver employs DFE with more than one tap, it shall take steps to limit the probability that a burst of errors is restarted right after it ends with the reception of one or more correct bits (see Section 3.1.1.2). The probability of Error-Burst Restart Events should not exceed 5-E7 (less than one restart event per 2 million bursts on average). The combination of an uncoded BER of 1E-12 and an Error-Burst Restart probability 5E-7 supports an uncoded BER of 1E-19. In cases where the actual uncoded BER is less than 1E-12 at a certain ratio, the Error-Burst Restart probability can be larger than 5E-7 at this same ratio, since the coded BER depends on the product of the two terms.

It is recommended that the receiver multi error-bursts probability shall be characterized using the compliance post-processing tool (Informative) as follows:

- Definitions:

- N is a parameter that defines the observation window for burst restart. It also defines the interval between error bursts. N shall be at least 32 bits.
- An Error Capture is an observation window that starts with the detection of a bit error which is preceded by at least N consecutive bits without errors.

- ~~○ A Burst Restart Event is an Error Capture that contains an error burst of one or more consecutive errors followed by one or more correct bits and then by one or more errors within the observation window.~~
- ~~Initialize-Construct~~ the receiver “Case 2” uncoded BER test setup with “Case 2” configuration used for testing the uncoded BER with periodic jitter component of 100 MHz, and run the test as described in (see Section 3.1.4.2). ~~PRBS31 test pattern shall be used and neither Forward Error Correction nor Pre-Coding shall be applied.~~
- ~~Extract the receiver vertical noise CDF function (vertical “bathtub” curve), and the converged values of the receiver DFE taps and evaluate the error burst-restart probability and the estimated coded BER using a compliance post-processing tool. Background and information on the compliance post-processing tool may be found at: <https://groups.usb.org/wg/usb4electrical/document/folder/1421>.~~
- ~~After initialization, the periodic jitter magnitude shall be increased to the point where uncoded BER of 1E-8 is observed.~~
- ~~The receiver under test shall trigger on random bit errors and capture errors that follow. This shall be done using the method described above for Error Captures. At least N consecutive bits shall be examined for errors starting from the initial trigger.~~
- ~~The probability for obtaining Burst Restart Events shall not exceed 5E-7 (i.e. one error burst restart per 2 million error captures on average).~~
- ~~Error Captures and Burst Restart Events shall be counted and reported out as detailed in Section 8.3.2.2.3 and Section 8.3.2.2.4. The Burst Restart Count shall not increment more than once in an Error Capture.~~

~~The following pseudocode example describes how to update the Error Capture Count and the Burst Restart Count:~~

~~Start: Wait for N consecutive bits without errors~~

~~Wait for a bit with error~~

~~Start an observation window of N bits~~

~~Increment Error Capture Count by 1~~

~~If a transition from a bit without errors to a bit with error is detected within the observation window, increment Burst Restart Count by 1~~

~~Wait for end of observation window~~

~~Go to Start~~

~~The following is an example Error Capture (N=32):~~

~~No burst restart (Error Capture Count shall be incremented by 1, Burst Restart Count shall not change):~~_____

~~captured_data[31:0]=0000000000000000000000001111111111~~

~~Burst restart (Error Capture Count shall be incremented by 1, Burst Restart Count shall be incremented by 1):~~_____

~~captured_data[31:0]=000000000000000000000000111001111111~~

~~where '1' represents a bit error and '0' represents a correct bit, as expected from "exclusive or" (XOR) operation between the received bits and the synchronized reference PRBS31 pattern. captured_data[0] corresponds to the initial error event trigger.~~

Note: A burst of errors contains one or more consecutive bit errors.

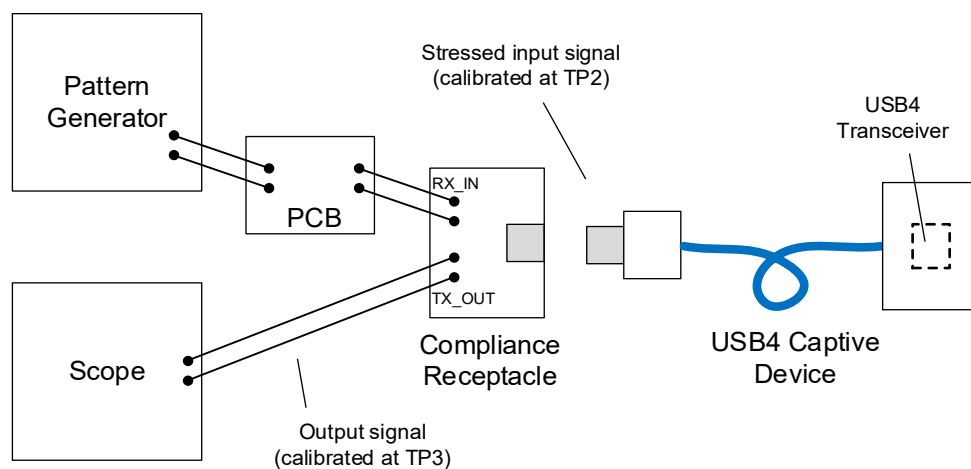
3.1.5 Gen 2 and Gen 3 Captive Device Compliance

A Captive Device is a Router Assembly. However, because a Captive Device has a cable permanently attached, it requires some adjustments in how compliance testing is performed.

3.1.5.1 Captive Device Compliance Test Setup

The compliance test requires connecting a Compliance Receptacle to the Captive Device's connector, as illustrated in Figure 3-20. Details of the Compliance Receptacle can be found in Section 3.1.2.6.2.

Figure 3-20. Captive Device Compliance Test Setup



3.1.5.2 Captive Device Transmitter Specifications

Transmitter compliance testing for a Captive Device is defined at the output of a Compliance Receptacle fixture referenced to TP3.

Unless otherwise specified, a Captive Device's Transmitter shall transmit PRBS31 pattern throughout the compliance testing. Compliance testing shall be performed with Spread-Spectrum-Clocking (SSC) enabled, and while the neighbor interfaces are all active.

3.1.5.2.1 Conducted Energy in Wireless Bands

In order to avoid interference to wireless systems, a Captive Device shall conform to the limits on conducted energy of the USB4 differential pair exiting the device as set forth in Table 3-12. The limits are specified both in the differential and the common mode domains.

Table 3-12. Wireless Band Conducted Limits (at TP3)

Symbol	Description	Max	Units	Comments
PWR_diff_1-14	Differential Power in each of the Wi-Fi bands 1-14, which are centered around the following frequencies (in MHz): 2412, 2417, 2422, 2427, 2432, 2437, 2442, 2447, 2452, 2457, 2462, 2467, 2472, 2484	-17	dBm	Measured in 18 MHz window around the center frequency

Symbol	Description	Max	Units	Comments
PWR_comm_1-14	Common mode Power in each of the Wi-Fi bands 1-14, which are centered around the following frequencies (in MHz): 2412, 2417, 2422, 2427, 2432, 2437, 2442, 2447, 2452, 2457, 2462, 2467, 2472, 2484	-47	dBm	Measured in 18 MHz window around the center frequency
PWR_diff_36-64	Differential Power in each of the Wi-Fi bands 36-64, which are centered around the following frequencies (in MHz): 5180, 5190, 5200, 5210, 5220, 5230, 5240, 5260, 5280, 5300, 5320	-22	dBm	Measured in 18 MHz window around the center frequency
PWR_comm_36-64	Common mode Power in each of the Wi-Fi bands 36-64, which are centered around the following frequencies (in MHz): 5180, 5190, 5200, 5210, 5220, 5230, 5240, 5260, 5280, 5300, 5320	-43	dBm	Measured in 18 MHz window around the center frequency
PWR_diff_100-140	Differential Power in each of the Wi-Fi bands 100-140, which are centered around the following frequencies (in MHz): 5500, 5520, 5540, 5560, 5580, 5600, 5620, 5640, 5660, 5680, 5700	-23	dBm	Measured in 18 MHz window around the center frequency
PWR_comm_100-140	Common mode Power in each of the Wi-Fi bands 100-140, which are centered around the following frequencies (in MHz): 5500, 5520, 5540, 5560, 5580, 5600, 5620, 5640, 5660, 5680, 5700	-44	dBm	Measured in 18 MHz window around the center frequency.
PWR_diff_149-165	Differential Power in each of the Wi-Fi bands 149-165, which are centered around the following frequencies (in MHz): 5745, 5765, 5785, 5805, 5825	-23	dBm	Measured in 18 MHz window around the center frequency.
PWR_comm_149-165	Common mode Power in each of the Wi-Fi bands 149-165, which are centered around the following frequencies (in MHz): 5745, 5765, 5785, 5805, 5825	-45	dBm	Measured in 18 MHz window around the center frequency.

3.1.5.2.2 Transmitter Specifications

Table 3-13, Table 3-14, and Table 3-15 define the parameters for Captive Device transmitters operating in Gen 2 and Gen 3 modes.

Table 3-13. Captive Device Transmitter Specifications at TP3 for Gen 2 and Gen 3

Symbol	Description	Min	Max	Units	Comments
RL_DIFF	Differential Return Loss, 0.05-12 GHz	--	See Section 3.1.5.2.3	dB	
RL_COMM	Common Mode Return Loss, 0.05-12 GHz	--	See Section 3.1.5.2.4	dB	
TX_EQ	Transmitter Equalization Settings	--	See Section 3.1.3.1.3	--	
SSC_DOWN_SPREAD_RANGE	Dynamic range of SSC down-spreading during steady-state	0.4	0.5	%	See Note 3, Note 4, and Figure 3-9.
SSC_DOWN_SPREAD_RATE	SSC down-spreading modulation rate during steady-state	30	33	KHz	See Note 4 and Figure 3-9.
SSC_PHASE_DEVIATION	Phase jitter associated with the SSC modulation during steady-state	2.5	22	ns pp	See Note 1, Note 4 and Figure 3-9.

Symbol	Description	Min	Max	Units	Comments
SSC_SLEW_RATE	SSC frequency slew rate (df/dt) during steady state	--	1250	ppm/μs	See Note 2, Note 4 and Figure 3-9.
TX_FREQ_VARIATIONS_TRAINING	TX frequency variations during Link training, before obtaining steady-state	--	See Section 3.1.3.1.1	ppm	See Note 4.
LANE_TO_LANE_SKEW	Skew between dual transmit signals of the same USB4 Port	--	44	ns	See Note 5.
RISE_FALL_TIME	TX rise/fall time measured between 20-80% levels	10	--	ps	Test pattern shall be SQ128 (see Table 8-66).
AC_CM	Output AC Common Mode Voltage	--	200	mV pp	
V_ELEC_IDLE	Peak voltage during transmit electrical idle (one-sided voltage opening of the differential signal)	--	20	mV	See Note 6.
V_TX_DC_AC_CONN	Instantaneous DC+AC voltages at the connector side of the AC coupling capacitors	-0.5 (min1) -0.3 (min2)	1.0	V	See Note 7.

Notes:

1. The SSC phase deviation shall be extracted from the transmitted signal. During this test, the transmitter shall be configured to send PRBS31 pattern. The SSC phase deviation shall be extracted from the signal phase after applying a 2nd order low-pass filter with 3 dB point at 5 MHz.
2. The SSC slew rate shall be extracted from the transmitted signal over measurement intervals of 0.5 μs. The SSC phase slew-rate shall be extracted from the signal phase after applying a 2nd order low-pass filter with 3 dB point at 5 MHz.
3. SSC_DOWN_SPREAD_RANGE specifies the required SSC modulation depth, represented by the difference of the maximum and minimum modulated frequencies, referenced to the Link speed.
4. Steady-state clocking is applied from the point that SLOS training pattern is sent by the transmitter.
5. Total Lane-to-Lane skew measured at TP3 including the skew introduced by the physical media, by the Router IC TX, and by up to 4 Re-timers placed on the board and inside the cable plugs. Informative Lane-to-Lane skew budget: Router IC TX pins: 8 ns, each Re-timer input-to-output: 8 ns, physical media mismatches: 4 ns.
6. V_ELEC_IDLE shall be extracted after applying first order low-pass filter with 3 dB point at 1.25 GHz.
7. The absolute single-ended voltage seen by the receiver. This requirement applies to all Link states, and during power-on and power-off. (min1, max) is measured with a 200 KΩ receiver load, and (min2, max) is measured with a 50 Ω receiver load. The ground offset between a DFP and UFP does not contribute to V_TX_DC_AC_CONN.

Table 3-14. Captive Device Transmitter Specifications at TP3 for Gen 2 Systems

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	99.97	100.03	ps	The minimum UI value corresponds to the Link baseline speed of 10.0 Gbps with an uncertainty range of -300 ppm to 300 ppm. See Note 5.
TJ	Total Jitter	--	0.60	UI pp	See Note 2, Note 3.
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	--	0.31	UI pp	See Note 2.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.17	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	--	0.04	UI pp	See Note 6.
DCD	Even-odd jitter associated with Duty-Cycle-Distortion	--	0.03	UI pp	
X1	TX eye horizontal deviation	--	0.23	UI	Measured for 1E6 UI. See Note 2, Note 4, and Figure 3-15.
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	53	--	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	--	650	mV	See Note 1, Note 2, and Figure 3-15.
Notes: 1. TX voltage is differential. 2. Measured while applying the reference CDR described in Section 3.1.2.3 and the reference equalizer defined in Section 3.1.2.4. Note that the measured jitter includes residual SSC jitter passing the reference CDR. 3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top). 4. X1 specification is informative but shall be assumed as a valid reference if direct TJ measurement cannot be reliably performed. 5. UI shall be calculated dynamically using a uniform moving average filter with window size of 3000 symbols. 6. UDJ_LF is the uncorrelated deterministic jitter measured after applying a 2 nd order Low-Pass-Filter with 3 dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR function described in Section 3.1.2.3.					

Table 3-15. Captive Device Transmitter Specifications at TP3 for Gen 3 Systems

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	49.985	50.015	ps	The minimum UI value corresponds to the Link baseline speed of 20.0 Gbps with an uncertainty range of -300 ppm to 300 ppm. See Note 5.
TJ	Total Jitter	--	0.60	UI pp	See Note 2, Note 3.
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	--	0.31	UI pp	See Note 2.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.17	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	--	0.07	UI pp	See Note 6.
DCD	Even-odd jitter associated with Duty-Cycle-Distortion	--	0.03	UI pp	
X1	TX eye horizontal deviation	--	0.23	UI	Measured for 1E6 UI. See Note 2, Note 4, and Figure 3-15.
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	49	--	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	--	650	mV	See Note 1, Note 2, and Figure 3-15.
Notes: 1. TX voltage is differential. 2. Measured while applying the reference CDR described in Section 3.1.2.3 and the reference equalizer defined in Section 3.1.2.4. Note that the measured jitter includes residual SSC jitter passing the reference CDR. 3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top). 4. X1 specification is informative but shall be assumed as a valid reference if direct TJ measurement cannot be reliably performed. 5. UI shall be calculated dynamically using a uniform moving average filter with window size of 6000 symbols. 6. UDJ_LF is the uncorrelated deterministic jitter measured after applying a 2 nd order Low-Pass-Filter with 3 dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR function described in Section 3.1.2.3.					

3.1.5.2.3 Transmitter Differential Return Loss

Transmitter differential return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω. When measured at TP3, the differential mode return loss shall not exceed the limits given in the following equation:

$$SDD22(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log_{10} \left(\frac{f_{GHz}}{12} \right) & 3 < f_{GHz} \leq 12 \end{cases} \text{ [dB]}$$

3.1.5.2.4 Transmitter Common Mode Return Loss

Transmitter common-mode return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω. When measured at TP3, the common-mode return loss shall not exceed the limits given in the following equation:

$$SCC22(f) = \begin{cases} -4 & 0.05 < f_{GHz} \leq 2.5 \\ -2 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

3.1.5.2.5 Transmit Equalization

A Captive Device shall implement tunable 3-tap finite-impulse-response (FIR) equalization at its output. The transmit equalization shall support Preset configurations with different de-emphasis and pre-shoot settings as specified in Table 3-4.

3.1.5.3 Captive Device Receiver Specifications**3.1.5.3.1 Receiver Specifications for Gen 2 and Gen 3**

Table 3-16 defines parameters for receivers that shall apply for both Gen 2 and Gen 3 modes of operation.

Table 3-16. Common Receiver Specifications at TP2

Symbol	Description	Min	Max	Units	Comments
RL_DIFF	Differential Return Loss, 0.05-12 GHz	--	See Section 3.1.5.3.2	dB	
RL_COMM	Common Mode Return Loss, 0.05-12 GHz	--	See Section 3.1.5.3.3	dB	
LANE_TO_LANE_SKEW	Skew between dual incoming signals of the same USB4 Port	--	26	ns	See Note 1.
RX_INIT_FREQ_VARIATION	Initial non-modulated signal frequency applied during training before obtaining steady-state operation	-300	300	ppm	See Notes 2, 3, 4.
RX_DELTA_FREQ_200ns	Incoming signal's frequency variation during Link training over 200 ns measurement windows	--	1400	ppm	See Notes 2, 3.
RX_DELTA_FREQ_1000ns	Incoming signal's frequency variation during Link training over 1 μs measurement windows	--	2200	ppm	See Notes 2, 3.

Symbol	Description	Min	Max	Units	Comments
RX_FREQ_OVERSHOOT	Incoming signal's maximum frequency offset from the Link baseline rate during training	--	1400	ppm	See Notes 2, 3.
V_MAX	Peak voltage	--	650	mV	
Notes: 1. LANE_TO_LANE_SKEW specifies the maximum skew at the connector. On top of the skew measured at TP2, the following informative budget is assumed between the connector and the Router RX IC: <ul style="list-style-type: none"> Each Re-timer input-to-output skew: 8 ns. Physical media mismatches: 4 ns. 2. The clocking configuration during the different stages of the Link initialization is described in Section 3.1.3.1.1 and Figure 3-8. 3. Extracted while applying a 2nd order low-pass filter with 3 dB point at 5 MHz over the signal phase. 4. RX_INIT_FREQ_VARIATION corresponds to the incoming nominal frequency offset from the Link baseline rate (10.0 Gbps in Gen 2 or 20.0 Gbps in Gen 3), without including low frequency jitter induced variations.					

3.1.5.3.2 Receiver Differential Return Loss

Receiver differential return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω. When measured at TP2, the differential mode return loss shall not exceed the limits given in the following equation:

$$SDD11(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log_{10}\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases} \text{ [dB]}$$

3.1.5.3.3 Receiver Common Mode Return Loss

Receiver common-mode return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω. When measured at TP2, the common-mode return loss shall not exceed the limits given in the following equation:

$$SCC11(f) = \begin{cases} -4 & 0.05 < f_{GHz} \leq 2.5 \\ -2 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

3.1.5.4 Captive Device Receiver Uncoded BER Tolerance Testing

The ability of a Captive Device Receiver to tolerate the worst-case incoming signal is examined using a stressed receiver test.

A Captive Device shall be able to reliably receive the stressed input signals specified in Table 3-17 and Table 3-18 (referenced to TP2), and operate with Bit-Error-Ratio of 1E-12 or lower, with neither Forward Error Correction nor Pre-Coding applied. A Captive Device receiver shall be tested by injecting several different periodic jitter components, one at a time. The test shall include sinusoidal jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. In all cases, the incoming signal shall include SSC modulation on top of the sinusoidal jitter component at the range of 5600ppm. PRBS31 pattern shall be used for Captive Device compliance testing, however calibration of the stressed signal source may be performed with a periodic pattern shorter than PRBS31. AC common-mode noise shall be added at the pattern-generator output to ensure worst-case transmitter characteristics. The total common-mode noise shall be 100 mV peak-to-peak at TP2, while the added noise profile shall be sine-wave at a frequency not smaller than 400 MHz. All the specified jitter values shall be calibrated while applying the reference CDR defined in Section 3.1.2.3.

A Captive Device receiver may configure its Link Partner's TX equalizer during Lane Initialization. The pattern generator shall support tunable 3-tap FIR at its output, which may be adjusted during the test by the receiver under test through out-of-band software channel.

The Captive Device receiver test setup is described in Figure 3-21.

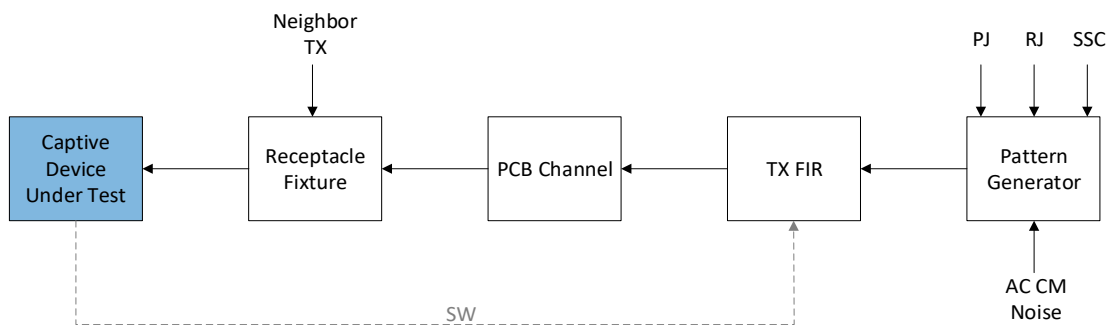
Table 3-17. Stressed Receiver Conditions for Gen 2 Captive Device Compliance Testing (at TP2)

Inner Eye Voltage [mV peak]	Data Dependent Jitter [UI peak-to-peak]	Random Jitter (RJ) [UI peak-to-peak]	Periodic Jitter [UI peak-to-peak]	Total Jitter [UI peak-to-peak]
140	0.10	0.14	0.17	0.41
Notes:				
1. The Total jitter and Random jitter shall be referenced to 1E-12 statistics. The Inner Eye Voltage shall be measured over 1E6 UI.				

Table 3-18. Stressed Receiver Conditions for Gen 3 Captive Device Compliance Testing (at TP2)

Inner Eye Voltage [mV peak]	Data Dependent Jitter [UI peak-to-peak]	Random Jitter (RJ) [UI peak-to-peak]	Periodic Jitter [UI peak-to-peak]	Total Jitter [UI peak-to-peak]
120	0.15	0.14	0.17	0.46
Notes:				
1. The Total jitter and Random jitter shall be referenced to 1E-12 statistics. The Inner Eye Voltage shall be measured over 1E6 UI.				

Figure 3-21. Captive Device Receiver Test Setup



3.1.5.5 Captive Device Receiver Multi Error-Bursts Testing

When a Captive Device's receiver employs DFE with more than one tap, it shall take steps to limit the probability that a burst of errors is restarted right after it ends with the reception of one or more correct bits (see Section 3.1.1.2). The probability of Error-Burst Restart Events should not exceed 5E-7 (less than one restart event per 2 million error burst on average). The combination of an uncoded BER of 1E-12 and an Error-Burst Restart probability of 5E-7 supports and uncoded BER of 1E-19. In cases where the actual uncoded BER is less than 1E-12 at a certain ratio, the Error-Burst probability can be largen than 5E-7at this same ratio, since the coded BER depends on the product of the two terms.

It is recommended that tThe receiver multi error-burst probability ~~shall~~ be characterized using the compliance post-processing tool (Informative)as follows:

- Definitions:

- N is a parameter that defines the observation window for burst restart. It also defines the interval between error bursts. N shall be at least 32 bits.

- ~~○ An Error Capture is an observation window that starts with the detection of a bit error which is preceded by at least N consecutive bits without errors.~~
- ~~○ A Burst Restart Event is an Error Capture that contains an error burst of one or more consecutive errors followed by one or more correct bits and then by one or more errors within the observation window.~~
- ~~● InitializeConstruct the receiver uncoded BER test setup as configured for testing the uncoded BER with periodic jitter component of 100 MHz, and run the test as described in (see Section 3.1.5.4). PRBS31 test pattern shall be used and neither Forward Error Correction nor Pre-Coding shall be applied.~~
- Extract the receiver vertical noise CDF function (vertical “bathtub” curve), and the converged values of the receiver DFE taps and evaluate the error burst-restart probability and the estimated coded BER using a compliance post-processing tool. Background and information on the compliance post-processing tool may be found at: <https://groups.usb.org/wg/usb4electrical/document/folder/1421>.
- ~~● After initialization, the periodic jitter magnitude shall be increased to the point where uncoded BER of 1E-8 is observed.~~
- ~~● The receiver under test shall trigger on random bit errors and capture errors that follow. This shall be done using the method described above for Error Captures. At least N consecutive bits shall be examined for errors starting from the initial trigger.~~
- ~~● The probability for obtaining Burst Restart Events shall not exceed 5E-7 (i.e. one error burst restart per 2 million error captures on average).~~
- ~~● Error capture events and error burst restart events shall be counted and reported out as detailed in Section 8.3.2.2.3 and Section 8.3.2.2.4. The Burst Restart Count shall not increment more than once in an Error Capture.~~

The following pseudo-code example describes how to update the Error Capture Count and the Burst Restart Count:

```

Start: Wait for N consecutive bits without errors

Wait for a bit with error

Start an observation window of N bits

Increment Error Capture Count by 1

If a transition from a bit without errors to a bit with error is detected within the observation window, increment Burst Restart Count by 1

Wait for end of observation window

Go to Start

```

The following is an example analysis:

No burst restart (Error Capture Count shall be incremented by 1, Burst Restart Count shall not change): _____

captured_data[31:0]=0000000000000000000000001111111111

Burst restart (Error Capture Count shall be incremented by 1, Burst Restart Count shall be incremented by 1): _____

~~captured_data[31:0]=000000000000000000000000111001111111~~

~~where '1' represents a bit error and '0' represents a correct bit, as expected from "exclusive or" (XOR) operation between the received bits and the synchronized reference PRBS31 pattern. captured_data[0] corresponds to the initial error event trigger.~~

Note: A burst of errors contains one or more consecutive bit errors.

3.1.6 Gen 2 and Gen 3 Receiver Lane Margining (Testability)

3.1.6.1 Background

All USB4 Ports shall support receiver Lane margining as defined in this section. Receiver Lane margining provides a means to assess end-to-end Link performance, enables the validation of Links that use Re-timers or device-down topologies (i.e. do not have a connector that can be used for compliance testing), and enables a standard method for margining systems in production or in the field. Receiver Lane margining is performed while the Link is Active. This allows derivation of the Link electrical performance that would be experienced by the end user.

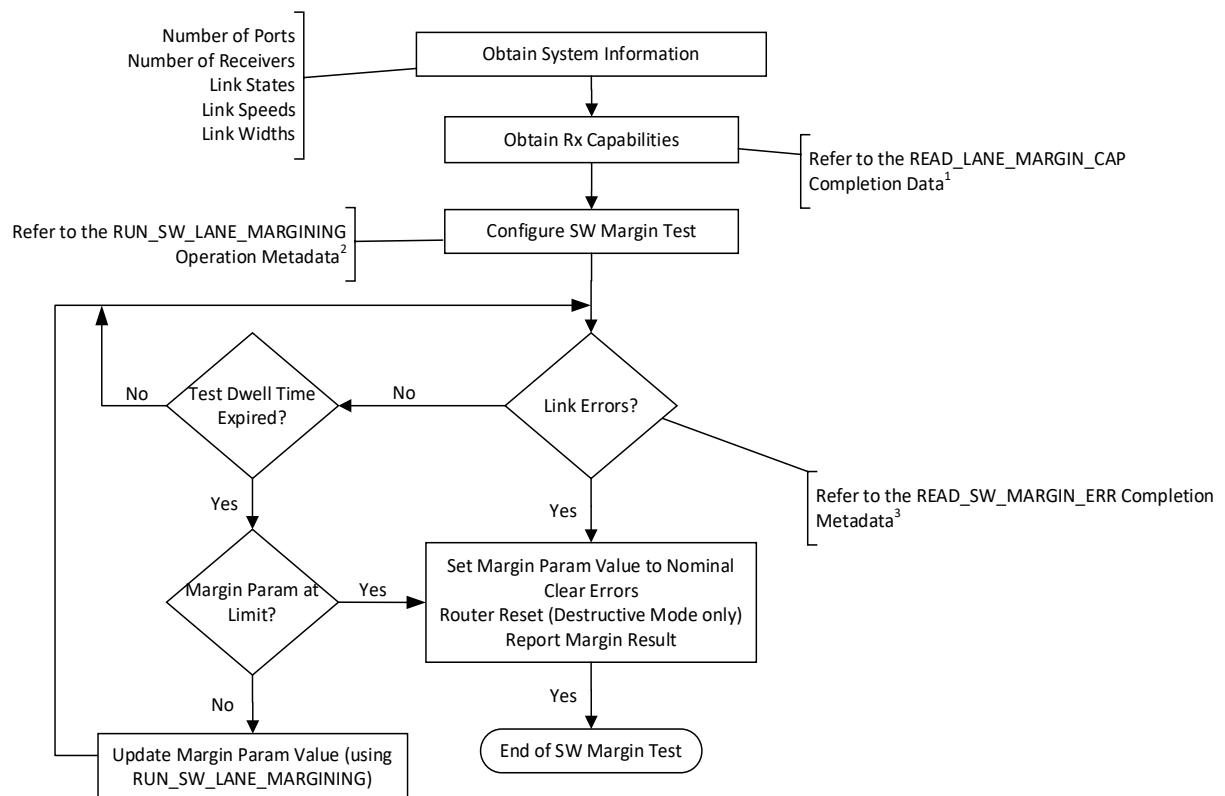
Receiver margin values and error counts described in this section are not designed to determine compliance for any component. Rather, Receiver Lane Margining standardizes methods already in use by many component and system manufacturers to determine a subjective measure of Link robustness.

A USB4 Port shall support either the software (SW) margining mode defined in Section 3.1.6.1.1 or the hardware (HW) margining mode defined in Section 3.1.6.1.2. A USB4 Port may optionally support both SW and HW margining modes.

Section 8.3.2.4 defines the Operations that are used to obtain receiver margining capabilities, configure margining parameters, run a margining test, and get margining results.

3.1.6.1.1 Software Margining Mode

The SW margining mode enables application software executing on the system under test to obtain the margin information using a test flow that is implemented in software. In this mode, software can perform sequential Operations of RUN_SW_LANE_MARGINING and READ_SW_MARGIN_ERR to implement the margining flow. A receiver that supports the SW mode and time margining shall be able to support a voltage and time offset concurrently, such that the voltage margin at each time offset can be obtained. A simplified example of a SW margining flow is depicted in Figure 3-22.

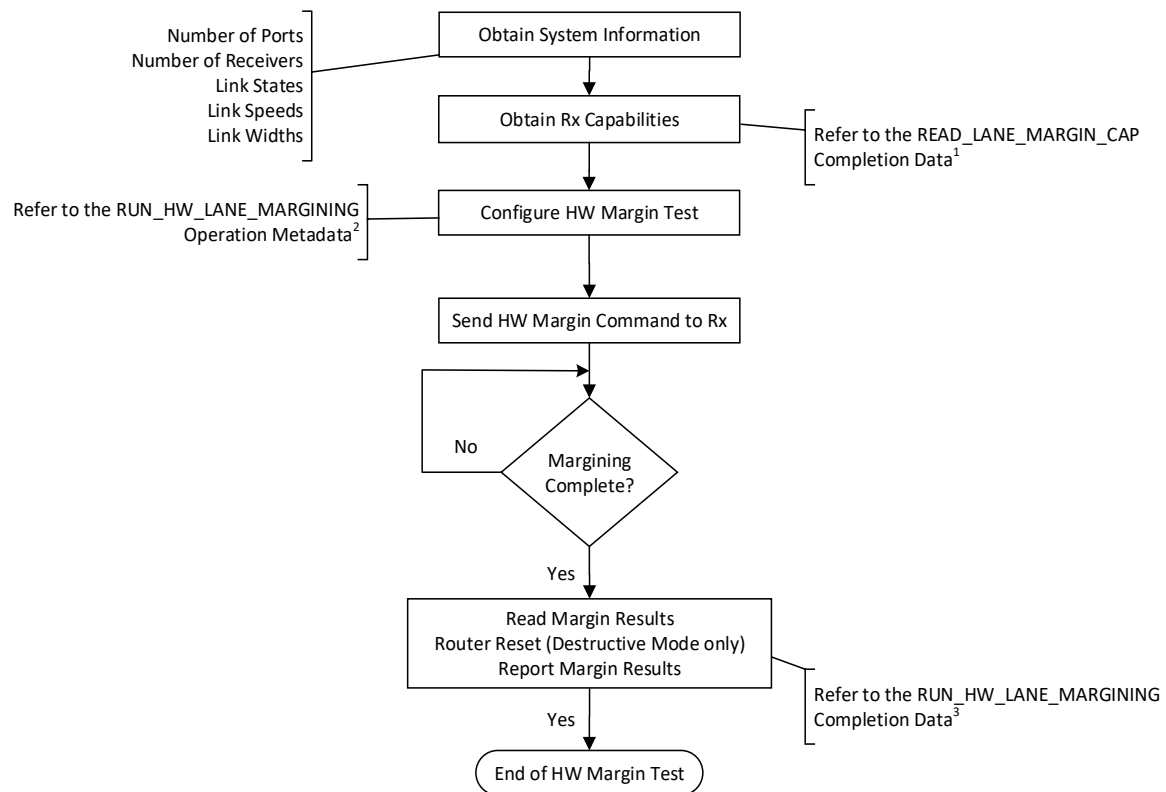
Figure 3-22. Software Margining Mode Example¹ See Table 8-82 for READ_LANE_MARGIN_CAP Completion Data² See Table 8-86 for RUN_SW_LANE_MARGINING Operation Metadata³ See Table 8-88 for READ_SW_MARGIN_ERR Completion Metadata

A Router shall implement a 4-bit error counter for each Lane when performing a non-destructive margining test in SW mode. A bit error counter shall increment when it detects a bit error on its Lane and shall stop when it reaches its maximum value. A Router shall allow system software to reset the bit error counters at any time.

A Router does not need to implement bit error counters if it only supports HW margining mode.

3.1.6.1.2 Hardware Margining Mode

HW margining mode implements the margin test flow in hardware or firmware. Application software executing on the system under test configures the test parameters and initiates a margining test by writing to configuration and command registers. The implementation of the margining flow is performed by hardware or firmware and software obtains the margin results through the reading of status and result registers. This flow is depicted in Figure 3-23.

Figure 3-23. Hardware Margining Flow¹ See Table 8-82 for READ_LANE_MARGIN_CAP Completion Data² See Table 8-83 for RUN_HW_LANE_MARGINING Operation Metadata³ See Table 8-85 for RUN_HW_LANE_MARGINING Completion Metadata

3.1.6.2 Receiver Voltage Margining and Timing Margining Requirements

All receivers shall support voltage margining whereby a receiver sampler is offset from the nominal sampling position in the voltage (vertical) dimension. Independent voltage margining in the positive (high) and negative (low) directions is optional but recommended. A USB4 Port shall be capable of performing voltage margining for each Lane independently. Voltage margining shall be non-destructive (i.e. not introduce actual bit errors on the Link). Voltage margining can be implemented using a monitor sampler that is offset from the nominal sample position while the data sampler remains at the nominal position. A receiver shall use the range and step size in Table 3-19 for voltage margining.

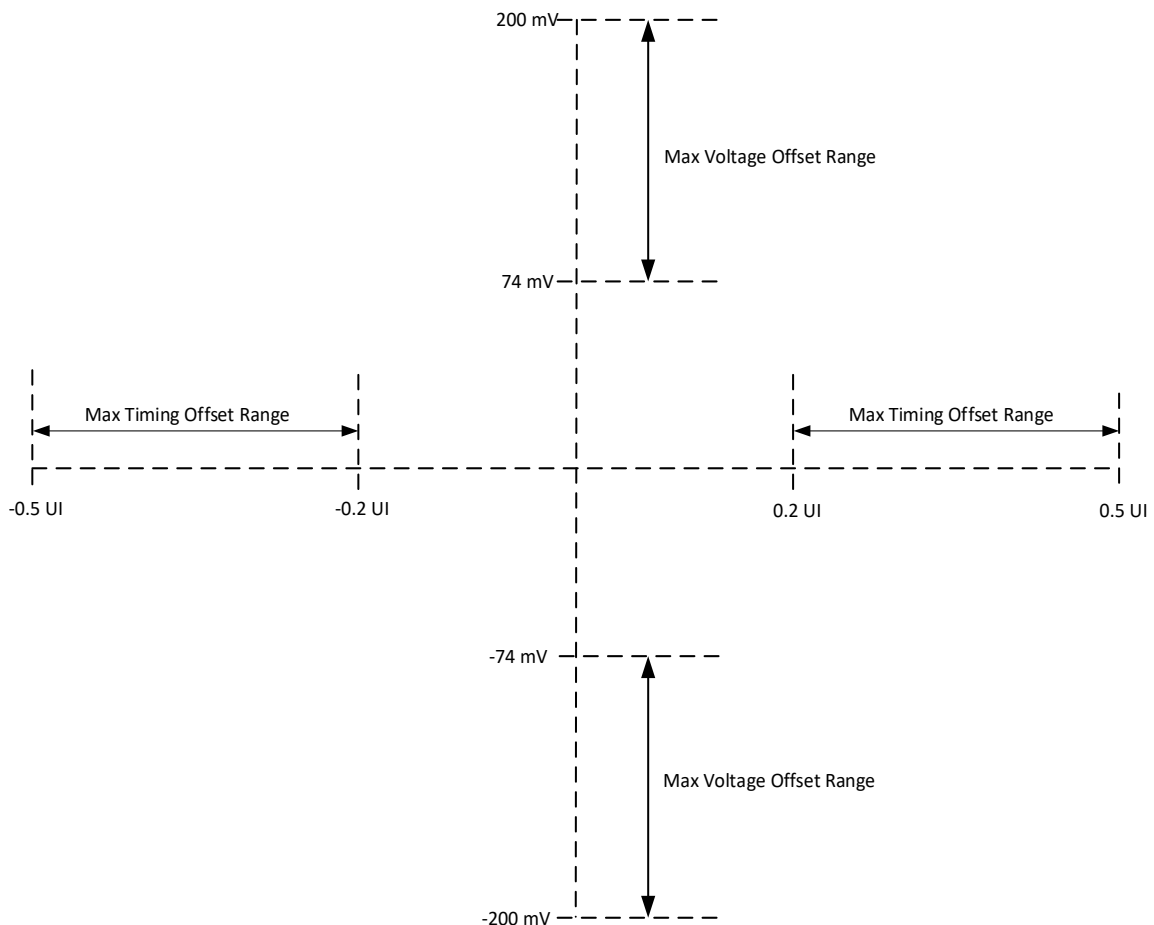
Support for timing margining, whereby a receiver sampler is offset from the nominal sampling position in the timing (horizontal) dimension, is optional. Independent margining in the positive (right) and negative (left) directions is optional but recommended. A USB4 Port that supports timing margining shall be capable of performing timing margining for each Lane independently. The timing margining may be destructive (i.e. cause actual bit errors in the Link). Timing margining can be implemented using a jitter injection circuit to inject jitter onto the Rx sampling clock to offset the data sampler from the nominal position. A receiver shall use the range and step size in Table 3-19 for timing margining.

Table 3-19. RX Margining Voltage and Timing Requirements

Parameter	Min	Max	Units
Voltage Margin Range	+/- 74	+/- 200	mV
Voltage Margining Step Size	Note 1	3	mV
Voltage Margining Steps (per direction)	Note 2	127	--
Timing Margining Range	+/- 0.2	+/- 0.5	UI
Timing Margining Step Size	Note 3	0.03	UI
Timing Margining Steps (per direction)	Note 4	31	--

Notes:

1. The minimum Voltage Margining Step Size is bounded by $\text{Min}(\text{Voltage Margin Range})/\text{Max}(\text{Voltage Margining Steps})$.
2. The minimum Voltage Margining Steps (per direction) is bounded by $\text{ceiling}(\text{Min}(\text{Voltage Margin Range})/\text{Max}(\text{Voltage Margin Step Size}))$.
3. The minimum Timing Margining Step Size is bounded by $\text{Min}(\text{Timing Margining Range})/\text{Max}(\text{Timing Margining Steps})$.
4. The minimum Timing Margining Steps (per direction) is bounded by $\text{ceiling}(\text{Min}(\text{Timing Margin Range})/\text{Max}(\text{Timing Margin Step Size}))$.

Figure 3-24. RX Margining Range Requirements

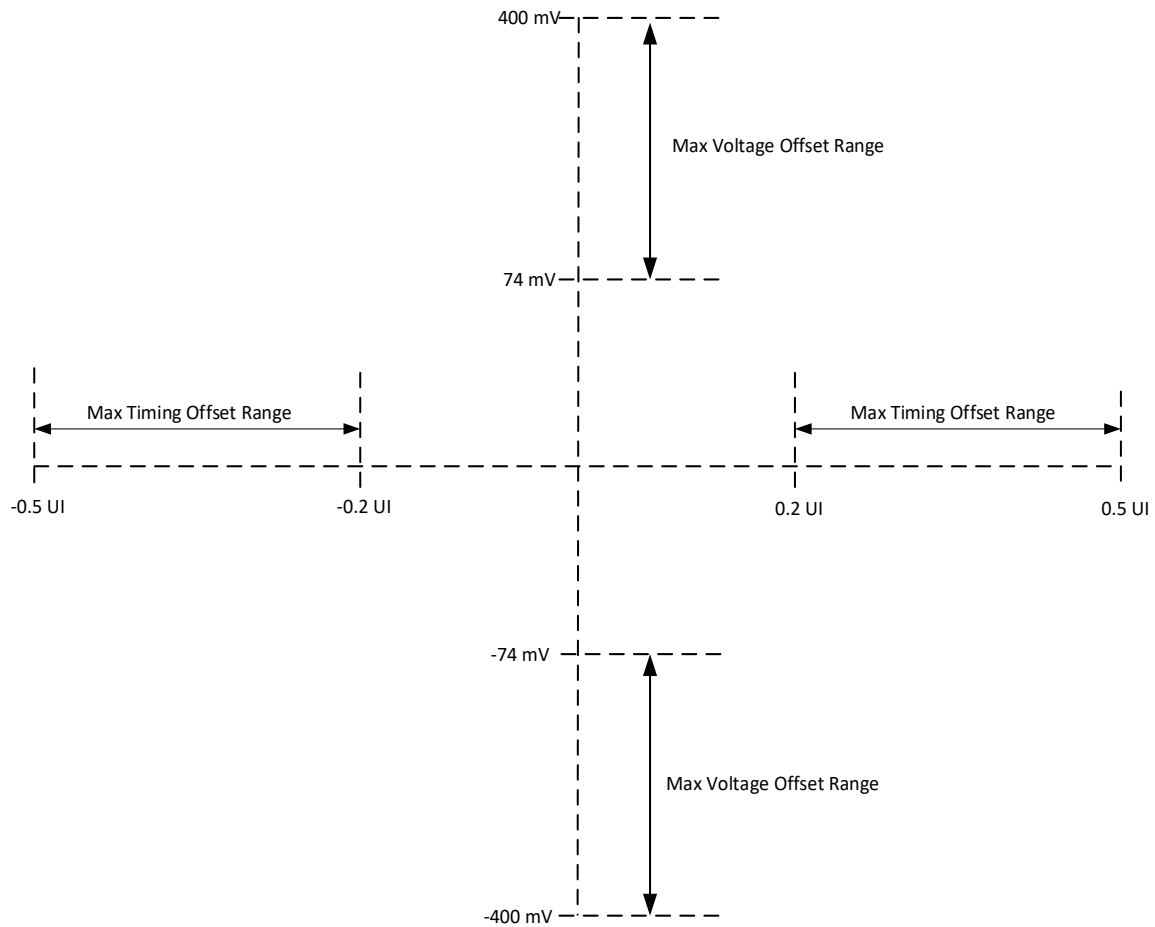
The purpose of timing margining is to measure the actual timing margin seen by the receiver when operating in a fully functional mode. Therefore, when performing timing margining, it is recommended that all RX adaptive circuitry be enabled and operating in a closed loop manner.

In addition to supporting the mandatory voltage requirements displayed in Table 3-19, a receiver may optionally support the Rx voltage margining capabilities defined in Table 3-20.

Table 3-20. Optional RX Margining Voltage Capabilities

Parameter	Min	Max	Units
Voltage Margin Range	+/- 74	+/- 400	mV
Voltage Margining Steps (per direction)	25	127	--

Figure 3-25. Optional RX Margining Range Capabilities



3.1.6.3 Receiver Parameter Access

It is recommended that all receiver training (e.g. equalization) parameters be accessible to system software to enable a system integrator with greater visibility into the operation of the receiver. This allows a system integrator to observe the stability and performance of the Link and provides an aid for debug. The receiver training parameters should be accessible from the vendor specific address range within the SB Register Space. The number and type of parameter values is implementation specific. The system integrator needs to work directly with the receiver IP (Intellectual Property) vendor to understand how to interpret the stored receiver parameters.

3.2 Gen 4 Mode of Operation

This section describes the Electrical Layer specifications for a Router Assembly that supports Gen 4 mode of operation.

The Electrical Layer specifications detail the requirements and testing methodologies for achieving reliable communication and obtaining interoperability over USB4 interconnects employing passive or active cables. The Gen 4 Electrical Layer utilizes 3-level Pulse Amplitude Modulation (PAM3) at a Baud rate of 25.6GB per Lane for conveying data over the physical media. Each PAM3 symbol encodes 1.57 bits obtained through 11-bits to 7-trits mapping. A Gen 4 Link shall operate with a Trit Error Ratio of 1E-8 or lower without Forward Error Correction (FEC). Spread-Spectrum-Clocking (SSC) shall be applied on the transmitted high-speed signals, with a single clock source used for all the transmitters within a USB4 Port.

3.2.1 Gen 4 Electrical Ecosystem

3.2.1.1 Insertion-Loss Considerations (Informative)

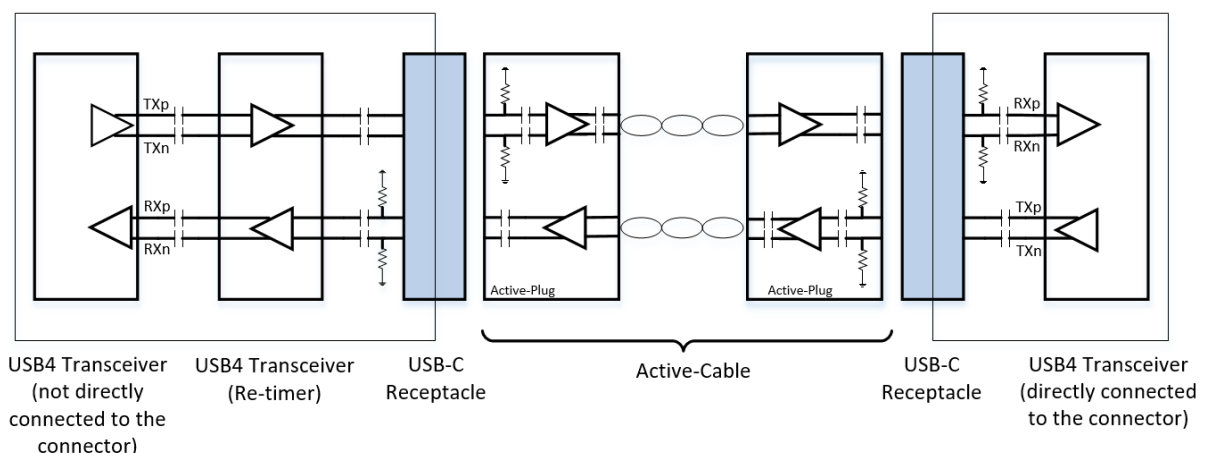
The insertion-loss of the physical media associated with the different system topologies is a key factor for facilitating Gen 4 electrical compliance. It is recommended that Router Assemblies limit the total insertion-loss from the USB Type-C receptacle to the Gen 4 transceiver such that the total insertion-loss is less than or equal to 9.5 dB at 12.8 GHz, including the receptacle tongue, the PCB trace, the integrated circuit's package and die load. The electrical characteristics of the passive and active cables supported for Gen 4 are defined in the USB Type-C Specification.

For a Captive Device that employs a passive attached cable, it is recommended that the device limit the total insertion-loss from the USB Type-C plug to the USB4 transceiver such that the total insertion-loss for a Captive Device supporting Gen 4 is less than or equal to 19 dB at 12.8 GHz, including the plug, the cable, the on-board connector, the PCB trace, the integrated circuit's package, and the die load.

3.2.1.2 AC Coupling Capacitors

All of the Lane 0 and Lane 1 electrical interfaces of a Router Assembly shall be AC-coupled. The SBTX and SBRX lines shall not be AC-coupled. All Lane 0 and Lane 1 transmit paths of a Router Assembly shall include AC-coupling capacitance between 135 nF and 265 nF. All Lane 0 and Lane 1 receive paths of a Router Assembly that are directly connected to a USB Type-C connector shall include AC-coupling capacitance between 300 nF and 363 nF, together with discharge resistors between 200 K Ω and 242 K Ω . AC-coupling capacitors with discharge resistors may be also placed at the receive paths of a Router Assembly that are not directly connected to USB Type-C connector.

Figure 3-26. Example AC-Coupling Capacitors Placement



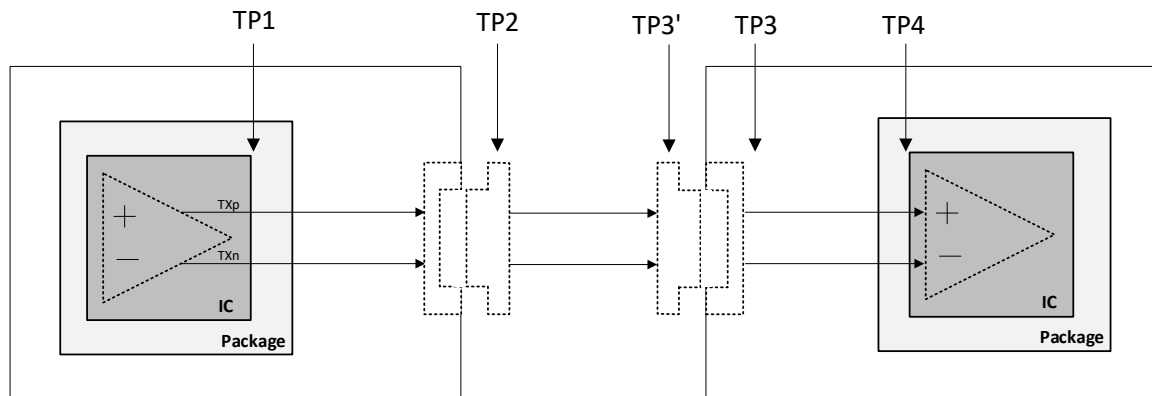
3.2.2 Gen 4 Electrical Compliance Methodology

3.2.2.1 System Compliance Test Points

All measurements shall be referenced to the compliance test points listed in Table 3-21 and shown in Figure 3-27. Calibration shall be applied in cases where direct measurement is not feasible.

Table 3-21. Electrical Compliance Test Points

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for Gen 4 electrical testing.
TP2	Transmitter port connector output	Defined at the output of a compliance plug fixture.
TP3	Receiver port connector output	Defined at the receptacle side of the connector. All measurements at this point shall be done while applying the reference equalization function.
TP3'	Receiver port connector input	Defined at the output of a compliance plug fixture.
TP4	Receiver IC input	Not used for Gen 4 electrical testing.

Figure 3-27. Gen 4 Compliance Test Point Definitions**3.2.2.2 Reference Clock-and-Data-Recovery (CDR) Function**

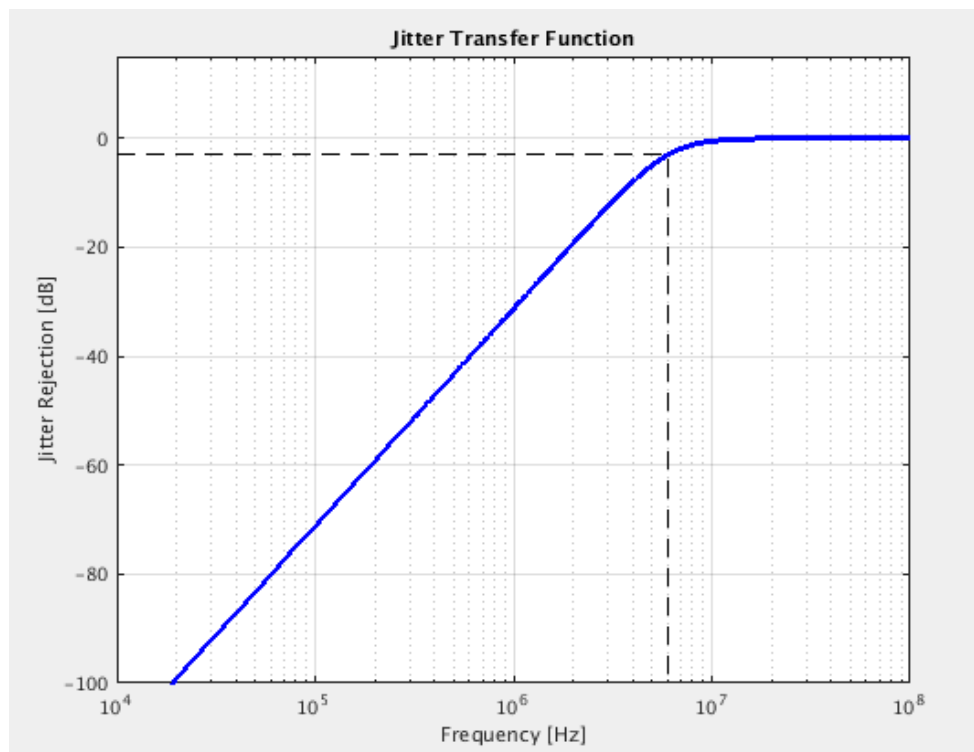
The reference clock-and-data-recovery (CDR) function is modeled by a 2nd order PLL response (type II), which derives the following jitter transfer function described in Laplace domain:

$$H_{jitter}(s) = \frac{s^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2}$$

where:

- s is the Laplace domain frequency term
- ζ is the damping factor
- ω_n is the natural frequency of the system

The damping factor (ζ) and natural frequency (ω_n) used for compliance testing shall be 0.71 and 3.8E7 rad/sec respectively, forming a High-Pass-Filter jitter transfer function with 3 dB point at 6 MHz.

Figure 3-28. Gen 4 Jitter Transfer Function**3.2.2.3 Time Domain Measurements**

Time domain measurements shall be performed using a real-time oscilloscope (or equivalent equipment) with an input bandwidth of 25 GHz \pm 1 GHz and a single-ended impedance of 50 Ω . The time domain measurement equipment shall support the Gen 4 reference CDR defined in Section 3.2.2.2.

3.2.2.4 Compliance Boards**3.2.2.4.1 Compliance Plug Test Board**

A high-quality USB Type-C plug-to-SMA/SMP test fixture shall be used to enable Router Assembly compliance testing. The fixture shall be comprised of a USB Type-C plug and a short paddle card that can be connected to a coaxial cable with a SMA/SMP connector at its end. The target single-ended impedance of the fixture shall be of 42.5 Ω .

The reference points TP2 and TP3' are defined such that the insertion-Loss from the connector pads to the compliance points is 0.5 dB \pm 0.25 dB at 5 GHz, 1 dB \pm 0.25 dB at 10 GHz, and 1.3 dB \pm 0.25 dB at 12.8 GHz. Extra loss and distortion elements shall be compensated by physical and/or mathematical means.

3.2.2.4.2 Compliance Receptacle Test Board

A high-quality USB Type-C receptacle-to-SMA/SMP test fixture shall be used to enable the testing of Captive Devices. The fixture shall be comprised of a USB Type-C receptacle and a short PCB trace that may be connected to coaxial cable with SMA/SMP connector at its end. The target single-ended impedance of the fixture shall be of 42.5 Ω .

The reference point TP3 is defined such that the insertion-loss from the connector pads to the compliance point is 0.5 dB \pm 0.25 dB at 5 GHz, 1 dB \pm 0.25 dB at 10 GHz, and 1.3 dB \pm 0.25 dB at 12.8 GHz. Extra loss and distortion elements shall be compensated by physical and/or mathematical means.

3.2.3 Gen 4 Router Assembly Transmitter Compliance

Transmitter compliance testing is defined at the output of a compliance plug fixture in the TP2 reference point (the compliance plug fixture is specified in Section 3.1.2.6.1).

Table 3-22 defines the transmitter parameters that shall apply for Gen 4 mode of operation. During all tests, except when measuring the electrical-idle output voltage, the transmitter under test shall send PRTS7 pattern and the neighboring transmitters shall transmit PRTS19 pattern.

Table 3-22. Transmitter Specifications for Gen 4 (at TP2)

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	39.0508	39.0742	ps	Corresponding to the Gen 4 baseline Baud rate of 25.6GB with an uncertainty range of -300 ppm to 300 ppm. See Notes 1, 2.
V_SWING	Peak differential voltage swing	410	545	mV	See Note 9 and Section 3.2.3.2.
TX_LEVELS_MISMATCH	Levels separation mismatch ratio	0.975	--	--	See Note 9 and Section 3.2.3.3.
TX_SNDR	Signal to Noise and Distortion Ratio	32.5	--	dB	See Note 9 and Section 3.2.3.4.
TX_ISI_MARGIN	Signal to Residual ISI Ratio	11	--	dB	See Note 9 and Section 3.2.3.5.
TX_IRL	Integrated Return-Loss	--	--	dB	See Section 3.2.3.6.
RL (Informative)	Informative Return Loss Mask	--	--	dB	See Section 3.2.3.7.
TX_EQ	Transmitter Equalization Settings	--	--	--	See Section 3.2.3.8.
AC_CM	AC Common Mode voltage	--	100	mV pp	
V_ELEC_IDLE	Peak voltage when the transmitter is in electrical-idle	--	20	mV	See Note 3.
INIT_FREQ_VARIATION	Initial non-modulated transmitter frequency applied during training before enabling the SSC modulation	-300	300	ppm	See Notes 1 and 4, Section 3.2.3.10, and Figure 3-34.
DELTA_FREQ_200ns	Frequency variation during Link training over 200 ns measurement windows	--	600	ppm	See Note 1, Section 3.2.3.10 and Figure 3-34.
DELTA_FREQ_1000ns	Frequency variation during Link training over 1 μ s measurement windows	--	900	ppm	See Note 1, Section 3.2.3.10 and Figure 3-34.
FREQ_OVERSHOOT	Maximum transient frequency offset from the Link baseline rate, including the clock source accuracy, dynamic clock switching effects and frequency variations induced by low frequency jitter	--	600	ppm	See Note 1, Section 3.2.3.10 and Figure 3-34.

Symbol	Description	Min	Max	Units	Comments
SSC_DOWN_SPREAD_RANGE	Dynamic range of the SSC down-spreading	0.2	0.3	%	See Notes 1, 5 and 9, Sections 3.2.3.10, and Figure 3-34.
SSC_DOWN_SPREAD_RATE	SSC down-spreading modulation rate	30	33	KHz	See Notes 1, 6 and 9, Sections 3.2.3.10, and Figure 3-34.
SSC_PHASE_DEVIATION	Phase jitter associated with the SSC modulation	2.5	15.5	ns pp	See Notes 1 and 9, Sections 3.2.3.10, and Figure 3-34.
SSC_SLEW_RATE	SSC modulation frequency slew rate (df/dt)	--	500	ppm/μs	See Notes 1, 7 and 9, Sections 3.2.3.10, and Figure 3-34.
UJ	Sum of uncorrelated DJ and RJ components	--	0.17	UI pp	The RJ shall be extrapolated to 1E-8 statistics. See Note 9 and Section 3.2.3.9.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.075	UI pp	See Note 9 and Section 3.2.3.9.
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	--	0.03	UI pp	See Notes 8 and 9, and Section 3.2.3.9.
EVEN_ODD	Difference between the mean jitter of symbols associated with even and odd indexes	--	0.02	UI pp	See Note 9 and Section 3.2.3.9.
LANE_TO_LANE_SKEW	Skew between any two transmit signals of the same USB4 Port	--	26	ns	
V_TX_DC_AC_CONN	Instantaneous single-ended voltage limit at TP2 during transmitter activation and de-activation	-0.5 (min1) -0.3 (min2)	1.0	V	See Note 10.

Notes:

1. Shall be extracted from the signal's phase after applying a 2nd order low-pass filter with 3 dB point at 6 MHz.
2. Shall be calculated after applying a uniform moving average filter with window size of 7500 trits over the instantaneous UI measurements.
3. Shall be extracted after applying first order low-pass filter with 3 dB point at 1.25 GHz.
4. Low frequency jitter variations shall be filtered out by averaging the extracted frequency variation waveform over a window of at least 30 μs.
5. Shall be extracted from the transmitted signal phase and calculated as the difference of the maximum and minimum modulated frequencies.
6. Shall be extracted from the transmitted signal phase and calculated based on the average time interval between the frequency peaks.
7. Shall be extracted from the transmitted signal phase and calculated over measurement intervals of 0.5 μs. Jitter induced variations shall be filtered out during this measurement.
8. Shall be calculated while applying 2nd order Low-Pass-Filter with 3 dB cut-off at 0.3 MHz on the measured jitter. This filter shall be applied on top of the reference jitter transfer function described in Section 3.2.2.2.
9. The transmitter equalization shall be set to the default Preset during this test as described in Section 3.2.3.8.
10. This requirement applies to all Link states and during power-on, power-off, and transitions between Asymmetrical and Symmetrical Links. (min1, max) is measured with a 200 KΩ receiver load, and (min2, max) is measured with a 50 Ω receiver load. The ground offset between a DFP and UFP does not contribute to V_TX_DC_AC_CONN.

3.2.3.1 Linear Fit Pulse Response

The following procedure is used to determine the linear fit pulse response and associated linear fitting error. The linear fit pulse response represents the linear output to a unit rectangular input with a width of 1 UI.

1. The transmitter shall be configured to transmit pre-defined periodic pattern.
2. Apply the reference CDR function on the captured signal (defined in Section 3.2.2.2).
3. Extract the linear fit pulse from the measured waveform using the parameters specified in Table 3-23:
 - a. Define an input pattern $x(n)$ to be a single period of the pattern with length N_{seq} and an output signal to be the captured waveform $y(n)$, sampled at M times the signal baud rate.
 - b. Correlate the captured waveform and the reference input pattern for aligning the output signal to the input pattern.
 - c. Average the captured waveform at intervals of single period of the pattern ($N_{seq} \cdot M$ samples) for filtering out uncorrelated noise and jitter. Define $y_1(n)$ to be the averaged output waveform.
 - d. Concatenate the post-cursor input pattern corresponding to the first waveform sample at the left of the input vector $x(n)$, and the pre-cursor input pattern corresponding to the last waveform sample at the right of the input vector as follows:

$$x_1[n] = [\{x(N_{seq}-N_{post}+1), x(N_{seq}-N_{post}+2), \dots, x(N_{seq})\}, \{x(1), x(2), \dots, x(N_{seq})\}, \{x(1), x(2), \dots, x(N_{pre})\}]$$

- e. Zero pad $x_1(n)$ to yield $x_z(n)$ such that $M-1$ zeros are inserted between each adjacent entries, before the first entry and after the last entry of $x_1(n)$.
- f. Present the output signal $y_1(n)$ as the convolution of $x_z(n)$ and FIR filter $h(n)$ containing $N_{taps} \cdot M$ coefficients:

$$y_1(n) = \sum_{k=1}^{N_{taps} \cdot M} x_z(n - k + N_{taps} \cdot M) \cdot h(k)$$

and in matrix representation:

$$y_1^{[(N_{seq} \cdot M) \times 1]} = X_z^{[(N_{seq} \cdot M) \times (N_{taps} \cdot M)]} \cdot h^{[(N_{taps} \cdot M) \times 1]}$$

where:

$$X_z = \begin{bmatrix} x_z(N_{taps} \cdot M) & x_z(N_{taps} \cdot M - 1) & \dots & x_z(3) & x_z(2) & x_z(1) \\ x_z(N_{taps} \cdot M + 1) & x_z(N_{taps} \cdot M) & \dots & x_z(4) & x_z(3) & x_z(2) \\ x_z(N_{taps} \cdot M + 2) & x_z(N_{taps} \cdot M + 1) & \dots & x_z(5) & x_z(4) & x_z(3) \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ x_z(N_{taps} \cdot M + N_{seq} \cdot M - 1) & x_z(N_{taps} \cdot M + N_{seq} \cdot M - 2) & \dots & x_z(N_{seq} \cdot M) & \dots & \dots \end{bmatrix}$$

- g. Extract the filter h coefficients by applying least-squares fitting:

$$h = [X_z^T \cdot X_z]^{-1} \cdot X_z^T \cdot y_1$$

where the superscript “T” denotes the matrix transpose operation.

- h. Extract the linear fitting error waveform:

$$e = y_1 - X_z \cdot h$$

The following parameters shall be used in the linear fit pulse calculation:

Table 3-23. Linear fit Pulse Extraction Parameters

Parameter	Description	Value	Units
N_{taps}	Linear fit pulse length	200	UI
N_{post}	Linear fit pulse post-cursor length	$N_{\text{taps}}-6$	UI
N_{pre}	Linear fit pulse pre-cursor length	5	UI
M	Number of samples per UI	32	

3.2.3.2 Transmitter Voltage Swing

The transmitter differential voltage swing (V_{SWING}) shall be calculated as the sum of the linear fit pulse response samples divided by the corresponding number of samples per UI.

The transmitter voltage swing shall be extracted as follows:

1. Configure the transmitter to send PRTS7 pattern and capture the signal at TP2 measurement point.
2. Apply the reference CDR function as defined in Section 3.2.2.2.
3. Extract the linear fit pulse response $p(n)$ as described in Section 3.2.3.1, with M samples per UI (see Table 3-23).
4. Calculate V_{SWING} as follows:

$$V_{\text{SWING}} = \frac{\sum_{n=1}^{M \cdot N_{\text{taps}}} p(n)}{M \cdot \sum_{n=-2}^1 C[n]}$$

where:

- p is the linear fit pulse response
- M is the number of samples per UI (see Table 3-23)
- N_{taps} is the linear fit pulse response length (see Table 3-23)
- $C[n]$ are the normalized values of the Tx Preset taps applied during the measurement, extracted as described in Section 3.2.3.8

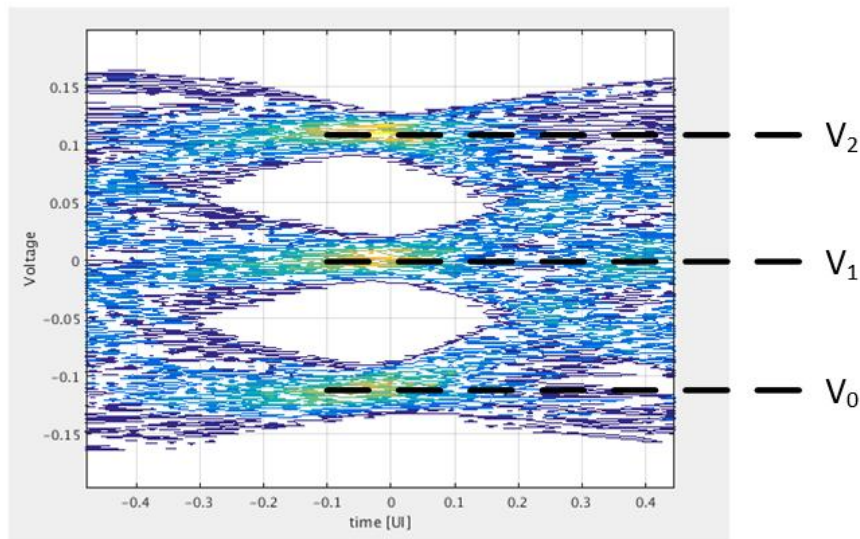
3.2.3.3 Transmitter Levels Mismatch

The transmitter levels mismatch ratio shall be calculated as a function of the mean PAM3 constellation levels as follows:

$$\text{TX_LEVELS_MISMATCH} = \min\{(V_2-V_1)/\Delta, (V_1-V_0)/\Delta\}$$

where:

- V_0 , V_1 , and V_2 are the mean constellation levels corresponding to PAM3 symbols 0, 1, and 2 (V_0 is the bottom level, V_1 is the middle level and V_2 is the upper level)
- $\Delta = (V_2 - V_0)/2$

Figure 3-29. PAM3 Constellation Levels

The mean constellation levels shall be extracted as follows:

1. Configure the transmitter to send PRTS7 pattern and capture the signal at TP2 measurement point.
2. Apply the reference CDR function as defined in Section 3.2.2.2.
3. Down-sample the signal to a single sample per UI, at the sampling phase corresponding to the center of the eye.
4. For each PAM3 symbol level x , V_x is the mean value of the corresponding waveform samples ($x=0, 1, 2$).

3.2.3.4 Transmitter Signal to Noise and Distortion

The transmitter signal-to-noise and distortion ratio (TX_SNDR) shall be calculated as the ratio between the linear fit pulse peak and the root square sum of the linear fit error (σ_e) and the additive noise (σ_n).

The transmitter signal-to-noise and distortion ratio shall be calculated as follows:

1. Configure the transmitter to send PRTS7 pattern and capture the signal at TP2 measurement point.
2. Apply the reference CDR function as defined in Section 3.2.2.2.
3. Extract the transmitter non-linearity noise RMS:
 - a. Average the signal across repeating PRTS7 cycles for filtering out additive noise and jitter.
 - b. Extract the linear fit pulse response $p(k)$ and the linear fit error waveform as described in Section 3.2.3.1. The reference input sequence used for extracting the linear fit pulse response and error waveform shall be modified for taking the levels mismatch into account such that normalized input symbols $\{-1, 0, 1\}$ is replaced by $\{-1, V_1^*, 1\}$, where $V_1^* = \frac{V_1 - \frac{1}{2}(V_2 + V_0)}{\frac{1}{2}(V_2 - V_0)}$ (V_0, V_1, V_2 are extracted as described in Section 3.2.3.3).
 - c. Denote the standard deviation of the linear fitting error as σ_e .

4. Extract the transmitter additive noise RMS:
 - a. For each of the V_0 , V_1 and V_2 constellation levels, measure the RMS deviation from the mean voltage at a fixed low-slope point in runs of at least 6 consecutive identical PAM3 symbols (PRTS7 includes such a run for each of the PAM3 levels).

The oscilloscope's intrinsic noise shall be removed or compensated for enabling accurate measurement of the transmitter additive noise.
 - b. σ_N is the average RMS deviation extracted from the three levels.
5. The TX_SNDR is defined as follows:

$$TX_SNDR = 20 \cdot \log_{10} \left(\frac{P_{max}}{\sqrt{\sigma_e^2 + \sigma_n^2}} \right)$$

where, P_{max} is the maximum value of the linear fit pulse response $p(k)$.

3.2.3.5 Transmitter ISI Margin

The transmitter ISI margin (TX_ISI_MARGIN) shall be calculated as the ratio between the equalized linear fit pulse peak and the sum of the absolute values of the pre cursor ISI and the post cursor ISI from tap 13 and above.

The transmitter ISI margin shall be calculated as follows:

1. Configure the transmitter equalization to the default Preset as described in Section 3.2.3.8. Send PRTS7 pattern and capture the signal at the TP2 measurement point.
2. Apply the reference CDR function as defined in Section 3.2.2.2.
3. Extract the linear fit pulse response $p(n)$ as described in Section 3.2.3.1.
4. Calculate the TX_ISI_MARGIN as the ratio between the signal and the sum of the 18 largest ISI samples, including the pre-cursors and the post-cursors from tap 13 and above:

$$TX_ISI_MARGIN = dB \left(\frac{Signal}{\sum_{i=1}^{18} Sorted_ISI[i]} \right)$$

where:

- *Signal* is calculated by integrating the pulse response samples over 1 UI window around the peak of the pulse, as following:

$$Signal = \sum_{n_{pk}-0.5 \cdot M}^{n_{pk}+0.5 \cdot M-1} p(n)$$

- *Sorted_ISI* is a descending order sorted version of the ISI vector comprised of the union of the Pre_Cursor_ISI and the Post_Cursor_ISI vectors, defined as follows:

$$Pre_Cursor_ISI[i] = \sum_{n_{pk}-(N_{pre}-i+0.5) \cdot M}^{n_{pk}-(N_{pre}-i-0.5) \cdot M} |p(n)|, \quad i = 1, 2, \dots, N_{pre} - 1$$

$$Post_Cursor_ISI[j] = \sum_{n_{pk}+(11.5+j) \cdot M}^{n_{pk}+(12.5+j) \cdot M} |p(n)|, \quad j = 1, 2, \dots, N_{post} - 13$$

- n_{pk} is the linear fit pulse response peak index.
- M , N_{pre} , and N_{post} are the oversampling ratio, number of pre-cursor taps, and number of post-cursor taps, respectively, as defined in Table 3-23.

3.2.3.6 Transmitter Integrated Return-Loss

The transmitter Integrated Return-Loss (TX_IRL) shall be calculated as the integrated power spectral density of the reflected signal normalized by the integrated power spectral density of the incident signal.

The transmitter Integrated Return-Loss is extracted as follows:

$$IRL = 20 \cdot \log_{10} \left(\sqrt{\frac{\int_0^{20\text{GHz}} |V_{in}(f)|^2 \cdot |S_{dd22}(f)|^2 df}{\int_0^{20\text{GHz}} |V_{in}(f)|^2 df}} \right)$$

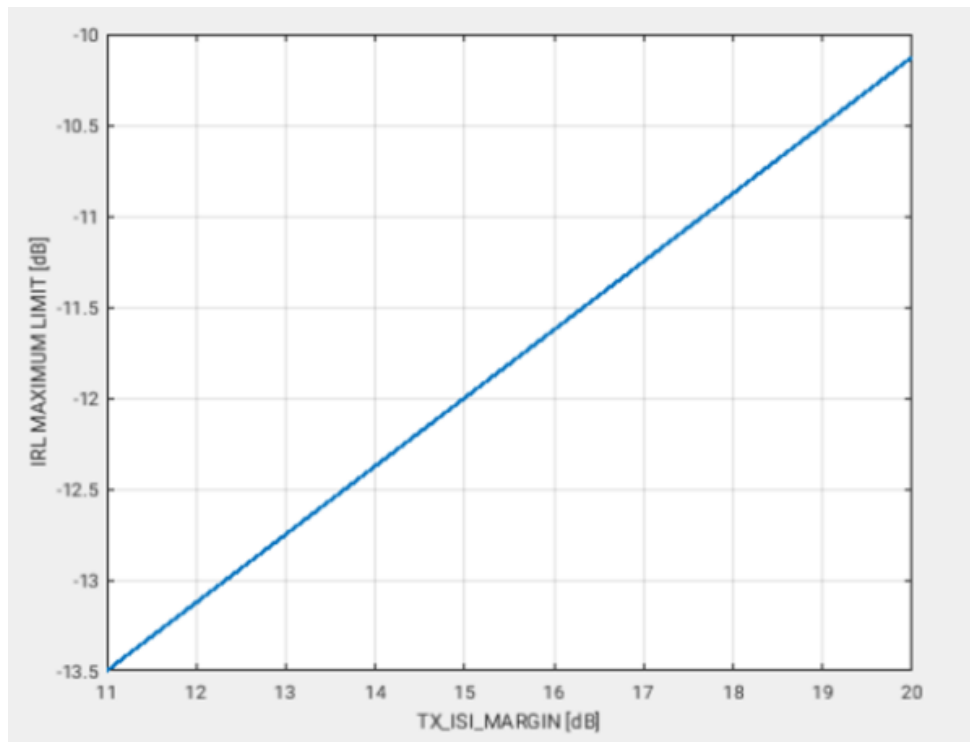
where:

- $S_{dd22}(f)$ is the Return-Loss of the transmitter at TP2, referenced to single-ended load impedance of 42.5Ω
- $V_{in}(f)$ is the spectrum of ideal PAM signal with 20% slew rate, defined as $V_{in}(f) = \frac{\sin(\pi \cdot f \cdot T_r)}{\pi \cdot f \cdot T_r} \cdot \frac{\sin(\pi \cdot f \cdot T_b)}{\pi \cdot f \cdot T_b}$, with $T_b=39.0625\text{ps}$ and $T_r=0.2 \cdot T_b$

The TX_IRL maximum limit is a function of the measured TX_ISI_MARGIN, as specified in Section 3.2.3.5:

$$IRL \leq -13.5 + (TX_ISI_MARGIN - 11) \times 0.375$$

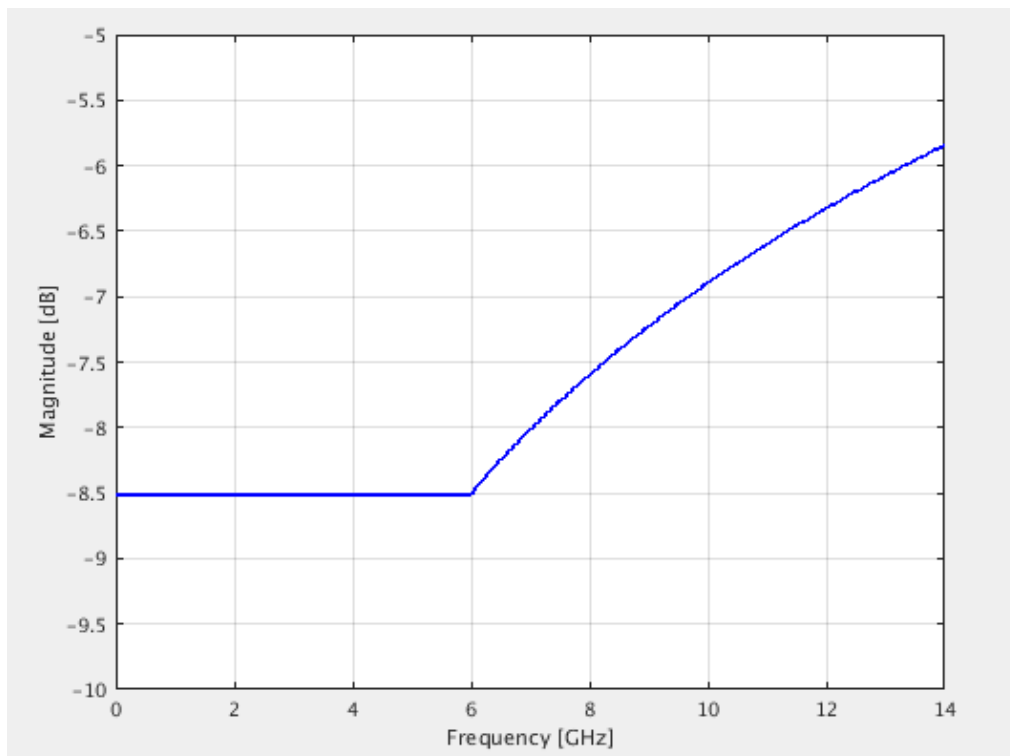
Figure 3-30. IRL Maximum Limit as a Function of TX_ISI_MARGIN



3.2.3.7 Transmitter Differential Return Loss Mask (Informative)

Transmitter return-loss measurements are referenced to a single-ended impedance of 42.5 Ω . When measured at TP2, the differential mode return loss is recommended not to exceed the limits given in the following equation:

$$SDD22(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 6 \\ -5.84 + 7.2 \cdot \log_{10} \left(\frac{f_{GHz}}{14} \right) & 6 < f_{GHz} \leq 14 \end{cases}$$

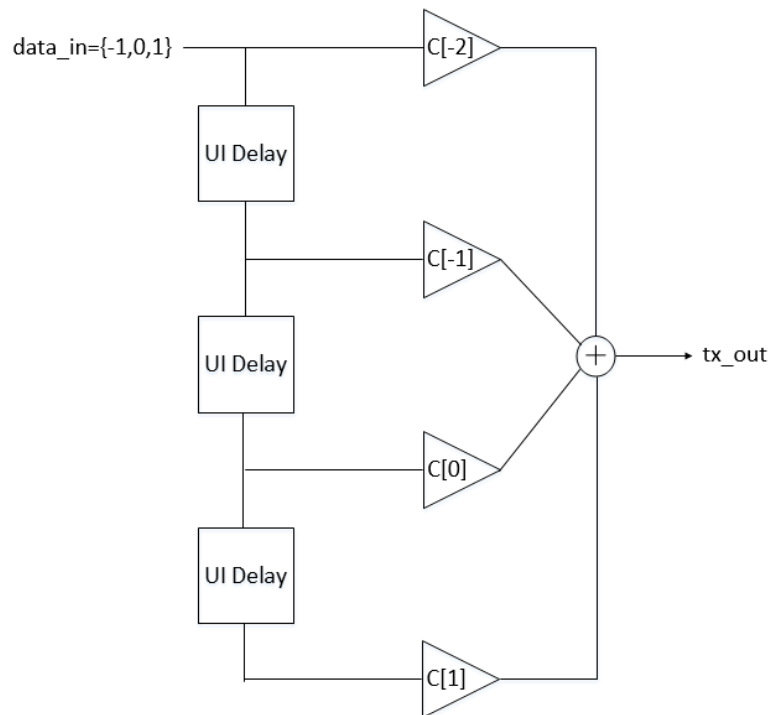
Figure 3-31. Gen 4 TX Differential Return Loss Mask**3.2.3.8 Transmitter Equalization**

A Router Assembly transmitter shall support coefficient-based Feed-Forward Equalization (FFE) at its output. The equalizer's structure is based on a 4-tap UI-spaced finite-impulse-response (FIR) filter. The output corresponding to the n-th transmitted symbol shall be calculated as follows:

$$tx_out[n] = \sum_{k=-2}^1 data_in[n-k] \cdot C[k]$$

where:

- tx_out[n] is the transmitted level at time instant n
- data_in[n-k] is the normalized input data at time instant n-k
- C[k] is the kth coefficient of the FIR filter

Figure 3-32. Transmitter Equalizer Structure

The transmitter shall support 42 Preset configurations, numbered from 0 to 41. Preset configurations 0-39 represent operation mode with full-swing transmitter output, while configurations 40-41 define low swing mode. When one of configurations 40 or 41 are selected, the transmitter's output swing shall be attenuated by 6 ± 1 dB compared to its full-swing mode of operation.

The default equalization Preset of the transmitter shall be configured to the setting that obtains the lowest Data Dependent Jitter (DDJ), as described in Section 3.2.3.9. During Link training, the far-end Receiver can change the Transmitter Preset configuration through the SBTX/SBRX side-band protocol. The transition from one Preset configuration to another is not required to be glitch-free. However, completion shall be acknowledged only after the new configuration is stable.

Table 3-24 lists the Preset configurations that a transmitter shall support.

Table 3-24. Transmitter Equalization Presets

Preset Number	C[-2]	C[-1]	C[0]	C[1]
0	0	0	1	0
1	0	0	0.95	-0.05
2	0	0	0.9	-0.1
3	0	0	0.85	-0.15
4	0	-0.05	0.95	0
5	0	-0.05	0.9	-0.05
6	0	-0.05	0.85	-0.1
7	0	-0.05	0.8	-0.15
8	0	-0.1	0.9	0
9	0	-0.1	0.85	-0.05

Preset Number	C[-2]	C[-1]	C[0]	C[1]
10	0	-0.1	0.8	-0.1
11	0	-0.1	0.75	-0.15
12	0	-0.15	0.85	0
13	0	-0.15	0.8	-0.05
14	0	-0.15	0.75	-0.1
15	0	-0.15	0.7	-0.15
16	0.025	-0.15	0.825	0
17	0.025	-0.15	0.775	-0.05
18	0.025	-0.15	0.725	-0.1
19	0.025	-0.15	0.675	-0.15
20	0	-0.2	0.8	0
21	0	-0.2	0.75	-0.05
22	0	-0.2	0.7	-0.1
23	0	-0.2	0.65	-0.15
24	0.025	-0.2	0.775	0
25	0.025	-0.2	0.725	-0.05
26	0.025	-0.2	0.675	-0.1
27	0.025	-0.2	0.625	-0.15
28	0.05	-0.2	0.75	0
29	0.05	-0.2	0.7	-0.05
30	0.05	-0.2	0.65	-0.1
31	0.05	-0.2	0.6	-0.15
32	0	-0.25	0.75	0
33	0	-0.25	0.7	-0.05
34	0.025	-0.25	0.725	0
35	0.025	-0.25	0.675	-0.05
36	0.05	-0.25	0.7	0
37	0.05	-0.25	0.65	-0.05
38	0.075	-0.25	0.675	0
39	0.075	-0.25	0.625	-0.05
40	0	-0.10	0.40	0
41	0	0	0.50	0
Notes: 1. The coefficients are normalized such that $ C_{-2} + C_{-1} + C_0 + C_1 $ corresponds to the full output swing. Preset configurations 40 and 41 represent operation mode with reduced transmitter swing. 2. The tolerance of the normalized coefficients shall be of ± 0.015 for C[-2] and of ± 0.025 for C[-1], C[0], and C[1] coefficients.				

The transmitter FFE coefficients shall be extracted as follows:

1. Configure the transmitter to Preset-0 and send PRTS7 pattern. Capture the signal at TP2 measurement point and apply the reference CDR function defined in Section 3.2.2.2.
2. Extract the linear fit pulse response $p^0[n]$ as defined in Section 3.2.3.1.
3. Configure the transmitter to the Preset- i under test and send PRTS7 pattern. Capture the signal at TP2 measurement point and apply the reference CDR function defined in Section 3.2.2.2.

Note: Additional mathematical filtering is allowed in order for easier acquisition of the signal, provided that the added filters are removed before extracting the coefficients values.

4. Extract the linear fit pulse response $p^i[n]$.
5. For each value of m in the range $-M/2$ to $M/2-1$ (M is the number of samples per UI defined in Table 3-23):
 - a. Define an $(M \times N_{\text{taps}})$ -by-4 matrix R_m (N_{taps} is the length of the linear fit pulse responses in terms of UI, as defined in Table 3-23). The elements of R_m are assigned as follows:

$$R_m(j, i + 3) = \begin{cases} p^0(m + j - M \cdot i) & \text{if } 1 \leq m + j - M \cdot i \leq M \cdot N_{\text{taps}} \\ 0 & \text{otherwise} \end{cases}$$

where $i = -2$ to 1 and $j = 1$ to $M \times N_{\text{taps}}$.

- b. The normalized coefficients of Preset- i are extracted as follows:

$$\begin{bmatrix} c_m(-2) \\ c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix} = [R_m^T \cdot R_m]^{-1} \cdot R_m^T \cdot \begin{bmatrix} p^i(1) \\ \vdots \\ p^i(M \cdot N_{\text{taps}}) \end{bmatrix}$$

- c. The linear fit pulse response is reconstructed from the matrix R_m and the normalized coefficients:

$$\begin{bmatrix} p_m^i(1) \\ \vdots \\ p_m^i(M \cdot N_{\text{taps}}) \end{bmatrix} = R_m \cdot \begin{bmatrix} c_m(-2) \\ c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix}$$

- d. The linear estimation square error is calculated as follows:

$$\varepsilon^2(m) = \sum_{k=1}^{M \cdot N_{\text{taps}}} (p^i(k) - p_m^i(k))^2$$

6. The normalized transmit equalizer coefficients $c(i)$ for a given linear fit pulse $p^i[n]$ are the values $c_m(i)$ for the value of m that minimizes $\varepsilon^2(m)$.

3.2.3.9 Transmitter Timing Parameters

The jitter parameters are extracted from the transitions between the PAM3 constellation levels as follows:

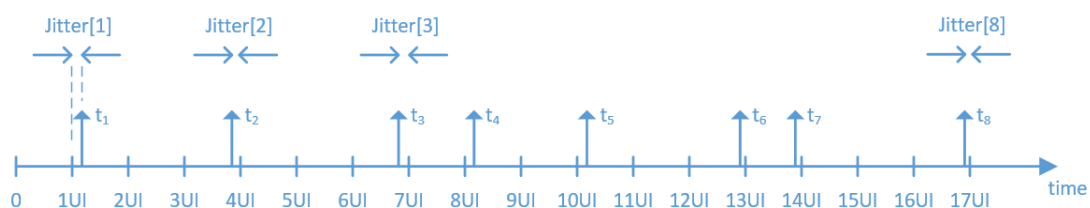
1. Configure the transmitter to send PRTS7 pattern and capture the signal at TP2 measurement point.
2. Apply the reference CDR function defined in Section 3.2.2.2.
3. Define the voltage thresholds for extracting the transitions as follows:

Table 3-25. Transition Types Between the PAM3 Constellation Levels

Transition Type	Description	Threshold Level
1	$V_2 \rightarrow V_0$	$(V_0 + V_2)/2$
2	$V_0 \rightarrow V_2$	$(V_0 + V_2)/2$
3	$V_1 \rightarrow V_0$	$(V_0 + V_1)/2$
4	$V_1 \rightarrow V_2$	$(V_1 + V_2)/2$
5	$V_2 \rightarrow V_1$	$(V_1 + V_2)/2$
6	$V_0 \rightarrow V_1$	$(V_0 + V_1)/2$

4. Extract the timing of the relevant threshold crossing for each of the transition types and define the timing jitter as the difference between the crossing times and the reference edges of an ideal recovered clock.
5. Extract the even-odd jitter by averaging the jitter associated with symbols in even indexes and in odd indexes and calculate the difference between the average values.

Figure 3-33 shows an example of the even-odd jitter extraction method:

Figure 3-33. Even-Odd Jitter Example

In this example, $\{t_n\}$ are the crossing times of the data pattern presented over the ideal grid of the recovered clock edges. In this example, the even-jitter is the average of Jitter[2], Jitter[4], Jitter[5] and Jitter[7] and the odd-jitter is the average of Jitter[1], Jitter[3], Jitter[6] and Jitter[8]. Then the even-odd jitter is calculated as the absolute value of the difference between the even and the odd jitter terms.

6. Extract the data dependent jitter (DDJ), required for separating between the correlated and uncorrelated jitter components, as follows:
 - a. for each specific transition of the periodic pattern, calculate the DDJ by averaging the transition time variations across its entire repetitions:

$$DDJ[n] = \frac{1}{K} \cdot \sum_{k=0}^{K-1} Jitter[n + k \cdot N]$$

where:

- N is the number of transitions in a single period of the pattern
 - K is the number of captured periods of the pattern
 - DDJ[n] is the Data-Dependent-Jitter associated with the n-th transition of the pattern's period ($n \in 1 \dots N$)
 - Jitter[i] is the phase variation of the i-th transition in the signal capture ($i \in 1 \dots K \cdot N$)
7. Extract the uncorrelated jitter component by subtracting the DDJ from the corresponding transition jitter:

$$UJ[i] = Jitter[i] - DDJ[mod(i - 1, N) + 1], \quad i = 1 \dots (K \cdot N)$$

The uncorrelated jitter shall be mathematically decomposed into its deterministic and random components. The even-odd jitter shall be then added to the uncorrelated deterministic jitter calculated in this step.

3.2.3.10 Transmitter Clocking during Link Training and During Steady State

A Gen 4 Link can include up to 6 Re-timers forwarding data from one end of the Link to the other end. During the initial phase of Link training, all the transmitters are enabled in parallel and send training pattern clocked without SSC down spreading. Initially, the Re-timer transmitters do not forward the incoming data but send training pattern using local clock. In the later stages of Link training, the Re-timer transmitters sequentially switch to forward the incoming data with the recovered clock. As soon as all the Re-timers complete the switching process and are locked on their incoming signal, the end-point transmitters enable the SSC modulation, which propagates through the Re-timers to the other end of the Link, obtaining steady-state operation. The end-point transmitters shall enable the SSC modulation in a glitch-free and continuous manner that meets the SSC_SLEW_RATE specifications described in Table 3-22.

On a Gen 4 Link, the Re-timers switch from sending local training data with the local clock to forwarding incoming data with the recovered clock as follows:

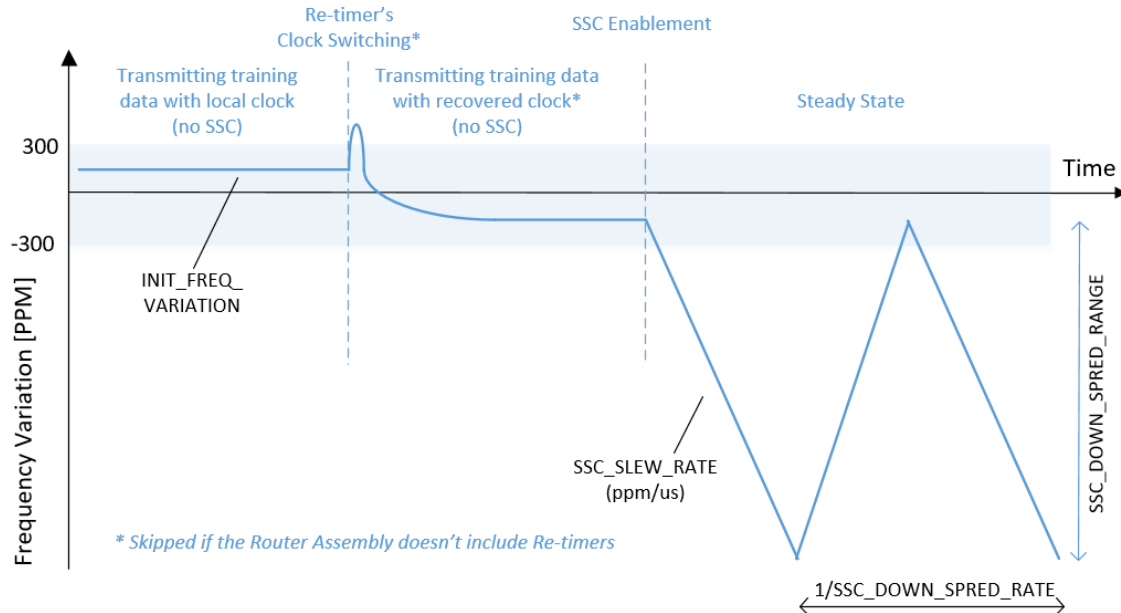
1. The Re-timer transmitters switch from sending Gen 4 TS2 local pattern to Gen 4 TS2.clksw local pattern, which is comprised of the following repeating 28 UI normalized sequence:

$$\{0, +1, -1, +1, +1, 0, -1, +1, +1, -1, 0, +1, -1, -1, +1, 0, -1, +1, -1, -1, 0, +1, -1, -1, +1, 0, -1, +1\}$$
2. The Re-timer transmitters switch from using the local clock to using the recovered clock while still sending Gen 4 TS2.clksw local pattern. The associated electrical behavior of the transmitted signal during the clock switching shall meet the DELTA_FREQ_200ns, DELTA_FREQ_1000ns and FREQ_OVERSHOOT specifications defined in Table 3-22.
3. Shortly after the clock switching event, the Re-timer switches to forwarding the incoming data (containing Gen 4 TS3 pattern propagated from the endpoint transmitter).

Note: Gen 2 and Gen 3 Links maintain the legacy behavior when switching from sending local training data with the local clock to forwarding incoming data with the recovered clock.

Note: The instantaneous frequency of different transmitters within USB4 port can be different during clock switching event.

Figure 3-34. Transmitter Output Frequency



3.2.4 Gen 4 Router Assembly Receiver Compliance

3.2.4.1 Summary of Receiver Specifications

Table 3-26 defines the receiver parameters at TP3' measurement point.

Table 3-26. Receiver Specifications

Symbol	Description	Min	Max	Units	Comments
RX_TOLERANCE	Receiver tolerance testing	--	--	--	See Section 3.2.4.2
RX_IRL(Informative)	Informative Integrated Return-Loss at TP3'	--	-13.5	dB	See Section 3.2.4.1.1
RL (Informative)	Informative Return Loss Mask at TP3'	--	See Section 3.2.4.1.2	dB	
LANE_TO_LANE_SKEW	Skew between incoming signals of the same Port at TP3'	--	44	ns	See Note 1.
V_MAX	Input signal peak differential voltage tolerance at TP3'	--	600	mV	See Note 4.
RX_INIT_FREQ_VARIATION	Initial non-modulated signal frequency applied during training	-300	300	ppm	See Notes 2, 3, Section 3.2.3.10 and Figure 3-34.
RX_DELTA_FREQ_200ns	Incoming signal's frequency variation during Link training over 200 ns measurement windows	--	600	ppm	See Note 2, Section 3.2.3.10 and Figure 3-34.

Symbol	Description	Min	Max	Units	Comments
RX_DELTA_FREQ_1000ns	Incoming signal's frequency variation during Link training over 1 μs measurement windows	--	900	ppm	See Note 2, Section 3.2.3.10 and Figure 3-34.
RX_FREQ_OVERSHOOT	Incoming signal's maximum frequency offset from the Link baseline rate during training	--	600	ppm	See Note 2, Section 3.2.3.10 and Figure 3-34.
Notes: 1. LANE_TO_LANE_SKEW specifies the maximum skew at the connector. On top of the skew measured at TP3', the following informative budget is assumed between the connector and the Router RX IC: <ul style="list-style-type: none"> Each Re-timer input-to-output skew: 8 ns. Physical media mismatches: 2 ns. 2. Extracted while applying a 2nd order low-pass filter with 3 dB point at 6 MHz over the signal phase. 3. RX_INIT_FREQ_VARIATION corresponds to the frequency offset from 25.6 GB, without including low frequency jitter induced variations that shall be filtered out. 4. V_MAX defines the differential steady-state input voltage. Limits for the transient single-ended voltage generated by the far-end transmitter are specified in Table 3-22. To avoid voltage overstress, receiver termination should be continuously enabled when the receiver is operational.					

3.2.4.1.1 Receiver Integrated Return-Loss

The receiver Integral Return-Loss (RX_IRL) shall be calculated as the integrated power spectral density of the reflected signal normalized by the integrated power spectral density of the incident signal.

The receiver Integrated Return-Loss is extracted as follows:

$$IRL = 20 \cdot \log_{10} \left(\sqrt{\frac{\int_0^{20GHz} |V_{in}(f)|^2 \cdot |S_{dd11}(f)|^2 df}{\int_0^{20GHz} |V_{in}(f)|^2 df}} \right)$$

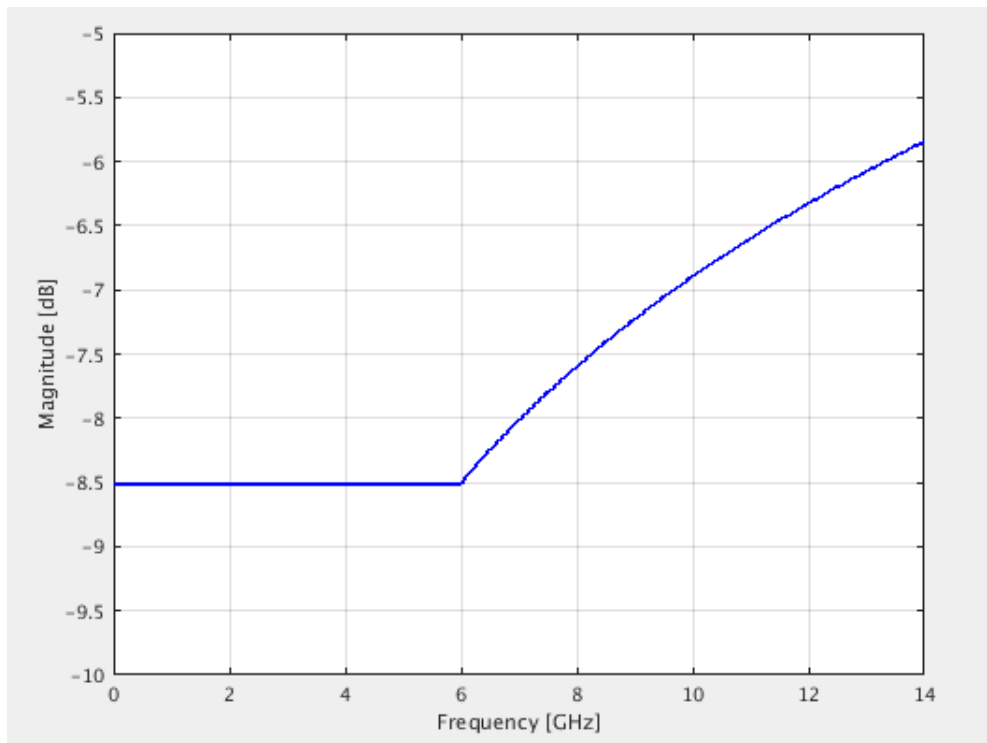
where:

- Sdd11(f) is the Return-Loss of the receiver at TP3', referenced to single-ended load impedance of 42.5Ω
- $V_{in}(f)$ is the spectrum of ideal PAM signal with 20% slew rate, defined as $V_{in}(f) = \frac{\sin(\pi \cdot f \cdot T_r)}{\pi \cdot f \cdot T_r} \cdot \frac{\sin(\pi \cdot f \cdot T_b)}{\pi \cdot f \cdot T_b}$, with $T_b=39.0625ps$ and $T_r=0.2 \cdot T_b$

3.2.4.1.2 Receiver Differential Return Loss (Informative)

Receiver return-loss measurements are referenced to a single-ended impedance of 42.5 Ω. When measured at TP3', the differential mode return loss is recommended not to exceed the limits given in the following equation:

$$SDD11(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 6 \\ -5.84 + 7.2 \cdot \log_{10} \left(\frac{f_{GHz}}{14} \right) & 6 < f_{GHz} \leq 14 \end{cases}$$

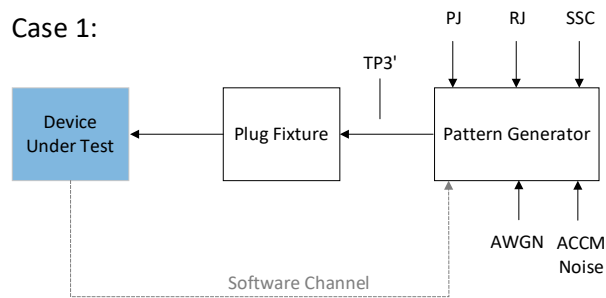
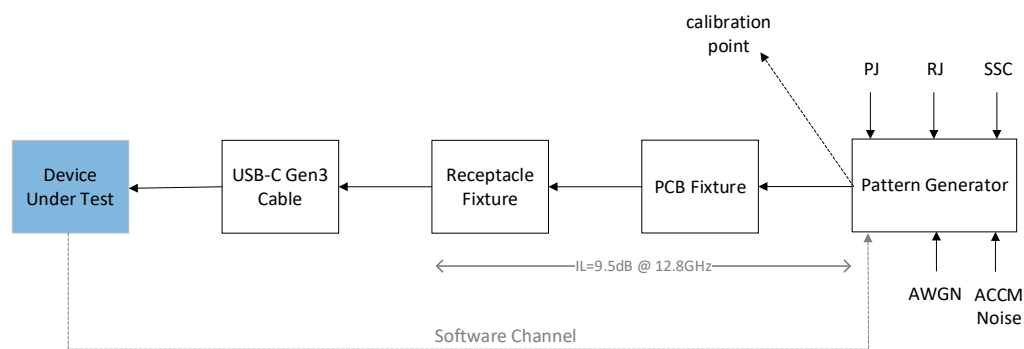
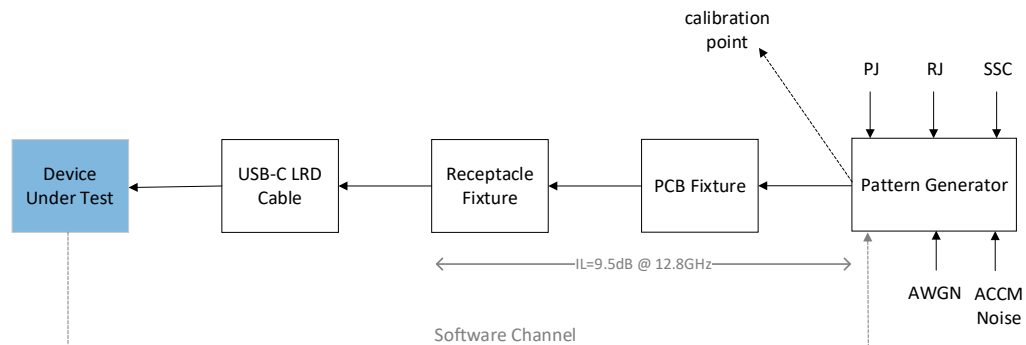
Figure 3-35. Gen 4 Receiver Differential Return-Loss Mask

3.2.4.2 Receiver Tolerance Testing

A Gen 4 receiver shall operate at a Trit Error Ratio (TER) of 1E-8 or lower without Forward Error Correction when a stressed signal is driven at its input. Tolerance testing shall be performed while all neighboring transceivers are active.

There are three test setups used for evaluating the receiver tolerance:

- “Case 1”, which addresses installations with low Insertion-Loss.
- “Case 2a”, which addresses passive cable installations with maximum Insertion-Loss. As part of this setup, the receiver under test shall be connected through a worst-case USB4 Gen 3 passive cable.
- “Case 2b”, which addresses installations employing linear re-driver (LRD) cables. As part of this setup, the receiver under test shall be connected through a worst-case USB Type-C LRD cable.

Figure 3-36. Gen 4 Receiver Tolerance Test Setup**Case 1:****Case 2a:****Case 2b:****Table 3-27. Stressed Signal for Gen 4 Receiver Compliance Testing**

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	32.5	0.975	100	0.085	0.0085
2a+2b	820	32.5	0.975	100	0.075	0.0085

A receiver shall be tested by injecting several different periodic jitter (PJ) components, one at a time. The testing shall include jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. All the specified jitter values shall be calibrated while applying the reference CDR defined in Section 3.2.2.2.

For Test Cases 2a and 2b, the stressed signal shall be further adjusted for compensating potential variations of the cable and the PCB fixture as follows (see Figure 3-37):

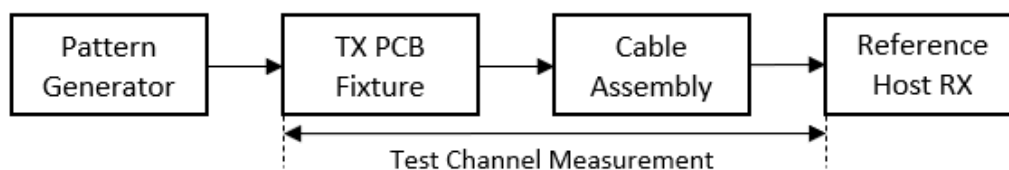
1. Measure the S-parameters of the Test Channel (TX PCB + cable assembly).
2. Cascade a Pattern-Generator model as follows:

$$Sdd21_{TOTAL} = \frac{Sdd21_{PG} \cdot Sdd21_{TC}}{1 - Sdd22_{PG} \cdot Sdd11_{TC}}$$

where:

- Sdd21_{PG} is the differential insertion-loss of the Pattern-Generator extracted by measuring step response at its output for deriving the corresponding impulse response and transforming to the frequency domain.
 - Sdd21_{TC} is the measured insertion-loss of the Test Channel comprised of the TX PCB fixture and the USB Type-C cable assembly.
 - Sdd22_{PG} is the differential return-loss of the Pattern-Generator measured at its output.
 - Sdd11_{TC} is the measured return-loss of the Test Channel.
3. Cascade the S-parameters of a reference worst-case RX host model for obtaining an end-to-end channel response.
 4. Evaluate the Link operating margin over the cascaded end-to-end channel using compliance post-processing tool with the following settings:
 - a. The transmitter parameters shall be initially configured according to Table 3-27.
 - b. The transmitter Presets table shall be configured according to the Pattern-Generator's measured Presets (as described in Section 3.2.3.8).
 5. As needed, adjust the transmitter voltage swing and periodic-jitter (PJ) magnitude such that the operating margin for TER=1E-8 will be 0±0.1 dB. If the fitted insertion-loss of the end-to-end channel at 12.8 GHz is smaller than 28.5 dB, start by decreasing the voltage swing in accordance with the difference between the end-to-end channel insertion-loss at 12.8 GHz and 28.5 dB. If this is insufficient, adjust the transmitter PJ magnitude on top until the target operating margin is obtained.

Figure 3-37. End-to-End Channel for Operating Margin Evaluation

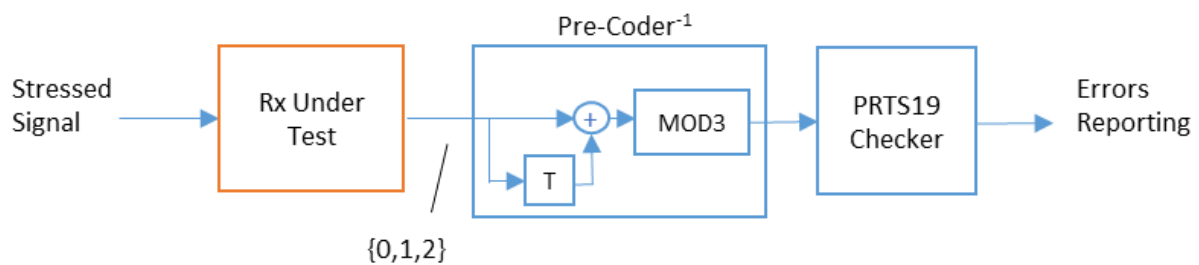


The Pattern-Generator shall support PRBS11, PRTS7 and PRTS19 patterns which may be transmitted with or without pre-coding applied to the data, as described in Section 4.3.2.8. Tunable 4-tap FIR shall be supported at the Pattern-Generator's output, aligned with the transmitter equalization Presets defined in Table 3-24.

The Pattern-Generator shall be initially configured to transmit PRBS11 pattern at 25.6 GB with stressed electrical conditions as described in Table 3-27, and without applying SSC down-spreading. As soon as the receiver under test completes its training with the PRBS11 pattern, it shall indicate to the Pattern-Generator through the SBU protocol to switch to transmit PRTS7 training pattern. The switching from PRBS11 to PRTS7 is asynchronous and needs to be performed in a glitch-free manner while maintaining the same jitter and noise settings. The Pattern-Generator Preset configuration may be adjusted by the receiver under test through the SBU protocol during the training phase when PRBS11 or PRTS7 are transmitted. As soon as the receiver under test completes the training with the PRTS7 signal, it shall indicate to the Pattern-Generator to switch to PRTS19 with pre-coding enabled and activate SSC down-spreading of 3400ppm in "Case 1" setup and 3000ppm in "Case 2a" and "Case 2b" setups. The switching of the pattern is asynchronous and needs to be performed in a glitch-free manner and while maintaining the same jitter and noise settings. The SSC activation shall be done in a glitch-free manner such that the SSC modulation profile starts from the transmitter's initial frequency.

At this point, steady state operation is obtained and the received trits shall be compared against reference PRTS19 LFSR after applying an inverse pre-coding operation, as illustrated in Figure 3-38. Since the pre-coding removes bursts of errors but leaves two single errors at the beginning and at the end of the burst, the Trit Errors count of the PRTS19 checker shall be divided by two in order to obtain the correct Trit Error Ratio computation, which corresponds to the random Trit Errors.

Figure 3-38. Gen 4 Trit Errors Reporting



Note: The receivers within a USB4 Port are tested one at a time. Therefore, if an Asymmetric Link with 3 receivers is supported by the Router Assembly, then Rx2 is tested without having a signal present at the input of Rx0.

3.2.5 Gen 4 Captive Device Compliance

Because a Captive Device has a cable permanently attached, it requires some adjustments in its compliance testing. This section defines the modifications to the Router Assembly compliance testing that apply to Captive Devices.

3.2.5.1 Captive Device Electrical Compliance Methodology

The compliance test setup for a Captive Device requires connecting a Compliance Receptacle to the Captive Device's connector, as shown in Figure 3-20. See Section 3.2.2.4.2 for more information on the Gen 4 Compliance Receptacle.

Reference equalization shall be applied on the Captive Device transmitter measurements performed at the TP3 compliance point. The reference equalization function is based on parametric Continuous-Time-Linear-Equalizer (CTLE), which shall be added on top of the equalization Preset applied by the Captive Device transmitter. The following equation describes the frequency response for the reference CTLE that shall be used for compliance testing:

$$H(s) = \frac{s + A_{DC} \cdot \omega_{p1}}{s + \omega_{p1}}$$

where:

- A_{DC} is the DC gain
- $\omega_{p1} = 2 \cdot \pi \cdot 4e9 \frac{rad}{sec}$

Different CTLE configurations shall be applied such that A_{DC} is one of $\{10^{\frac{-x}{20}} : x = 0, 1, \dots, 10 [dB]\}$.

The default equalization Preset shall be configured to the setting providing the lowest Data Dependent Jitter (DDJ) when combined with the reference equalization function.

3.2.5.2 Captive Device Transmitter Specifications

Transmitter compliance testing for a Captive Device is defined at the output of a Compliance Receptacle fixture referenced to TP3.

Table 3-28 defines the transmitter parameters that shall apply for Gen 4 mode of operation. During all tests, except when measuring the electrical-idle output voltage, the transmitter under test shall send PRTS7 pattern and the neighboring transmitters shall transmit PRTS19 pattern.

Table 3-28. Captive Device Transmitter Specifications for Gen 4 (at TP3)

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	39.0508	39.0742	ps	Corresponding to the Gen 4 baseline Baud rate of 25.6GB with an uncertainty range of -300 ppm to 300 ppm. See Notes 1, 2.
V_SWING	Peak differential voltage swing	410	545	mV	See Notes 9, 10
TX_LEVELS_MISMATCH	Levels separation mismatch ratio	0.975	--	--	See Note 9 and Section 3.2.3.3.
TX_SNR	Signal to Noise and Distortion Ratio	32.5	--	dB	See Note 9 and Section 3.2.3.4.
PULSE_PEAK_NORM	Normalized peak voltage of the linear-fit pulse response	-19	--	dB	See Note 9 and Section 3.2.5.2.1.
TX_ISI_MARGIN_CD	Signal to Residual ISI Ratio	--	--	dB	See Note 9 and Section 3.2.5.2.1.
TX_EQ	Transmitter Equalization Settings	--	--	--	See Section 3.2.3.8.
AC_CM	AC Common Mode voltage	--	100	mV pp	
V_ELEC_IDLE	Peak voltage when the transmitter is in electrical-idle	--	20	mV	See Note 3.
TX_INIT_FREQ	Initial non-modulated transmitter frequency applied during training before enabling the SSC modulation	-300	300	ppm	See Notes 1 and 4, Sections 3.2.3.10, and Figure 3-34.
DELTA_FREQ_200ns	Frequency variation during Link training over 200 ns measurement windows	--	600	ppm	See Note 1, Section 3.2.3.10 and Figure 3-34.

Symbol	Description	Min	Max	Units	Comments
DELTA_FREQ_1000ns	Frequency variation during Link training over 1 μ s measurement windows	--	900	ppm	See Note 1, Section 3.2.3.10 and Figure 3-34.
FREQ_OVERSHOOT	Maximum transient frequency offset from the Link baseline rate, including the clock source accuracy, dynamic clock switching effects and frequency variations induced by low frequency jitter	--	600	ppm	See Note 1, Section 3.2.3.10 and Figure 3-34.
SSC_DOWN_SPREAD_RANGE	Dynamic range of the SSC down-spreading	0.2	0.3	%	See Notes 1, 5 and 9, Sections 3.2.3.10, and Figure 3-34.
SSC_DOWN_SPREAD_RATE	SSC down-spreading modulation rate	30	33	KHz	See Notes 1, 6 and 9, Sections 3.2.3.10, and Figure 3-34.
SSC_PHASE_DEVIATION	Phase jitter associated with the SSC modulation	2.5	15.5	ns pp	See Notes 1 and 9, Sections 3.2.3.10, and Figure 3-34.
SSC_SLEW_RATE	SSC modulation frequency slew rate (df/dt)	--	500	ppm/ μ s	See Notes 1, 7 and 9, Sections 3.2.3.10, and Figure 3-34.
UJ	Sum of uncorrelated DJ and RJ components	--	0.17	UI pp	The RJ shall be extrapolated to 1E-8 statistics. See Note 9 and Section 3.2.3.9.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.075	UI pp	See Note 9 and Section 3.2.3.9.
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	--	0.03	UI pp	See Notes 8, 9 and Section 3.2.3.9.
EVEN_ODD	Difference between the mean jitter of symbols associated with even and odd indexes	--	0.02	UI pp	See Note 9 and Section 3.2.3.9.
LANE_TO_LANE_SKEW	Skew between any two transmit signals of the same USB4 Port	--	44	ns	
RF_INTERFERENCE	Conducted Energy in Wireless Bands	--	--	--	Relevant for Captive Devices with Active tethered cable. See Section 3.1.5.2.1.
V_TX_DC_AC_CONN	Instantaneous single-ended voltage limit at TP3 during transmitter activation and de-activation	-0.5 (min1) -0.3 (min2)	1.0	V	See Note 11.

Symbol	Description	Min	Max	Units	Comments
Notes:					
1.	Shall be extracted from the signal's phase after applying a 2nd order low-pass filter with 3 dB point at 6 MHz.				
2.	Shall be calculated after applying a uniform moving average filter with window size of 7500 trits over the instantaneous UI measurements.				
3.	Shall be extracted after applying first order low-pass filter with 3 dB point at 1.25 GHz.				
4.	Low frequency jitter variations shall be filtered out by averaging the extracted frequency variation waveform over a window of at least 30 μ s.				
5.	Shall be extracted from the transmitted signal phase and calculated as the difference of the maximum and minimum modulated frequencies.				
6.	Shall be extracted from the transmitted signal phase and calculated based on the average time interval between the frequency peaks.				
7.	Shall be extracted from the transmitted signal phase and calculated over measurement intervals of 0.5 μ s. Jitter induced variations shall be filtered out during this measurement.				
8.	Shall be calculated while applying 2 nd order Low-Pass-Filter with 3 dB cut-off at 0.3 MHz on the measured jitter. This filter shall be applied on top of the reference jitter transfer function described in Section 3.2.2.2.				
9.	The equalization shall be set to the combination of transmitter Preset and reference CTLE setting that obtains the lowest Data Dependent Jitter (DDJ) at TP3.				
10.	V_SWING shall be first extracted according to Section 3.2.3.2 and then be normalized by the reference CTLE DC gain A _{DC} as described in Section 3.2.5.1.				
11.	This requirement applies to all Link states and during power-on, power-off, and transitions between Asymmetrical and Symmetrical Links. (min1, max) is measured with a 200 K Ω receiver load, and (min2, max) is measured with a 50 Ω receiver load. The ground offset between a DFP and UFP does not contribute to V_TX_DC_AC_CONN.				

3.2.5.2.1 Linear Fit Pulse Peak and Transmitter ISI Margin

The Captive-Device normalized pulse peak voltage (PULSE_PEAK_NORM) and transmitter ISI margin (TX_ISI_MARGIN_CD) shall be calculated using the equalized linear fit pulse response as follows:

1. Configure the transmitter equalization to the default Preset, which obtains the lowest data dependent jitter (DDJ) when combined with the reference CTLE described in section 3.2.5.1. Send PRTS7 pattern and capture the signal at the TP3 measurement point.
2. Apply the reference CDR function as defined in Section 3.2.2.2.
3. Extract the linear fit pulse response $p(n)$ as described in Section 3.2.3.1.
4. Calculate the Signal term by integrating the linear fit pulse response samples over 1 UI window around the peak of the pulse. Define the PULSE_PEAK_NORM as the average voltage around the peak normalized by the maximum peak voltage of 500 mV:

$$Signal = \sum_{n_{pk}-0.5 \cdot M}^{n_{pk}+0.5 \cdot M-1} p(n)$$

$$PULSE_PEAK_NORM = dB \left(\frac{\frac{1}{M} \cdot Signal}{0.5} \right)$$

where:

- n_{pk} is the linear fit pulse response peak index.
- M is the oversampling ratio, as defined in Table 3-23.

5. Calculate the TX_ISI_MARGIN_CD as the ratio between the integrated signal term and the sum of the 18 largest post-cursor ISI samples, from tap 13 and above:

$$TX_ISI_MARGIN_CD = dB \left(\frac{Signal}{\sum_{i=1}^{18} Sorted_ISI[i]} \right)$$

where:

- Sorted_ISI is a descending order sorted version of the Post_Cursor_ISI vector:

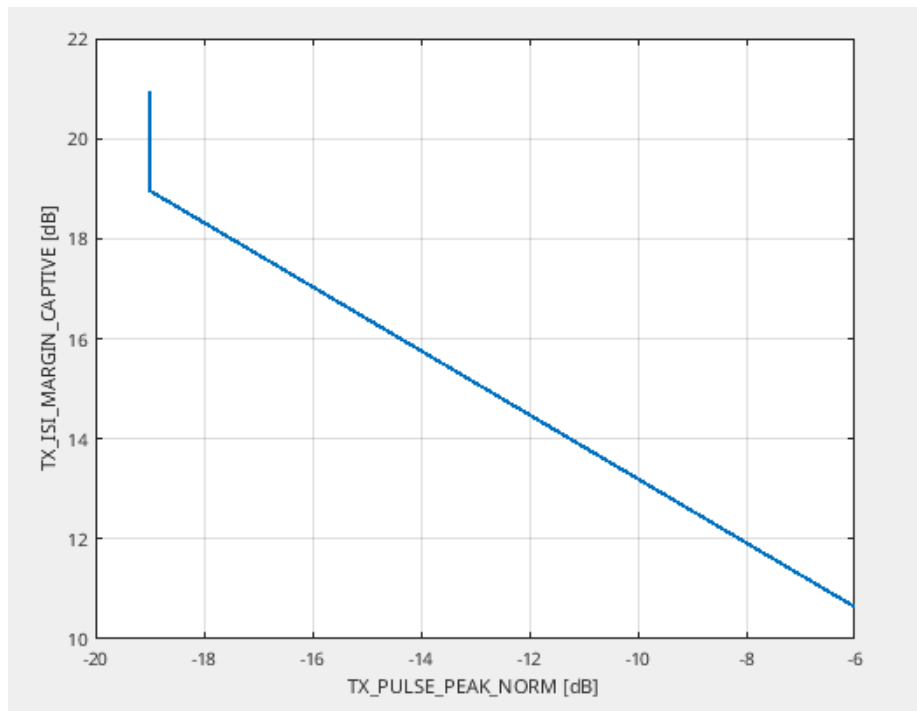
$$Post_Cursor_ISI[j] = \sum_{n_{pk}+(11.5+j) \cdot M}^{n_{pk}+(12.5+j) \cdot M} |p(n)|, \quad j = 1, 2, \dots, N_{post} - 13$$

- n_{pk} is the linear fit pulse response peak index.
- M and N_{post} are the oversampling ratio and the number of post-cursor taps, respectively, as defined in Table 3-23.

The minimum limit of TX_ISI_MARGIN_CD is specified as a function of PULSE_PEAK_NORM as follows:

$$TX_ISI_MARGIN_CD \geq -0.64 \times PULSE_PEAK_NORM + 6.8$$

Figure 3-39. TX_ISI_MARGIN_CD minimum limit as a function of PULSE_PEAK_NORM



3.2.5.3 Captive Device Receiver Specifications**3.2.5.3.1 Summary of Receiver Specifications**

Table 3-29 defines the receiver parameters.

Table 3-29. Captive-Device Receiver Specifications

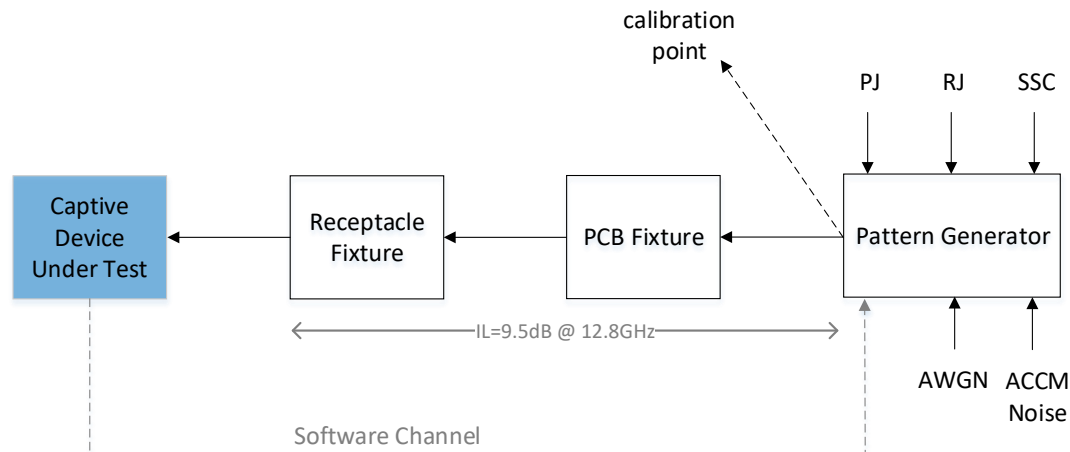
Symbol	Description	Min	Max	Units	Comments
RX_TOLERANCE	Receiver tolerance testing	--	--	--	See Section 3.2.5.3.2
LANE_TO_LANE_SKEW	Skew between incoming signals of the same Port at TP2 (tethered cable input)	--	26	ns	
V_MAX	Input signal peak differential voltage tolerance at TP2 (tethered cable input)	--	600	mV	See Note 3.
RX_INIT_FREQ_VARIATION	Initial non-modulated signal frequency applied during training	-300	300	ppm	See Notes 1, 2, Section 3.2.3.10 and Figure 3-34.
RX_DELTA_FREQ_200ns	Incoming signal's frequency variation during Link training over 200 ns measurement windows	--	600	ppm	See Note 1, Section 3.2.3.10 and Figure 3-34.
RX_DELTA_FREQ_1000ns	Incoming signal's frequency variation during Link training over 1 μ s measurement windows	--	900	ppm	See Note 1, Section 3.2.3.10 and Figure 3-34.
RX_FREQ_OVERSHOOT	Incoming signal's maximum frequency offset from the Link baseline rate during training	--	600	ppm	See Note 1, Section 3.2.3.10 and Figure 3-34.
Notes: 1. Extracted while applying a 2nd order low-pass filter with 3 dB point at 6 MHz over the signal phase. 2. RX_INIT_FREQ_VARIATION corresponds to the frequency offset from 25.6 GB, without including low frequency jitter induced variations. 3. V_MAX defines the differential steady-state input voltage. Limits for the transient single-ended voltage generated by the far-end transmitter are specified in Table 3-28. To avoid voltage overstress, receiver termination should be continuously enabled when the receiver is operational.					

3.2.5.3.2 Receiver Tolerance Testing

The ability of a Captive Device Receiver to tolerate the worst-case incoming signal is examined using a stressed receiver test. A Gen 4 receiver shall operate at a Trit Error Ratio (TER) of 1E-8 or lower without Forward Error Correction when a stressed signal is driven at its input.

A Gen 4 Captive Device shall be able to reliably receive the stressed input signals specified in Table 3-30 and operate with Trit-Error-Ratio of 1E-8 or lower, without Forward Error Correction.

The Captive Device Receiver test setup is shown in Figure 3-40.

Figure 3-40. Captive Device Receiver Test Setup**Table 3-30. Stressed Signal for Gen 4 Captive Device Receiver Compliance Testing**

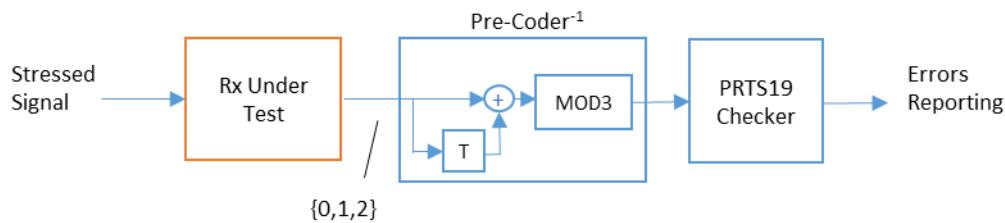
Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
820	32.5	0.975	100	0.075	0.0085

A receiver shall be tested by injecting several different periodic jitter (PJ) components, one at a time. The testing shall include jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. All the specified jitter values shall be calibrated while applying the reference CDR defined in Section 3.2.2.2.

The Pattern-Generator shall support PRBS11, PRTS7 and PRTS19 patterns, which may be transmitted with or without pre-coding applied to the data as described in Section 4.3.2.8. Tunable 4-tap FIR shall be supported at the Pattern-Generator's output, aligned with the transmitter equalization Presets defined in Table 3-24.

The Pattern-Generator shall be initially configured to transmit PRBS11 pattern at 25.6 GB with stressed electrical conditions as described in Table 3-30, without applying SSC down-spreading. As soon as the receiver under test completes its training with the PRBS11 pattern, it shall indicate to the Pattern-Generator, using the SBU protocol, to switch to transmit PRTS7 training pattern. The switch from PRBS11 to PRTS7 is asynchronous and needs to be performed in a glitch-free manner while maintaining the same jitter and noise settings. The Pattern-Generator Preset configuration may be adjusted by the receiver under test using the SBU protocol during the training phase when PRBS11 or PRTS7 are transmitted. As soon as the receiver under test completes the training with the PRTS7 signal, it shall indicate to the Pattern-Generator to switch to PRTS19 with pre-coding enabled and activate SSC down-spreading of 3000 ppm. The switching of the pattern is asynchronous and needs to be performed in a glitch-free manner while maintaining the same jitter and noise settings. The SSC activation shall be done in a glitch-free manner such that the SSC modulation profile starts from the transmitter's initial frequency.

At this point, steady state operation is obtained and the received trits shall be compared against the reference PRTS19 LFSR after applying an inverse pre-coding operation, as shown in Figure 3-41. Since the pre-coding removes bursts of errors but leaves two single errors at the beginning and at the end of the burst, the Trit Errors count of the PRTS19 checker shall be divided by two in order to obtain the correct Trit Error Ratio computation, which corresponds to the random Trit Errors.

Figure 3-41. Gen 4 Trit Errors Reporting for Captive-Devices

Note: The receivers within a USB4 Port are tested one at a time. Therefore, if an Asymmetric Link with 3 receivers is supported by the Router Assembly, then Rx2 is tested without having a signal present at the input of Rx0.

3.2.6 Gen 4 Testability

3.2.6.1 Receiver FEC Symbol Error Ratio Measurement

3.2.6.1.1 Background

All USB4 Gen 4 Ports shall support the FEC Symbol Error Ratio Measurement as defined in this section. A receiver shall support the ability to directly count the number of Pre-FEC symbol errors that occur per FEC block at the Port level. FEC Symbol Error Ratio Measurement is performed while the Link is Active to verify or monitor Link performance and to aid in debug.

Section 8.3.2.3.3 defines the Operations that are used to configure FEC Symbol Error Ratio Measurement, run a FEC Symbol Error Ratio Measurement, and get FEC Symbol Error Ratio Measurement results.

3.2.6.1.2 FEC Symbol Error Ratio Measurement Requirements

A USB4 Port that supports Gen 4 speed implements the following to measure the FEC Symbol Error Ratio while the Link is Active:

- 14 counters per USB4 Port to count the number of errors that occur per FEC block (13 counters that increment based on the occurrence of 0-12 errors and 1 counter that increments on the occurrence of an uncorrectable error). Based on the values of these counters, the cumulative FEC Symbol Error Ratio can be calculated.
- The capability to count the number of FEC blocks that have been transacted.
- The ability to start, stop, and clear the counters.
- Counter depths that are sufficient to measure FEC Symbols Error Ratio to three orders or magnitude below the FEC error rate target of 1E-7 (which corresponds to Trit Error Ratio of 1E-8) at a 95% confidence limit.

See Section 8.3.2.3.3 for more details.

3.2.6.2 Receiver Lane Margining

3.2.6.2.1 Background

All Gen 4 Ports shall support the Lane margining requirements defined in this section. Receiver Lane margining provides a means to assess end-to-end Link performance, enables the validation of Links that use Re-timers or device-down topologies (i.e. do not have a connector that can be used for compliance testing), and enables a standard method for margining systems in production or in the field. Receiver Lane margining is performed while the Link is Active. This allows derivation of the Link electrical performance that would be experienced by the end user.

The receiver Lane margin values and error counts described in this section are not designed to determine compliance for any component. Rather, Receiver Lane margining standardizes

methods already in use by many component and system manufacturers to determine a subjective measure of Link robustness.

A Gen 4 Port shall support either the hardware (HW) Lane margining mode or the software (SW) Lane margining mode for voltage margining. A Gen 4 Port may optionally support both SW and HW Lane margining modes.

Section 8.3.2.4.1 defines the Operations that are used to obtain receiver Lane margining capabilities, configure margining parameters, run a margining test, and get margining results.

3.2.6.2.2 Receiver Voltage Margining and Timing Margining Requirements

All receivers on a Gen 4 Link shall support voltage margining whereby a receiver sampler is offset from the nominal sampling position in the voltage (vertical) dimension separately for both the upper and lower eyes of the PAM3 signal. Independent voltage margining in the positive (high) and negative (low) directions is required. A USB4 Port shall be capable of performing voltage margining for each Lane independently. Voltage margining shall be non-destructive (i.e. not introduce actual bit errors on the Link). Voltage margining can be implemented using a monitor sampler that is offset from the nominal sample position while the data sampler remains at the nominal position. A receiver shall use the range and step size in Table 3-31 for voltage margining.

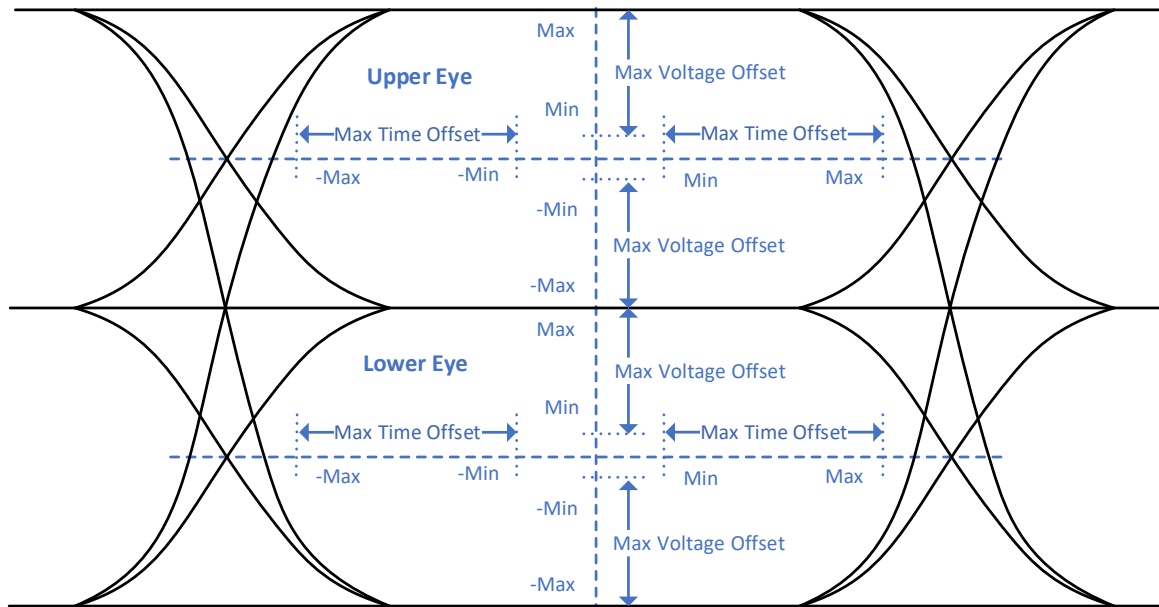
All receivers on a Gen 4 Link may optionally support timing margining whereby a receiver sampler is offset from the nominal sampling position in the timing (horizontal) dimension separately for both the upper and lower eyes of the PAM3 signal. Independent margining in the positive (right) and negative (left) directions is optional but recommended. A USB4 Port that supports timing margining shall be capable of performing timing margining for each Lane independently. The timing margining may be destructive (i.e. cause actual bit errors in the Link). Timing margining can be implemented using a jitter injection circuit to inject jitter onto the Rx sampling clock to offset the data sampler from the nominal position. A receiver shall use the range and step size in Table 3-31 for timing margining.

Table 3-31. Gen 4 RX Margining Voltage and Timing Requirements

Parameter	Min	Max	Units
Voltage Margin Range	+/- 74/2	+/- 200/2	mV
Voltage Margining Step Size	Note 1	3/2	mV
Voltage Margining Steps (per direction)	Note 2	127	--
Timing Margining Range	+/- 0.2	+/- 0.5	UI
Timing Margining Step Size (per direction)	Note 3	0.03	UI
Timing Margining Steps (per direction)	Note 4	31	--

Notes:

1. The minimum Voltage Margining Step Size is bounded by $\text{Min}(\text{Voltage Margin Range})/\text{Max}(\text{Voltage Margining Steps})$.
2. The minimum Voltage Margining Steps (per direction) is bounded by $\text{ceiling}(\text{Min}(\text{Voltage Margin Range})/\text{Max}(\text{Voltage Margin Step Size}))$.
3. The minimum Timing Margining Step Size is bounded by $\text{Min}(\text{Timing Margining Range})/\text{Max}(\text{Timing Margining Steps})$.
4. The minimum Timing Margining Steps (per direction) is bounded by $\text{ceiling}(\text{Min}(\text{Timing Margin Range})/\text{Max}(\text{Timing Margin Step Size}))$.

Figure 3-42. Gen 4 RX Margining Range Requirements

The purpose of timing margining is to measure the actual timing margin seen by the receiver when operating in a fully functional mode. Therefore, when performing timing margining, it is recommended that all RX adaptive circuitry be enabled and operating in a closed loop manner.

3.2.6.3 Receiver Parameter Access (Informative)

It is recommended that the receiver training parameters be accessible to system software to enable a system integrator with greater visibility into the operation of the receiver. This allows a system integrator to observe the stability and performance of the Link and provides an aid for debug. The receiver training parameters may be accessible from the vendor specific address range within the SB Register Space. The number and type of parameter values is implementation specific. The system integrator needs to work directly with the receiver IP vendor to understand how to interpret the stored receiver parameters.

3.3 Sideband Channel Electrical Specifications

The Sideband Channel shall operate at 1 Mbps rate. A Router Assembly shall meet the Sideband Channel requirements defined in Table 3-32.

Table 3-32. SBTX and SBRX Specifications

Symbol	Description	Min	Max	Units	Conditions
SBTX _{VOH}	SBTX High Voltage	2.4	3.47 (max1) 3.52 (max2)	Volts	See Note 1 and Note 2.
SBTX _{VOL}	SBTX Low Voltage	-0.05	0.4	Volts	See Note 1 and Note 2.
SBRX _{VIH}	SBRX High Voltage Detection	2.0	3.72 (max1) 3.77 (max2)	Volts	See Note 1 and Note 2.
SBRX _{VIL}	SBRX Low Voltage Detection	-0.3	0.65	Volts	See Note 2.
SBRX _{IIH}	SBRX High input current	--	25	μA	V _{in} = 3.3 V. See Note 3.
SBRX _{IL}	SBRX Low input current	--	0.4	μA	V _{in} = 0 V. See Note 4.

Symbol	Description	Min	Max	Units	Conditions
SBX _{TRTF}	SBTX/SBRX 10-90% Rise/Fall time	3.5	65	ns	See Note 5.
SBTX _{PULL_UP_RES}	SBTX pull-up resistor	7.0K	10.5K	Ω	See Note 6.
SBRX _{PULL_DOWN_RES}	SBRX pull-down resistor	0.70M	1.05M	Ω	See Note 7.
SBTX _{SOURCE_IMPEDANCE}	SBTX output impedance	25	90	Ω	
SBX_UI	UI duration	970	1030	ns	See Note 8.

Notes:

1. This parameter shall be verified in both transaction and steady state. SBTX_{VOH} and SBRX_{VIH} (min, max1) shall be measured in steady state condition with continuous high level, and (min, max2) shall be measured in transaction mode. Over/undershoot shall be ignored.
2. A buffer may be used between the connector and the SBU transceiver to meet the required voltage levels.
3. Intended to limit the voltage drop on the SBRX input due to current through the SBTX pull-up resistor.
4. Intended to limit the voltage on the SBRX pull-down resistor when the cable is disconnected.
5. Verify this parameter in transaction and not from power down to power up. The minimum is specified to control crosstalk and EMI.
6. A Router shall terminate the SBTX signal to 3.3 V nominal power.
7. A Router shall terminate the SBRX signal to GND.
8. SBX_UI corresponds to the instantaneous period of the SBU signal and not to the average period and shall be measured over the SBTX signal. The SBU receiver design is expected to operate properly with the worst-case incoming SBX UI and SBX_{TRTF} and while considering the SBU receiver loading.

3.4 Low Frequency Periodic Signaling (LFPS)

Low frequency periodic signaling (LFPS) is used for in-band communication between two Link Partners when exiting power management Link states.

3.4.1 LFPS Signal Definition

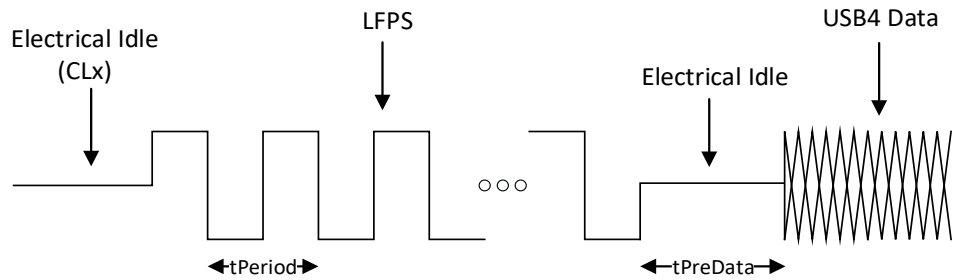
The following table defines the LFPS electrical specification.

Table 3-33. LFPS Electrical Specifications

Symbol	Description	Min	Max	Units	Comments
tPeriod	Period of LFPS cycle (clock pattern)	20	80	ns	
tPreData	Period of time in which electrical-idle shall be set after the LFPS sequence	80	120	ns	See Figure 3-43.
V_CM_AC_LFPS	Common mode noise	--	100	mV pk-pk	
V_TX_DIFF_PP_LFPS	LFPS peak-to-peak differential amplitude	800	1200	mV pk-pk	
V_LFPS_RX_DETECT_TH	LFPS RX detect threshold	100	300	mV pk-pk	Signal shall be rejected below minimum level and shall be accepted above maximum level.
tRiseFall	Rise/Fall time of LFPS signal, measured from 20% to 80% of the signal dynamic range	--	4	ns	

Symbol	Description	Min	Max	Units	Comments
LFPS_DUTY_CYCLE	Duty-Cycle of LFPS signal	45	55	%	Applies for all the LFPS cycles including the first and the last, which should not be cut in the middle.

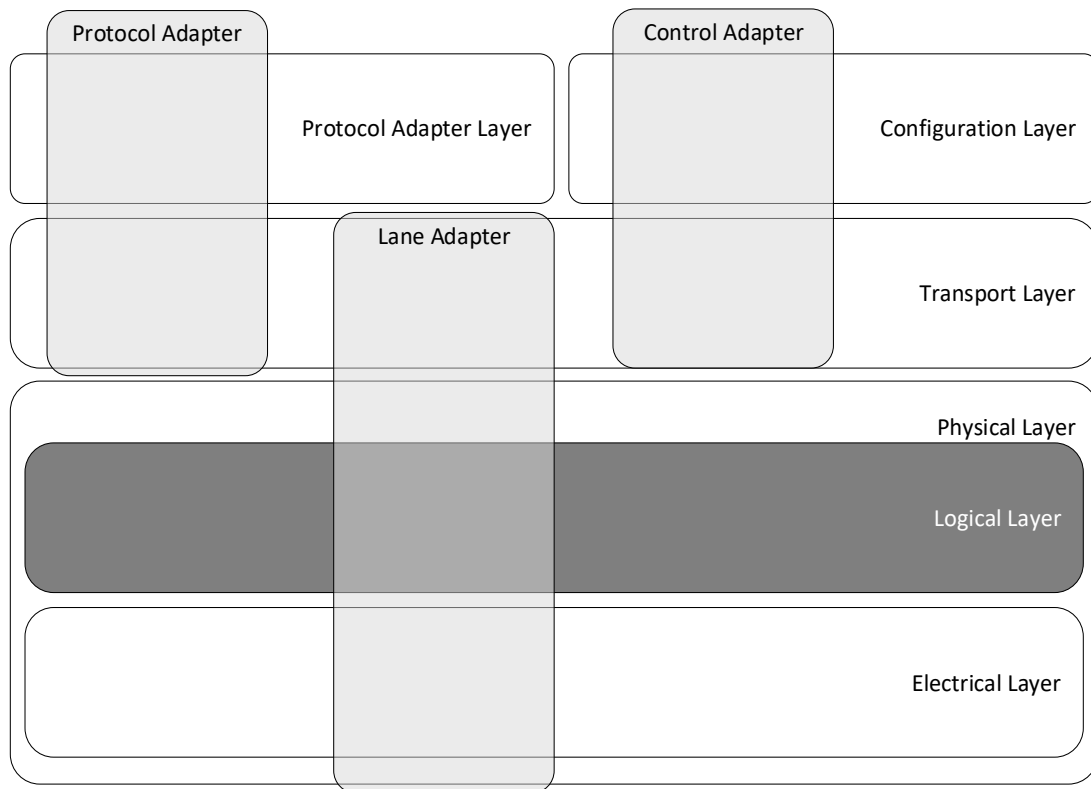
Figure 3-43. Signaling During Power Management State Exit



IMPLEMENTATION NOTE

Typical implementations for transitioning from LFPS to USB3 Data might not be suitable for USB4. Such implementations can have an uncertainty of up to LFPS t_{Period} max (80 ns) for the actual duration of LFPS signaling. This uncertainty would not allow generation of $t_{PreData}$ (electrical idle) with a duration of 80 ns – 120 ns. It is implementation specific how to transition from LFPS via electrical idle to USB4 Data as shown in Figure 3-43.

4 Logical Layer

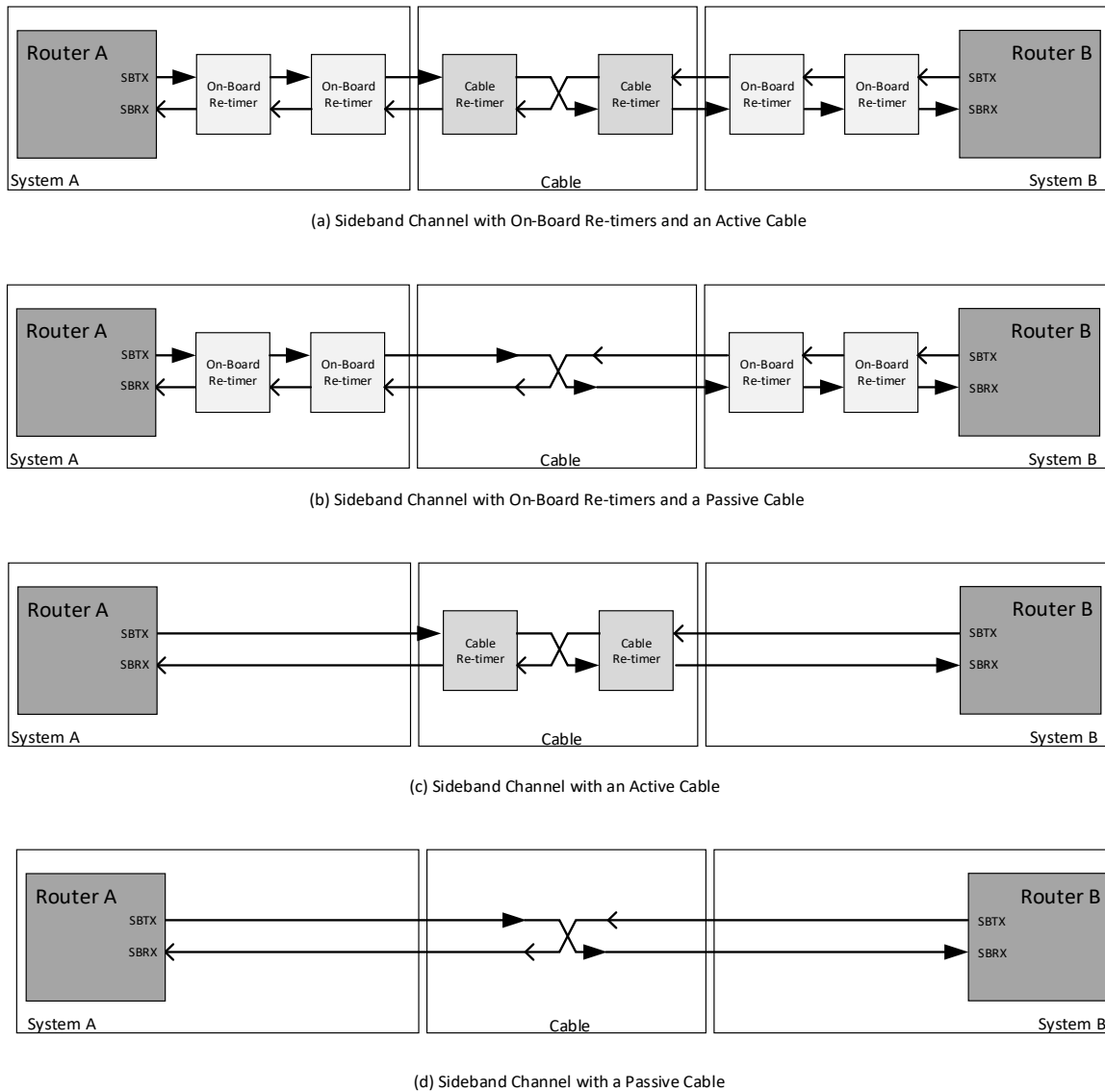


4.1 Sideband Channel

Transactions are sent over the SBTX wire and received over the SBRX wire defined in Section 3.3.

Figure 4-1 depicts several examples of SBTX and SBRX connectivity between two Routers using On-Board Re-timers, and Passive or Active Cables.

A Router may support a maximum of two On-Board Re-timers between it and the cable.

Figure 4-1. Cable Topologies (Informative)**4.1.1 Transactions****4.1.1.1 Symbols**

A Sideband Channel shall encode all transmitted Symbols using the 10-bit Start/Stop encoding scheme as follows:

- A Start bit (logical 0b).
- Eight bits of payload.
- A Stop bit (logical 1b).

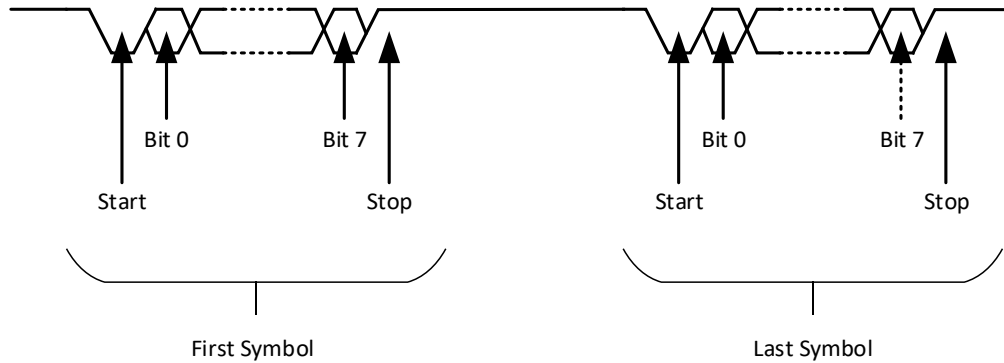
4.1.1.2 Transaction Types

Transactions are carried over the Sideband Channel in one of the following Transaction types:

- Link Type (LT).
- Extended Link Type (ELT).
- Administrative Type (AT).
- Re-timer Type (RT).

The symbols within a Transaction shall be sent in ascending order. The bits within a symbol shall be sent in the order from bit 0 to bit 7. Figure 4-2 illustrates this ordering.

Figure 4-2. Symbol and Bit Order on Sideband Channel



An inter-Symbol gap between Symbols of the same Transaction shall be within $t_{SBInterSymbolGap}$ time.

Table 4-1 describes how a Router shall handle reserved values and fields in Sideband Transactions.

Table 4-1. Sideband Transactions Reserved Value and Field Handling

Type	Handling
Reserved value	The originator of a Transaction shall not use a value that is marked as "Reserved". The target of a Transaction shall ignore the Transaction if any of its defined fields are set to a "Reserved" value..
Reserved field	The originator of a Transaction shall set a field that is marked "Reserved" to zero. The target of a Transaction shall ignore any fields that are marked "Reserved".

4.1.1.2.1 LT Transactions

LT Transactions are used during Lane Initialization. They are also used to signal a change in Adapter state due to events such as a Lane disconnect or transition to a Low Power state. An LT Transaction shall consist of the three Symbols described in Table 4-2.

Table 4-2. LT Transaction Format

Byte	Payload Value	Description
0	FEh	Data Link Escape (DLE) Symbol – indicates the beginning of a Transaction.
1	See Table 4-3	Lane State Event (LSE) – identifies a change in originator's state or in the Adapter state.
2	Bitwise complement of LSE	Complement LSE (CLSE)

Table 4-3. LSE Symbol

Bits	Name	Function
[2:0]	<i>LSESymbol</i>	This field defines the LT Transaction type. Undefined values are Rsvd. 000b – LT_Fall (Lane Disable event) 010b – LT_Resume (USB4® Port started USB4 transmission) 011b – LT_LRoff (disconnect or system sleep state) 100b – LT_SwitchRx2Tx (Asymmetric flow) 111b – LT_SwitchAck (Asymmetric flow)
[3]	<i>ELT</i>	Shall be set to 0b.
[4]	<i>Rsvd</i>	Reserved
[5]	<i>LSELane</i>	Indicates the Lane affected by this Transaction. Shall be 0b (for Lane 0) or 1b (for Lane 1). Shall be set to 0b when issuing an LT_LRoff Transaction. Shall be set to 1b when issuing an LT_SwitchRx2Tx or LT_SwitchAck Transaction.
[7:6]	<i>StartLT</i>	Identifies that this is an LT Transaction. Shall be set to 10b.

The recipient of an LT Transaction shall verify that the CLSE Symbol payload is a bitwise complement of the LSE Symbol payload. An LT Transaction that fails this check shall be dropped and no further action shall be taken on its behalf.

4.1.1.2.2 Extended LT (ELT) Transactions

A Router or Re-timer sends an ELT Transaction to other Routers and Re-timers. An ELT Transaction shall consist of the three Symbols described in Table 4-4.

Table 4-4. ELT Transaction Format

Byte	Payload Value	Description
0	FEh	Data Link Escape (DLE) Symbol – indicates the beginning of a Transaction.
1	See Table 4-5	Extended Lane State Event (ELSE) – identifies a change in originator's state or in the Adapter state.
2	Bitwise complement of ELSE	Complement ELSE (CELSE)

Table 4-5. ELSE Symbol

Bits	Name	Function
[2:0]	<i>Rsvd</i>	Reserved
3	<i>ELT</i>	Shall be set to 1b.
[5:4]	<i>ELTtype</i>	This field defines the ELT Transaction type. 00b – ELT_OpDone (Port Operation Complete) 10b – ELT_Recovery (Gen 4 Link Recovery Initiation/Completion) All other values are Rsvd.
[7:6]	<i>StartLT</i>	Identifies that this is an ELT Transaction. Shall be set to 10b.

The recipient of an ELT Transaction shall verify that the CELSE Symbol payload is a bitwise complement of the ELSE Symbol payload. An ELT Transaction that fails this check shall be dropped and no further action shall be taken on its behalf.

4.1.1.2.3 AT Transactions

There are two types of AT Transactions:

- AT Commands – used to read from or write to SB Register Space of a Router.
- AT Responses – used to respond to an AT Command.

An AT Transaction shall consist of the Symbols in Table 4-6.

Table 4-6. AT Transaction Format

Byte	Payload Value	Description
0	FEh	Data Link Escape (DLE) Symbol – indicates the beginning of a Transaction.
1	See Table 4-7	Start Transaction (STX) Symbol – defines the operation of the Transaction.
[n+1:2]	See Section 4.1.1.3	Data Symbols – the number of Data Symbols is not explicitly defined and is inferred from the end-of-Transaction delimiters (DLE-ETX). The number of Data Symbols (n) shall not exceed 66.
n+2	Low-order byte of 16-bit CRC	Low CRC (LCRC) Symbol
n+3	High-order byte of 16-bit CRC	High CRC (HCRC) Symbol
n+4	FEh	Data Link Escape (DLE) Symbol
n+5	40h	End of Transaction (ETX) Symbol

Table 4-7. STX Symbol for an AT Transaction

Bits	Name	Function
[0]	<i>CmdNotResp</i>	Identifies whether the AT Transaction is an AT Command or an AT Response. Shall be set to 0b for an AT Response or 1b for an AT Command.
[1]	<i>ReturnBounce</i>	Shall be set to 0b.
[2]	<i>Recipient</i>	Identifies the intended final recipient of the Transaction. Shall be set to 1b.
[3]	<i>Bounce</i>	Shall be set to 0b.
[4]	<i>Responder</i>	Shall be set to 0b.
[5]	<i>Rsvd</i>	Reserved.
[7:6]	<i>StartAT</i>	Identifies that this is an AT Transaction. Shall be set to 00b.

A Router that receives an AT Command with the *Recipient* bit set to 1b shall respond with an AT Response.

Note: Only a Router issues AT Transactions. A Re-timer does not issue AT Transactions. See the USB4 Re-Timer Specification for more information.

4.1.1.2.4 RT Transactions

There are two types of RT Transactions:

- RT Command – used by a Router or a Re-timer to communicate with another Router or Re-timer. Can be Broadcast (Section 4.1.1.2.4.1) or Addressed (Section 4.1.1.2.4.2).
- RT Response – used to respond to an RT Command (Addressed RT Transactions only).

4.1.1.2.4.1 Broadcast RT Transactions

A Router sends Broadcast RT Transactions to enumerate the Re-timers along a Link and to propagate Link attributes to Re-timers along a Link. A Broadcast RT Transaction does not cause an RT Response.

A Broadcast RT Transaction shall have the format shown in Table 4-8.

Table 4-8. Broadcast RT Transaction Format

Byte	Payload Value	Description
0	FEh	Data Link Escape (DLE) Symbol – indicates the beginning of a Transaction.
1	See Table 4-9	Start Transaction (STX) Symbol – defines the operation of the Transaction.
3:2	See Table 4-10 and Table 4-11	Link Parameters – contains a list of the Link parameters selected during Lane Initialization.
4	Low-order byte of 16-bit CRC	Low CRC (LCRC) Symbol
5	High-order byte of 16-bit CRC	High CRC (HCRC) Symbol
6	FEh	Data Link Escape (DLE) Symbol
7	40h	End of Transaction (ETX) Symbol

Table 4-9. STX Symbol for a Broadcast RT Transaction

Bits	Name	Function
[7:6]	<i>StartRT</i>	Identifies that this is an RT Transaction. Shall be set to 01b.
[5]	<i>Broadcast</i>	Identifies that this is a Broadcast RT Transaction. Shall be set to 1b.
[4:1]	<i>Index</i>	Index of the transmitting Router or Re-timer. Shall be set to 0.
[0]	<i>CmdNotResp</i>	Identifies whether the RT Transaction is an RT Command or an RT Response. Shall be set to 1b.

Table 4-10. Contents of Byte 2 in a Broadcast RT Transaction

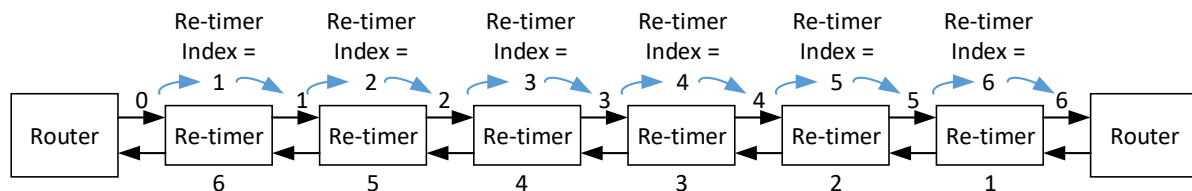
Bits	Name	Function
[7:5]	<i>Rsvd</i>	Reserved
[4]	<i>TBT3-CompatibleSpeed</i>	Set to 0b.
[3]	<i>SSCAwaysOn</i>	For a Gen 2 or Gen 3 Link: Set to 0b when the Router sending the Transaction exits from a CLx state with SSC off. Set to 1b when the Router sending the Transaction always operates with SSC on, including during exit from CLx state. It is recommended that a Router set <i>SSCAwaysOn</i> to 1b. For a Gen 4 Link: Set to 0b. <i>Note: A Re-timer sets this field to 0b before forwarding a Broadcast RT Transaction.</i>
[2]	<i>RS_FEC</i>	Set to 0b when RS-FEC is not enabled on the Link. Set to 1b when RS-FEC is enabled on the Link.
[1]	<i>Rsvd</i>	Reserved
[0]	<i>USB4</i>	Set to 1b.

Table 4-11. Contents of Byte 3 in a Broadcast RT Transaction

Bits	Name	Function
[7:4]	<i>SelectedGen</i>	Indicates the Gen speed selected for operation. 0000b – Reserved 0001b – Gen 2 speed 0010b – Gen 3 speed 0100b – Gen 4 speed Else – Reserved.
[3]	<i>Enable3Tx</i>	Shall be equal to the value of the <i>Asymmetric Decision (Tx)</i> bit in the Link Configuration register of the SB Register Space.
[2]	<i>Enable3Rx</i>	Shall be equal to the value of the <i>Asymmetric Decision (Rx)</i> bit in the Link Configuration register of the SB Register Space.
[1]	<i>Lane1Enabled</i>	Shall equal the value of the <i>Enabling Decision (Lane 1)</i> bit in the Link Configuration register of the SB Register Space (see Section 4.1.1.3).
[0]	<i>Lane0Enabled</i>	Shall equal the value of the <i>Enabling Decision (Lane 0)</i> bit in the Link Configuration register of the SB Register Space (see Section 4.1.1.3).

Note: The above Tables are arranged in a way that MSB is on the top and LSB is on the bottom.

Figure 4-3 depicts an example of how a Broadcast RT Transaction is used to assign indexes to a Link with six Re-timers. In the example, each Re-timer that receives the Broadcast RT Transaction increments the index by one and stores the resulting Re-timer Index locally as its index in the direction of the Broadcast RT Transaction. The Re-timer then sends the Broadcast RT Transaction on its other USB4 Port.

Figure 4-3. Propagation of a Broadcast RT Transaction

Note: Only a Router issues Broadcast RT Transactions. A Re-timer does not issue Broadcast RT Transactions. See the USB4 Re-Timer Specification for more information.

4.1.1.2.4.2 Addressed RT Transactions

A Router uses an Addressed RT Transaction to access the SB Register Space of a Re-timer on the Link. The Router sets the *Index* field in the STX symbol of the Addressed RT Transaction to the Re-timer Index of the target Re-timer.

A Router can also use an Addressed RT Transaction to access the SB Register Space of an adjacent Re-timer or Router during TxFFE negotiation. A Router sets the *Index* field in the STX symbol of the Addressed RT Transaction to 0 to target an adjacent Router or Re-timer.

An Addressed RT Transaction shall have the format shown in Table 4-12.

Table 4-12. Addressed RT Transaction Format

Byte	Payload Value	Description
0	FEh	Data Link Escape (DLE) Symbol – indicates the beginning of a Transaction.
1	See Table 4-13	Start Transaction (STX) Symbol – defines the operation of the Transaction.
[n+1:2]	See Section 4.1.1.3	Data Symbols – a number (n) of Data Symbols. The number of Data Symbols shall not exceed 66. <i>Note: The number of Data Symbols is not explicitly defined and is inferred from the end-of-Transaction delimiters (DLE-ETX).</i>
n+2	Low-order byte of 16-bit CRC	Low CRC (LCRC) Symbol
n+3	High-order byte of 16-bit CRC	High CRC (HCRC) Symbol
n+4	FEh	Data Link Escape (DLE) Symbol
n+5	40h	End of Transaction (ETX) Symbol

Table 4-13. STX Symbol for an Addressed RT Transaction

Bits	Name	Function
[7:6]	<i>StartRT</i>	Identifies that this is an RT Transaction. Shall be set to 01b.
[5]	<i>Broadcast</i>	Shall be set to 0b.
[4:1]	<i>Index</i>	Addressed RT Command: Shall be set to 0 if the target of the Transaction is the first Router or Re-timer that receives the Transaction. Else, shall be set to the Re-timer Index of the Re-timer that is the target of the Command. Addressed RT Response: Shall be set to the value of the <i>Index</i> field in the corresponding Addressed RT Command.
[0]	<i>CmdNotResp</i>	Identifies whether the RT Transaction is an RT Command or an RT Response. Shall be set to 0b for an RT Response or 1b for an RT Command.

A Router that receives an Addressed RT Command with the *Index* field set to 0 shall respond with an Addressed RT Response. A Router shall not respond to Addressed RT Commands with a non-zero *Index* field.

4.1.1.2.5 AT and RT Transaction Rules

A transmitter may abort an AT Transaction or an RT Transaction after sending the first DLE Symbol (in order to send a higher priority LT Transaction), but shall not abort an AT Transaction or an RT Transaction after the STX Symbol is sent. When a receiver receives two or more leading DLE symbols it shall discard the extra leading DLE symbols and process the received LT Transaction as if only one leading DLE symbol was received.

To avoid identifying a pattern of FEh-40h inside the payload as an end-of-Transaction delimiter, if any Data Symbol or a CRC Symbol in an AT Transaction or an RT Transaction contains the same payload as a DLE Symbol, the transmitter of the AT Transaction or RT Transaction shall insert a Symbol with payload of FEh in front of that Data Symbol. The recipient of an AT Transaction or an RT Transaction shall strip all duplicating FEh Symbols that immediately precede a Data Symbol or a CRC Symbol. See also Figure 4-4.

Each AT Transaction or RT Transaction shall include a 16-bit CRC. The 16-bit CRC is broken up into two bytes, which make up the Low CRC and High CRC Symbols described in Table 4-6, Table 4-8, and Table 4-12. The CRC protects the STX and Data Symbols only. Thus, only the STX and

Data Symbols shall be used in CRC calculation. FEh Symbols inserted by the transmitter into the Data Symbols of the Transaction are not CRC protected.

The CRC shall be calculated in increasing Symbol order, starting with the STX Symbol. Within each Symbol, CRC shall be calculated from bit[7] to bit[0]. The CRC shall be calculated using the following rules:

- Width: 16
- Poly: 8005h
- Init: FFFFh
- RefIn: True
- RefOut: True
- XorOut: 0000h

Appendix A provides an example of a CRC calculation.

4.1.1.2.6 AT and RT Command Rules

A Router shall process AT Commands and AT Responses arriving from the Link Partner or Re-timer in the order received. For example, a Router shall respond to a received AT Command before it processes an AT Response that arrived after the AT Command.

A Router shall process Addressed RT Commands and Addressed RT Responses arriving from a Re-timer in the order received. For example, a Router shall respond to a received Addressed RT Command before it processes an Addressed RT Response that arrived after the Addressed RT Command.

Note: A Router may send Commands and Responses in any order so long as timing constraints are met. Thus, when retransmitting a Transaction, a Router may send a Response before reissuing a Command, or it may reissue a Command, then send a Response.

A Router shall not send an AT Command or Addressed RT Command while it is waiting for a response for either a previously sent AT Command or a previously sent Addressed RT Command.

4.1.1.2.6.1 AT Commands

The recipient of an AT Command shall send an AT Response within tCmdResponse of receiving the AT Command. It is recommended that the recipient of an AT Command respond with an AT Response as soon as possible.

If a Router sends an AT Command, then receives at least two AT Commands from the target of the outstanding AT Command within tATTimeout, it shall stop waiting for an AT Response and shall immediately reissue the outstanding AT Command. An example of when this can occur, is when one Router powers up before the other Router.

Otherwise, a Router shall wait tATTimeout for an AT Response and may timeout the outstanding AT Command if an AT Response is not received within tATTimeout. When a timeout occurs, the originator may either resend the AT Command, issue another AT Command, or handle the timeout in an implementation-specific manner.

4.1.1.2.6.2 Addressed RT Commands

The recipient of an Addressed RT Command shall send an Addressed RT Response within tCmdResponse of receiving the Addressed RT Command. It is recommended that the recipient of an Addressed RT Command respond with an Addressed RT Response as soon as possible.

A Router shall wait tRTTimeout for an Addressed RT Response and may timeout the outstanding Addressed RT Command if an Addressed RT Response is not received within tRTTimeout. When a timeout occurs, the originator may either resend the Addressed RT Command, issue another Addressed RT Command, or handle the timeout in an implementation-specific manner.

4.1.1.2.7 Receiver Decoding of LT, ELT, AT, and RT Transactions

Figure 4-4 and Table 4-14 depict the receive state-machine to decode LT, ELT, AT, and RT Transactions over the Sideband Channel. For each entry in the Table, if Condition is met, then Action is taken and the state-machine transitions to Next State.

A Router shall ignore and discard an AT Transaction or an Addressed RT Transaction if any of the following are true:

- The CRC in the Transaction is invalid.
- The Transaction has no data and no *CRC* field.

Any sequence of Symbols not handled as an LT Transaction, an ELT Transaction, an AT Transaction, or an RT Transaction shall be discarded. An AT Response or an RT Response shall not be sent in response to such a sequence.

Figure 4-4. Sideband Channel Receive Transaction State Machine

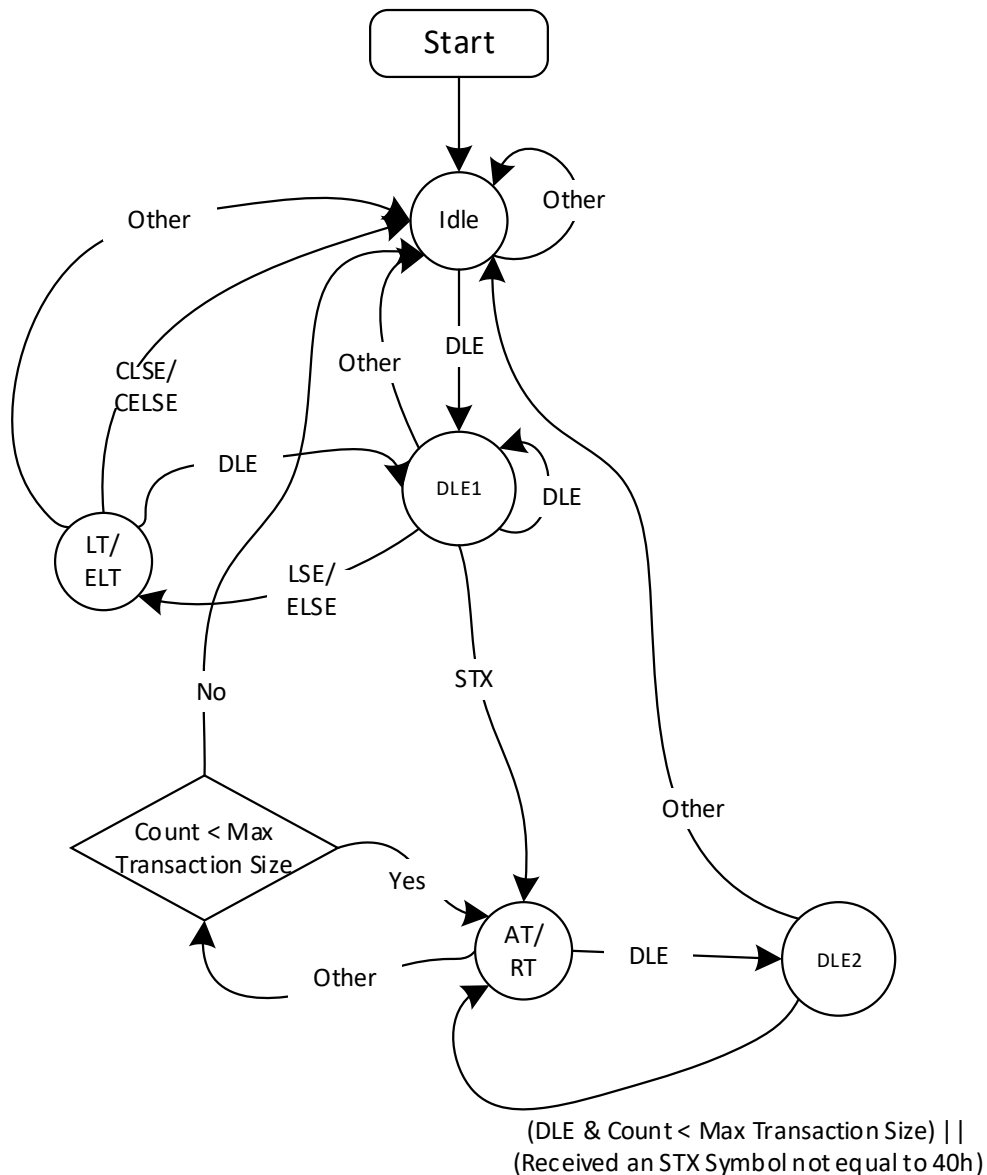


Table 4-14. Sideband Channel Receive Transaction State Machine

Initial State	Next State	Condition	Action
Idle	DLE1	Received a DLE Symbol	--
Idle	Idle	Received other Symbol	--
DLE1	LT/ELT	Received LSE/ELSE Symbol.	Store LSE/ELSE Symbol.
DLE1	DLE1	Received a DLE Symbol.	--
DLE1	AT/RT	Received an STX Symbol.	Initialize <i>Count</i> to 1. Store STX Symbol. Initialize CRC machine and update with STX Symbol.
DLE1	Idle	Received other Symbol.	--
LT/ELT	DLE1	Received a DLE Symbol.	Discard stored LSE/ELSE Symbol.
LT/ELT	Idle	Received CLSE/CELSE Symbol.	Process LT or ELT Transaction. See Section 4.1.1.2.1.
LT/ELT	Idle	Received other Symbol.	Discard stored LSE/ELSE Symbol.
AT/RT	DLE2	Received a DLE Symbol.	--
AT/RT	AT/RT	Received other Symbol AND Count < Max Transaction Size. See Note 1.	Store Symbol. Update CRC. Increment Count.
AT/RT	Idle	Received other Symbol AND Count >= Max Transaction Size. See Note 1.	Discard stored Symbols.
DLE2	AT/RT	Received DLE Symbol AND Count < Max Transaction Size. See Note 1.	Store Symbol. Update CRC. Increment Count.
DLE2	AT/RT	Received an STX Symbol not equal to 40h.	Initialize <i>Count</i> to 1. Store STX Symbol. Initialize CRC machine and update with STX Symbol.
DLE2	Idle	Received an ETX Symbol.	Process AT Transaction or RT Transaction.
DLE2	Idle	Received other Symbol.	Discard stored symbols.
Notes:			
1. Max Transaction Size is 69 Symbols for an AT Transaction or Addressed RT Transaction or 5 Symbols for a Broadcast RT Transaction.			

4.1.1.3 SB Register Space

A Router uses AT Transactions to access the SB Register Space of its Link Partner. A Router uses Addressed RT Transaction to access the SB Register Space of a Re-timer on the Link. Section 4.1.1.3.1 describes how a Router accesses SB Register Space.

A Connection Manager can also initiate an access to the SB Register Space of a Router or Re-timer. Section 4.1.1.3.2 describes how a Connection Manager accesses SB Register Space.

A Router shall maintain one SB Register Space per USB4 Port. Section 4.1.1.3.3 describes the format and contents of SB Register Space.

4.1.1.3.1 Router Access

A Router uses an AT Transaction with an AT Command to access the SB Register Space of its Link Partner. A Router uses an Addressed RT Transaction with an AT Command to access the SB Register Space of a Re-timer on the Link. An AT Command or RT Command shall consist of the Symbols described in Table 4-15.

Table 4-15. AT/RT Command Data Symbols

Symbol	Bits	Name	Function
0	7:0	<i>REG</i>	8-bit address of the register being read from or written to.
1	6:0	<i>LEN</i>	Number of bytes to read/write. Shall not be greater than 64.
1	7	<i>WnR</i>	0b for a Read Command. 1b for a Write Command.
m:2	7:0	COMMAND_DATA	For a Write Command: A sequence of up to 64 bytes to be written. Register contents shall appear least significant byte first. For a Read Command: There is no COMMAND_DATA.

When a Router receives an AT Command it sends an AT Response. When a Re-timer receives an RT Command, it sends an RT Response. An AT Response or RT Response shall consist of the Symbols described in Table 4-16.

Table 4-16. AT/RT Response Data Symbols

Symbol	Bits	Name	Function
0	7:0	<i>REG</i>	8-bit address of the register being read to or written from.
1	6:0	<i>LEN</i>	See Table 4-17.
1	7	<i>WnR</i>	0b for a Read Response. 1b for a Write Response.
m:2	7:0	RESPONSE_DATA	For a Write Response: One of the Result Codes defined in Table 4-17. For a Read Response: The sequence of bytes returned from target. Each Symbol contains one byte as payload. Register contents shall appear low-ordered byte first.

When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-17 and in the order listed.

Table 4-17. Processing of a Received AT/RT Command

STX Symbol Case	Action Taken	LEN Field in Response	RESPONSE_DATA field in Response
Operation with a single Data Symbol.	Send Response with no RESPONSE_DATA.	0	None.
Read Operation cases:			
Read operation to an unsupported vendor defined register or to an undefined register.	Send Response with no RESPONSE_DATA.	0	None.
Read operation with more than two Data Symbols.	Send Response with no RESPONSE_DATA.	0	None.
Read operation of more bytes than the target register length.	Send Response with a truncated read of the entire target register contents.	Set to the size in bytes of the target register being accessed.	Target register being accessed.
Read operation of fewer bytes than the target register length.	Send Response with the number of bytes requested.		Bytes requested.
All other read operations.	Perform the operation. Send Response.		Target register being accessed.
Write Operation cases:			
Write operation to an unsupported vendor defined register or to an undefined register.	Do not perform the write operation. Send Response.	0	Result Code = 01h (ERROR).
Write operation with LEN field that does not match the Transaction size.			
Write operation to a register with all Read-only (RO) fields.			
Write operation of more bytes than the target register length.			
Write operation of less bytes than the target register length.	Perform the write operation only on the requested bytes. Send Response.	Size in bytes of the target register being accessed.	Result Code = 00h (SUCCESS).
All other write operations.	Perform the write operation. Send Response.	Size in bytes of the target register being accessed.	Result Code = 00h (SUCCESS).

4.1.1.3.2 Connection Manager Access

A Connection Manager initiates a read from or write to SB Register Space via the USB4 Port Capability in Adapter Configuration Space. The Connection Manager writes to the *Target*, *Address*, *WnR*, *LEN*, *Index*, and *Data* fields then sets the *Pending* bit to 1b, which causes the Router to issue a SB Register access. When the SB Register access completes, the Router writes back to the *LEN*, *No Response*, *Result Code*, and *Data* fields and sets the *Pending* bit to 0b.

When the *Pending* bit in a USB4 Port Capability is set to 1b, a Router shall:

- If the *Target* field in the USB4 Port Capability is set to 000b, the Router shall issue an access to the SB Register Space of the USB4 Port:
 - The Router shall access the register identified in the *Address* field in the USB4 Port Capability.

- The Router shall access the number of bytes indicated in the *Length* field.
- If the *WnR* field is set to 0b, the Router shall read from the SB Register Space.
- If the *WnR* field is set to 1b, the Router shall write to the SB Register Space. The Router shall write the contents from the *Data* DWs in the USB4 Port Capability. Register contents shall be written least significant byte first.
- If the *Target* field in the USB4 Port Capability is set to 001b, the Router shall send an AT Command on the Sideband Channel of the USB4 Port to access the SB Register Space of the Link Partner. The AT Command shall have the following contents:
 - The *REG* field shall be set to the contents of the *Address* field in the USB4 Port Capability.
 - The *LEN* field shall be set to the contents of the *Length* field in the USB4 Port Capability.
 - The *WnR* field shall be set to the contents of the *WnR* field in the USB4 Port Capability.
 - If the *WnR* field is set to 1b, the COMMAND_DATA Symbols shall contain the contents from the *Data* DWs in the USB4 Port Capability. Register contents shall appear least significant byte first.
- If the *Target* field in the USB4 Port Capability is set to 010b, the Router shall send an Addressed RT Command on the Sideband Channel of the USB4 Port to access the SB Register Space of a Re-timer on the Link. The Addressed RT Command shall have the following contents:
 - The *Index* field shall be set to the contents of the Re-timer Index in the USB4 Port Capability.
 - The *REG* field shall be set to the contents of the *Address* field in the USB4 Port Capability.
 - The *LEN* field shall be set to the contents of the *Length* field in the USB4 Port Capability.
 - The *WnR* field shall be set to the contents of the *WnR* field in the USB4 Port Capability.
 - If the *WnR* field is set to 1b, the COMMAND_DATA Symbols shall contain the contents from the *Data* DWs in the USB4 Port Capability. Register contents shall appear least significant byte first.

A Router shall process an AT Command as described in Table 4-17. When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows:

- The *LEN* field in the AT Response, the RT Response, or the local access is copied to the *Length* field in the USB4 Port Capability.
- The *No Response* bit is updated.
- The *Result Code* bit in the USB4 Port Capability is updated.
- For a read, the *Data* DWs in the USB4 Port Capability are updated.

The Router shall then set the *Pending* bit in the USB4 Port Capability to 0b.

If the read or write access is to the SB Register Space of the local Router, then the Router shall complete the read or write access and set the *Pending* bit to 0b within *tLocalSBAccess* time after the *Pending* bit is set to 1b.

If the read or write access is to the SB Register Space of a Re-timer or a remote Router, the Router shall complete the read or write access and set the *Pending* bit to 0b within *tRemoteSBAccess* time after the *Pending* bit is set to 1b.

4.1.1.3.3 SB Register Definitions

Unless specified otherwise, the Connection Manager shall not write a register with a value that is marked as “Rsvd”. Writing a register with a value that is marked as “Rsvd” results in undefined behavior.

Table 4-18 lists the registers in the SB Register Space of a Router. See the USB4 Re-Timer Specification for the structure of the SB Register Space of a Re-timer.

Table 4-18. SB Registers

Register	Size (Bytes)	Name	Description
0	4	<i>Vendor ID</i>	Identifies the manufacturer of the Router silicon.
1	4	<i>Product ID</i>	Identifies the type of the Router.
2 to 4	N/A	--	Undefined.
5	4	<i>Debug Configuration</i>	Defines Debug Configuration for a USB4 Port.
6	54	<i>Debug</i>	Data written or read for a Debug.
7	4	<i>LRD Tuning</i>	Used to tune LRD Cable.
8	4	<i>Opcode</i>	A Port Operation Opcode in FourCC format.
9	4	<i>Metadata</i>	Metadata written or read with a Port Operation.
10 to 11	N/A	--	Undefined.
12	3	<i>Link Configuration</i>	Defines Link Configuration for a USB4 Port.
13	4	<i>Gen 2/3 TxFFE</i>	Used to exchange the TxFFE parameters of Gen 2 or Gen 3 Link transmitters.
14	4	<i>Gen 4 TxFFE</i>	Used to exchange the TxFFE parameters of Gen 4 Link transmitters.
15	4	<i>Sideband Channel Version</i>	A vendor defined version of the Sideband Channel implementation.
16 to 17	vendor specific	<i>vendor specific</i>	Vendor specific register.
18	64	<i>Data</i>	Data written or read with a Port Operation.
19 to 127	vendor specific	vendor specific	Vendor specific register.
128 to 255	N/A	--	Undefined.

Table 4-19 defines the Commands that are allowed for a particular SB Register field.

Table 4-19. SB Register Fields Access Types

Access Type	Description
RO	Read Only. A Write operation to a field with this access type shall have no effect. A Read operation shall return a meaningful value.
WO	Write Only. A field with this access type shall be capable of a Write operation. A Read operation may not return a meaningful value.
RW	Read/Write. A field with this access type shall be capable of both Read operation and Write operation. The value read from this field shall reflect the last value written to it unless the field was reset in the interim.
Rsvd	Reserved. Reserved for future implementation. A Write operation to this field shall have no effect.

The SB Register Space registers shall have the structure and fields described in Table 4-17. Registers not listed in Table 4-20 are undefined and shall not be used.

Table 4-20. SB Register Fields

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
0	Vendor ID	0	7:0	Vendor ID Low – Identifies the manufacturer of the Router silicon. Shall contain the same value as the lower byte of the <i>Vendor ID</i> field in Router Configuration Space.	RO	Vendor Defined
		1	7:0	Vendor ID High – Identifies the manufacturer of the Router silicon. Shall contain the same value as the higher byte of the <i>Vendor ID</i> field in Router Configuration Space.	RO	Vendor Defined
		2	7:0	Reserved	Rsvd	0
		3	7:0	Reserved	Rsvd	0
1	Product ID	0	7:0	Product ID Low – Assigned by the manufacturer to identify the type of the Router. Shall contain the same value as the lower byte of the <i>Product ID</i> field in Router Configuration Space.	RO	Vendor Defined
		1	7:0	Product ID High – Assigned by the manufacturer to identify the type of the Router. Shall contain the same value as the higher byte of the <i>Product ID</i> field in Router Configuration Space.	RO	Vendor Defined
		2	7:0	Reserved	Rsvd	0
		3	7:0	Reserved	Rsvd	0
5	Debug Capability Configuration	0	1:0	Scrambler Re-Sync Support Gen 2 or Gen 3 – Indicates Lanes supported by Scrambler Re-Sync on this USB4 Port for Gen 2 or Gen 3 speeds. Defined encodings are: 00b – Scrambler Re-Sync not supported 01b – Scrambler Re-Sync supports Tx only 10b – Scrambler Re-Sync supports Tx and Rx 11b – Reserved	RO	Vendor Defined
			3:2	Scrambler Re-Sync Support Gen 4 – Indicates Lanes supported by Scrambler Re-Sync on this USB4 Port for Gen 4 speed. Defined encodings are: 00b – Scrambler Re-Sync not supported 01b – Scrambler Re-Sync supports Tx only 10b – Scrambler Re-Sync supports Tx and Rx 11b – Reserved	RO	Vendor Defined
			5:4	Enable Scrambler Re-Sync (ESRS) Gen 2 or Gen 3 – A Router uses this field to enable Scrambler Re-Sync on this USB4 Port for Gen 2 or Gen 3 speeds. These values shall be retained during Sleep. Defined encodings are: 00b – Disable Scrambler Re-Sync 01b – Enable Scrambler Re-Sync for Tx only 10b – Enable Scrambler Re-Sync for Tx and Rx 11b – Reserved	R/W	00b

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
			7:6	Enable Scrambler Re-Sync (ESRS) Gen 4 – A Router uses this field to enable Scrambler Re-Sync on this USB4 Port for Gen 4 speed. These values shall be retained during Sleep. Defined encodings are: 00b – Disable Scrambler Re-Sync 01b – Enable Scrambler Re-Sync for Tx only 10b – Enable Scrambler Re-Sync for Tx and Rx 11b – Reserved	R/W	00b
6	Debug	0	7:0	Debug Capability ID – Indicates Debug Capability for this read or write of register. See Table 4-24.	R/W	0
		53:1	See Table 4-24.			
7	LRD Tuning	0	0	Response Request – When this bit is set to 1b, the USB4 Port shall send a Write Command to the LRD Tuning register in the adjacent Router/Re-timer. The write shall contain the values of the local LRD Tuning register and shall have the Response Request bit set to 0b. The USB4 Port shall then set this bit to 0b.	R/W SC	0
			7:1	Data 0	R/W	0
		1	7:0	Data 1	R/W	0
		2	7:0	Data 2	R/W	0
		3	7:0	Data 3	R/W	0
8	Opcode	0	7:0	Opcode 0 Contains the first character of the Opcode.	RW	0
		1	7:0	Opcode 1 Contains the second character of the Opcode.	RW	0
		2	7:0	Opcode 2 Contains the third character of the Opcode.	RW	0
		3	7:0	Opcode 3 Contains the fourth character of the Opcode.	RW	0
9	Metadata	3:0	7:0	Metadata A Connection Manager writes to this field when initiating a Port Operation. A Router shall write the Completion Metadata (if any) to this field after executing a Port Operation. See Section 8.3.2 for more information on Port Operations.	RW	0
12	Link Configuration	0	0	Enabling Decision (Lane 0) – Shall indicate whether the Lane 0 Adapter is enabled during Lane Initialization. 0b – Not enabled 1b – Enabled	RO	0b
			1	Enabling Decision (Lane 1) – Shall indicate whether the Lane 1 Adapter is enabled during Lane Initialization. 0b – Not enabled 1b – Enabled	RO	0b
			2	Asymmetric Decision (Tx) – Shall be set to 1b if both lanes are enabled and three transmitters are enabled in the USB4 Port, and shall be set to 0 otherwise. <u>During Phase 3 in Lane Initialization, based on Table 4-30, otherwise based on the Negotiated Link Width field.</u>	RO	0b

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
			3	Asymmetric Decision (Rx) – Shall be set to 1b if both lanes are enabled and three receivers are enabled in the USB4 Port, and shall be set to 0 otherwise. <u>During Phase 3 in Lane Initialization, - based on Table 4-30, otherwise, base on the Negotiated Link Width field.</u>	RO	0b
			7:4	Reserved	Rsvd	0
		1	0	Enabling Request (Lane 0) – Indicates whether the Router requests enabling for Lane 0. 0b – No request to enable 1b – Request to enable A Router shall set this bit to 0b when the <i>Lane Disable</i> bit in the Lane Adapter Configuration Capability for Lane 0 is 1b. Otherwise, this bit shall be set to 1b.	RO	1b
			1	Enabling Request (Lane 1) – Indicates whether the Router requests enabling for Lane 1. 0b – No request to enable 1b – Request to enable A Lane 1 Adapter shall not request enabling unless the Lane 0 Adapter requests enabling. A Router shall set this bit to 0b when the <i>Lane Disable</i> bit in the Lane Adapter Configuration Capability for Lane 1 is 1b. Otherwise, this bit shall be set to 1b.	RO	1b
			3:2	Reserved	Rsvd	0
			4	Bonding Support – Indicates whether Lane Bonding is supported for this USB4 Port. 0b – Lane Bonding is not supported 1b – Lane Bonding is supported	RO	1b
			5	Gen 3 Support – Indicates whether Gen 3 speeds are supported on this USB4 Port. 0b – Gen 3 speeds are not supported 1b – Gen 3 speeds are supported A USB4 Port shall only set this bit to 1b if all the following are true: <ul style="list-style-type: none"> The USB4 Port supports Gen 3 speeds. All On-Board Re-timers connected between the USB4 Port and the Type-C connector support Gen 3 speeds. <i>Note: The method of conveying the capabilities of an On-Board Re-timer to the Router is implementation specific.</i> <ul style="list-style-type: none"> The USB4 Port implements both a Lane 0 Adapter and a Lane 1 Adapter. The <i>Target Link Speed</i> field in the Lane 0 Adapter Configuration Capability is 1100b or 1110b. Otherwise this bit shall be 0b.	RO	1b for a USB4 Hub, else Vendor Defined
			6	RS-FEC Request (Gen 2) – Indicates whether the Router requests enabling RS-FEC in Gen 2 Speeds for this USB4 Port. 0b – No request to enable 1b – Request to enable A USB4 Port shall set this bit to the same value as the <i>Request RS-FEC Gen 2</i> bit in the USB4 Port Capability.	RO	1b

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
		2	7	RS-FEC Request (Gen 3) – Indicates whether the Router requests enabling RS-FEC in Gen 3 Speeds for this USB4 Port. 0b – No request to enable 1b – Request to enable A USB4 Port shall set this bit to the same value as the <i>Request RS-FEC Gen 3</i> bit in the USB4 Port Capability.	RO	1b
			0	USB4 Sideband Channel Support Indicates that this USB4 Port supports a Sideband Channel as defined in Chapter 4 of this specification. Shall be set to 1b.	RO	1b
			1	TBT3-Compatible Speeds Support – Indicates whether TBT3-Compatible speeds are supported on this USB4 Port. 0b – TBT3-Compatible speeds are not supported 1b – TBT3-Compatible speeds are supported A USB4 Port shall only set this bit to 1b if the Router and all On-Board Re-timers connected between the Router and the Type-C connector support TBT3-Compatible Mode speeds. The method of conveying the capabilities of an On-Board Re-timer to the Router is implementation specific.	RO	Vendor Defined
			2	Gen 4 Support Indicates whether Gen 4 speed is supported on this USB4 Port. 0b – Gen 4 speed is not supported 1b – Gen 4 speed is supported A USB4 Port shall set this bit to 1b if all the following are true: <ul style="list-style-type: none"> The USB4 Port supports Gen 4 speed. All On-Board Re-timers connected between the USB4 Port and the Type-C connector support Gen 4 speed. <i>Note: The method of conveying the capabilities of an On-Board Re-timer to the Router is implementation specific.</i> <ul style="list-style-type: none"> The <i>Target Link Speed</i> field in the Lane 0 Adapter Configuration Capability is 1110b. Otherwise, this bit shall be 0b.	RO	Vendor Defined
			3	Asymmetric Support 3 Tx Indicates whether an Asymmetric Link with three transmitters is supported on the USB4 Port. 0b – Asymmetric Link with three transmitters is not supported. 1b – Asymmetric Link with three transmitters is supported. A USB4 Port shall set this bit to 1b if the USB4 Port supports Gen 4 speed and Asymmetric Link with three transmitters (bit 22 is 1b in the <i>Gen 4 Asymmetric Support</i> field). Otherwise this bit shall be 0b.	RO	Vendor Defined

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
			4	Asymmetric Support 3 Rx Indicates whether an Asymmetric Link with three receivers is supported on the USB4 Port. 0b – Asymmetric Link with three receivers is not supported. 1b – Asymmetric Link with three receivers is supported. A USB4 Port shall set this bit to 1b if the USB4 Port supports Gen 4 speed and Asymmetric Link with three receivers (bit 23 in the <i>Gen 4 Asymmetric Support</i> field is 1b). Otherwise this bit shall be 0b.	RO	Vendor Defined
			5	Request Asymmetric Tx Indicates whether the USB4 Port is requesting to operate with three transmitters in an Asymmetric Link. Shall be set to 1b if the <i>Target Asymmetric Link</i> field is 01b. Otherwise this bit shall be 0b.	RO	Vendor Defined
			6	Request Asymmetric Rx Indicates whether the USB4 Port is requesting to operate with three receivers in an Asymmetric Link. Shall be set to 1b if the <i>Target Asymmetric Link</i> field is 10b. Otherwise this bit shall be 0b	RO	Vendor Defined
			7	Reserved	Rsvd	0
13	Gen 2/3 TxFFE	0	3:0	TxFFE Request (Lane 0) – Identifies one of 16 predefined TxFFE configurations requested by the receiver.	RO	Vendor Defined
			4	Rx Locked (Lane 0) – Indicates that the receiver completed TxFFE negotiation. 0b – TxFFE negotiation is not done 1b – TxFFE negotiation is done	RO	0b
			5	Rx Active (Lane 0) – Indicates whether the receiver is active. 0b – Receiver is inactive 1b – Receiver is active	RO	0b
			6	Clock Switch Done (Lane 0) Shall be set to the value of the <i>Rx Locked (Lane 0)</i> bit.	RO	0b
			7	New Request (Lane 0) – Indicates whether the receiver is processing a TxFFE Request. 0b – Receiver finished processing the previous request 1b – Receiver is still processing the previous request	RO	0b
		1	3:0	TxFFE Request (Lane 1) – Identifies one of 16 predefined TxFFE configurations requested by the receiver.	RO	Vendor Defined
			4	Rx Locked (Lane 1) – Indicates that the receiver completed TxFFE negotiation. 0b – TxFFE negotiation is not done 1b – TxFFE negotiation is done	RO	0b
			5	Rx Active (Lane 1) – Indicates whether the receiver is active. 0b – Receiver is inactive 1b – Receiver is active	RO	0b

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
			6	Clock Switch Done (Lane 1) Shall be set to the value of the <i>Rx Locked (Lane 1)</i> bit.	RO	0b
			7	New Request (Lane 1) – Indicates whether the receiver is processing a TxFFE Request. 0b – Receiver finished processing the previous request 1b – Receiver is still processing the previous request	RO	0b
		2	3:0	TxFFE Setting (Lane 0) – Index of the TxFFE configuration to be loaded to the transmitter.	RO	Vendor Defined
			5:4	Reserved	Rsvd	0
			6	Request Done (Lane 0) – Indicates whether the transmitter loaded the recent requested index of TxFFE configuration. 0b – Transmitter has not yet loaded the recent requested index of TxFFE configuration 1b – Transmitter has loaded the recent requested index of TxFFE configuration	RO	0b
			7	Tx Active (Lane 0) – Indicates whether the transmitter is transmitting a valid signal. 0b – Transmitter is not transmitting a valid signal 1b – Transmitter is transmitting a valid signal	RO	0b
		3	3:0	TxFFE Setting (Lane 1) – Index of the TxFFE configuration to be loaded to the transmitter.	RO	Vendor Defined
			5:4	Reserved	Rsvd	0
			6	Request Done (Lane 1) – Indicates whether the transmitter loaded the recent requested index of TxFFE configuration. 0b – Transmitter has not yet loaded the recent requested index of TxFFE configuration 1b – Transmitter has loaded the recent requested index of TxFFE configuration	RO	0b
			7	Tx Active (Lane 1) – Indicates whether the transmitter is transmitting a valid signal. 0b – Transmitter is not transmitting a valid signal 1b – Transmitter is transmitting a valid signal	RO	0b
14	Gen 4 TxFFE	See Table 4-21.				
15	Sideband Channel Version	0	7:0	Sub Version – The binary coded decimal digit of the sub version number of the Sideband Channel implementation. Contains a vendor defined value.	RO	Vendor Defined
		1	7:0	Minor Version – The binary coded decimal digit of the minor version number of the Sideband Channel implementation. Contains a vendor defined value.	RO	Vendor Defined
		2	7:0	Major Version LSB – The least-significant binary coded decimal digit of the major version number of the Sideband Channel implementation. Contains a vendor defined value.	RO	Vendor Defined
		3	7:0	Major Version MSB – The most-significant binary coded decimal digit of the major version number. Contains a vendor defined value.	RO	Vendor Defined

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
18	Data	63:0	7:0	Data A Connection Manager writes to this field when initiating a Port Operation. A Router shall write the Completion Data (if any) to this field after executing a Port Operation. See Section 8.3.2 for more information on Port Operations.	RW	0
Notes: 1. Byte 0 in register 13 is the <i>Rx Status & TxFFE Request</i> byte for Lane 0. 2. Byte 1 in register 13 is the <i>Rx Status & TxFFE Request</i> byte for Lane 1. 3. Byte 2 in register 13 is the <i>Tx Status</i> byte for Lane 0. 4. Byte 3 in register 13 is the <i>Tx Status</i> byte for Lane 1.						



CONNECTION MANAGER NOTE

The Connection Manager shall not write to bits 7:4 in Sideband Register 5 if the relevant Debug feature is not supported.

4.1.1.3.3.1 Gen 4 TxFFE Register Mapping

The Gen 4 TxFFE register shall have a dynamic mapping according to Table 4-21. When changing the register mapping, the new byte shall be set to its default values according to Table 4-21 or Table 4-22.

Table 4-21. Gen 4 TxFFE Register Mapping

Byte	Symmetric	Asymmetric – USB4 Port has 3 Receivers	Asymmetric – USB4 Port has 3 Transmitters
0	Gen 4 Partner Rx 0 Status & TxFFE Request	Gen 4 Partner Rx 0 Status & TxFFE Request	Gen 4 Partner Rx 0 Status & TxFFE Request
1	Gen 4 Partner Rx 1 Status & TxFFE Request	Gen 4 Partner Tx 0 Status	Gen 4 Partner Rx 1 Status & TxFFE Request
2	Gen 4 Partner Tx 0 Status	Gen 4 Partner Tx 1 Status	Gen 4 Partner Rx 2 Status & TxFFE Request
3	Gen 4 Partner Tx 1 Status	Gen 4 Partner Tx 2 Status	Gen 4 Partner Tx 0 Status
Notes: 1. Gen 4 Partner Rx Status & TxFFE Request byte is defined in Table 4-22. 2. Gen 4 Partner Tx Status byte is defined in Table 4-23.			

Table 4-22. Gen 4 Partner Rx Status & TxFFE Request Byte

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
14	Gen 4 TxFFE		5:0	Gen 4 TxFFE Request – Identifies one of 50-42 predefined PAM3 TxFFE configurations requested by the receiver.	RW	0h
			6	Reserved	RO	0b
			7	New Request – Indicates whether the receiver has a new Gen 4 TxFFE Request. 0b – Receiver does not have a new Gen 4 TxFFE request. 1b – Receiver has a new Gen 4 TxFFE request.	RW	0b

Table 4-23. Gen 4 Partner Tx Status Byte

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
14	Gen 4 TxFFE		5:0	Gen 4 TxFFE Setting – Index of the Gen 4 TxFFE configuration loaded by the transmitter.	RW	0h
			6	Request Done – Indicates whether the transmitter loaded the recent requested index of Gen 4 TxFFE configuration: 0b – Transmitter has not yet loaded the recent requested index of Gen 4 TxFFE configuration. 1b – Transmitter has loaded the recent requested index of Gen 4 TxFFE configuration.	RW	0b
			7	Start TxFFE – Indicates whether the Link Partner transmitter is ready to receive a TxFFE request: 0b – Transmitter is not ready to receive a TxFFE request. 1b – Transmitter is ready to receive a TxFFE request. This bit is shall be cleared when the final TxFFE preset is set and Request Done bit is 0b.	R/W SC	0b

4.1.1.3.3.2 Debug Capability Register Mapping**Table 4-24. Debug Register Mapping**

Debug Capability ID	Debug Capability Name	Debug Register Bytes 1-63 Mapping
0	None	Reserved
1	Scrambler Re-Sync	See Table 4-25 if ESRS is set to 01b. See Table 4-26 if ESRS is set to 10b.
2-127	Reserved	Reserved
128-255	Vendor Defined	Vendor Defined

Table 4-25. Debug Register Scrambler Re-Sync Bytes (ESRS = 01b)

Byte	Symmetric	Asymmetric – Port has 3 Receivers	Asymmetric – Port has 3 Transmitters
1	Scrambler Re-Sync Link Configuration		
14:2	Scrambler Re-Sync Tx 0 State	Scrambler Re-Sync Tx 0 State	Scrambler Re-Sync Tx 0 State
27:15	Scrambler Re-Sync Tx 1 State		Scrambler Re-Sync Tx 1 State
40:28			Scrambler Re-Sync Tx 2 State
53:41			
Notes:			
1. Scrambler Re-Sync Link Configuration is defined in Table 4-27.			
2. Scrambler Re-Sync State byte is defined in Table 4-28 (Gen 4) and Table 4-29 (Gen 2/3).			

Table 4-26. Debug Register Scrambler Re-Sync Bytes (ESRS = 10b)

Byte	Symmetric	Asymmetric – Port has 3 Receivers	Asymmetric – Port has 3 Transmitters
1	Scrambler Re-Sync Link Configuration		
14:2	Scrambler Re-Sync Tx 0 State	Scrambler Re-Sync Tx 0 State	Scrambler Re-Sync Tx 0 State
27:15	Scrambler Re-Sync Tx 1 State	Scrambler Re-Sync Rx 0 State	Scrambler Re-Sync Tx 1 State
40:28	Scrambler Re-Sync Rx 0 State	Scrambler Re-Sync Rx 1 State	Scrambler Re-Sync Tx 2 State
53:41	Scrambler Re-Sync Rx 1 State	Scrambler Re-Sync Rx 2 State	Scrambler Re-Sync Rx 0 State
Notes:			
1. Scrambler Re-Sync Link Configuration is defined in Table 4-27.			
2. Scrambler Re-Sync State byte is defined in Table 4-28 (Gen 4) and Table 4-29 (Gen 2/3).			

Table 4-27. Scrambler Re-Sync Link Configuration Byte

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
6	Debug	1	0	Enable Scrambler Re-Sync – A Router uses this field to enable Scrambler Re-Sync on this USB4 Port. Defined encodings are: 0b – Scrambler Re-Sync for Tx only 1b – Scrambler Re-Sync for Tx and Rx	WO	Vendor Defined
			2:1	Link Gen – Indicates which speed is for this USB4 Port: 00b – Gen 2 speed 01b – Gen 3 speed 10b – Gen 4 speed 11b – Reserved	WO	Vendor Defined
			3	RS_FEC Enabled – Indicates if RS_FEC is enabled on the link: 0b – RS-FEC is not enabled on the Link. 1b – RS-FEC is enabled on the Link.	WO	Vendor Defined
			4	Asymmetric Decision (Tx) – Shall be set to 1b if three transmitters are enabled in the Port based on Table 4-30. Otherwise, shall be set to 0b. This bit shall only be set to 1b if both Lanes are enabled.	WO	0b
			5	Asymmetric Decision (Rx) – Shall be set to 1b if three receivers are enabled in the Port based on Table 4-30. Otherwise, shall be set to 0b. This bit shall only be set to 1b if both Lanes are enabled.	WO	0b

Table 4-28. Scrambler Re-Sync State Byte for Gen 4

Byte	Bits	Field Name and Description	Type	Default Value
5:0	41:0	Lane Data – 21 trits sampled from Physical Layer of this Lane, converted to binary using method defined in Section 4.4.8.3. Byte0[0:1] – HS_Sample[0] – Oldest Data Sample Byte0[2:3] – HS_Sample[1] ... Byte5[0:1] – HS_Sample[20] – Newest Data Sample	WO	Vendor Defined
	47:42	Reserved	Rsvd	0h
10:6	37:0	PRTS LFSR State – 19 trits of PRTS state, converted to binary using method defined in Section 4.4.8.3. PRTS19 Ternary LFSR State (19 Trits) Byte 6[0:1] – Ternary LFSR[0] Byte 6[2:3] – Ternary LFSR [1] ... Byte 10[0:1] – Ternary LFSR [16] Byte 10[2:3] – Ternary LFSR [17] Byte 10[4:5] – Ternary LFSR [18]	WO	Vendor Defined
	39:38	Reserved	Rsvd	0h
12:11	10:0	PRBS LFSR State – 11bits of PRBS state. Byte 11[0] – Binary LFSR[0] Byte 11[1] – Binary LFSR [1] ... Byte 12[0] – Binary LFSR [8] Byte 12[1] – Binary LFSR [9] Byte 12[2] – Binary LFSR [10]	WO	Vendor Defined
	15:11	Reserved	Rsvd	0h

Table 4-29. Scrambler Re-Sync State Byte for Gen 2/3

Byte	Bits	Field Name and Description	Type	Default Value
3:0	31:0	Lane Data – 21 bits sampled from Physical Layer of this Lane. Byte 0[0] – HS_Sample[0] – Oldest Data Sample Byte 0[1] – HS_Sample[1] ... Byte 3[7] – HS_Sample[31] – Newest Data Sample	WO	Vendor Defined
6:4	22:0	LFSR State – 23 bits of LFSR state. Byte 4[0] – Binary LFSR[0] Byte 4[1] – Binary LFSR [1] ... Byte 6[4] – Binary LFSR [20] Byte 6[5] – Binary LFSR [21] Byte 6[6] – Binary LFSR [22]	WO	Vendor Defined
	23	Reserved	Rsvd	0h

Note: The Least Significant Symbol of the High-Speed Data and LFSR are aligned.

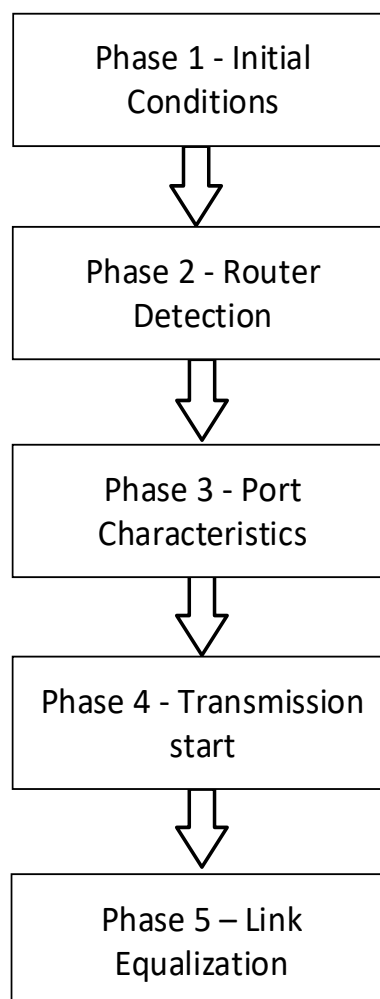
4.1.2 Lane Initialization

This section defines how a Sideband Channel is used to initialize the Lane(s) that make up a USB4 Link. Lane Initialization is the process by which the Electrical Layer of a Lane goes from inactive to actively transmitting and receiving traffic.

The Sideband Channel shall initialize each Lane independently. A Sideband Channel is used to initialize all enabled Lanes in its USB4 Port. Initialization shall occur for all enabled USB4 Ports on a Router.

Lane Initialization consists of a series of phases, which are summarized in Figure 4-5 and described in the subsections below. Lane Initialization starts with the Adapter in CLd state and ends with the Adapter either in Training. LOCK1 sub-state (for Gen 2 and Gen 3 Links) or in Training. TS2 sub-state (for Gen 4 Links). The transition from CLd state to Training state is defined in Section 4.2.1.2.3.

Figure 4-5. Overview of Lane Initialization



Lane Initialization is described from the point of view of a single Router and its Link Partner, which are called “Router A” and “Router B” respectively for distinction. Note that Lane Initialization is symmetrical, meaning that the steps defined for Router A are also followed by Router B in parallel (with Router A and Router B switching roles) for each phase of Lane Initialization. Furthermore, the steps for each phase are defined within the context of a single Lane and are repeated for each Lane shared between Router A and Router B.

4.1.2.1 Phase 1 – Determination of Initial Conditions

During Phase 1, Router A discovers the following connection information:

- Whether the Link is USB4.
- Whether there is a reverse insertion at the USB Type-C® connector.
- Whether it is connected by an Active Cable that contains Re-timers.
 - If connected by an Active Cable that contains Re-timers:
 - Whether the cable is a TBT3 Active Cable (See Section 13.2.1.1).
 - Whether the cable supports Gen 4 speed.
 - Else:
 - Whether the Cable supports Gen 3 speed.
 - Whether the Cable supports Gen 4 speed.
 - Whether the cable supports CLx states.
 - Whether the cable supports an Asymmetric Link.

A USB4 Port shall not continue on to Phase 2 until it has obtained the connection information described in this section. See the USB PD Specification and the USB Type-C Specification for how to determine the connection information.

A USB4 Port shall not proceed to Phase 2 if the Link is not USB4.

A USB4 Port shall drive SBTX to logic low by default.

**IMPLEMENTATION NOTE**

Each Router has a pull-up resistor that pulls SBTX up to logical high unless the Router actively drives SBTX low. Because of this, it is necessary to actively drive SBTX in Phase 1, so that the pull-up resistor doesn't cause the Sideband Channel to inadvertently read as logic high.

4.1.2.1.1 Lane Reversal

Lane mismatch is caused by reverse insertion of a USB Type-C connector. Lane mismatch results in a Link where:

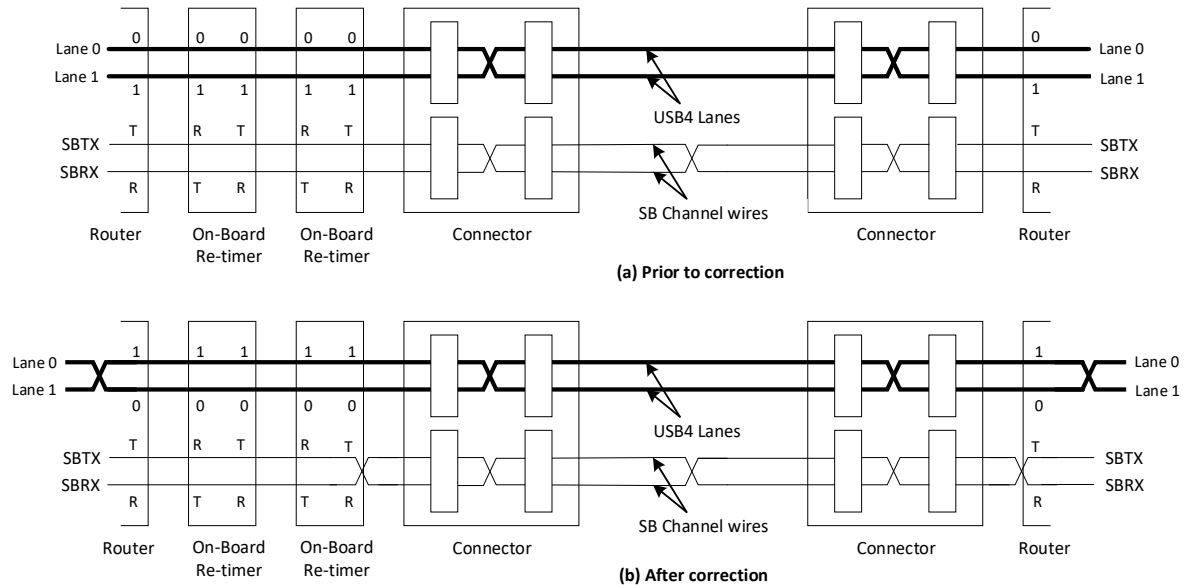
- The SBTX wires for the USB4 Ports at each end of the Link are connected to each other.
- The SBRX wires for the USB4 Ports at each end of the Link are connected to each other.
- The Lane 0 Adapters at each end of the Link are connected to the Lane 1 Adapters at the other end of the Link.

When a Router detects a reverse insertion on a USB Type-C connector, it shall perform Lane Reversal in the USB4 Port that faces the reversed connector. Lane Reversal shall be performed during Phase 1. Lane Reversal consists of the following:

- The Router shall swap the designation of Lane 0 and Lane 1 and shall associate the Lane 0 Adapter with the updated Lane 0 and the Lane 1 Adapter with the updated Lane 1.
- If there are no On-Board Re-timers between Router and the USB Type-C connector, the Router shall swap its SBTX and SBRX lines facing the connector.

Figure 4-6 show an example of a Link before and after Lane reversal. Note that in Figure 4-6 Lane mismatch occurs on both ends of the Link, therefore both ends of the Link perform Lane Reversal.

Figure 4-6. Example of Lane Reversal



4.1.2.1.2 Polarity Inversion

Polarity mismatch is caused by connecting a Lane between a Router and an On-Board Re-timer or a Router and a USB Type-C connector such that the positive half of a differential pair at one end is connected to the negative half of a differential pair at the other end.

A Router may be configured to perform polarity inversion during Phase 1 of Lane Initialization. The method to perform polarity inversion is outside the scope of this specification.

4.1.2.2 Phase 2 – Router Detection

The second phase of Lane Initialization consists of each Router detecting any connected Routers.

After completion of Phase 1, a Host Router shall initiate Router detection by driving SBTX to logic high on all of its Downstream Facing Ports.

When a Device Router detects a logic high on SBRX of its Upstream Facing Port for $t_{ConnectRx}$ time, it shall drive SBTX to logic high on all of its USB4 Ports.

After a USB4 Port drives its SBTX to logic high and detects a logic high on its SBRX for $t_{ConnectRx}$ time, it shall set its *Router Detected* bit to 1b, then transition to Phase 3 of Lane Initialization.

Note: If a USB4 Port receives a Transaction while it is still in Phase 2, it may ignore or drop the Transaction.

4.1.2.3 Phase 3 – Determination of USB4 Port Characteristics

The third phase of Lane Initialization consists of each Router acquiring information about its Link Partner.

During Phase 3, Router A shall read the Link Configuration register (register 12) of Router B using AT Transactions. Router A shall issue additional register reads to Router B as needed to avoid a tATimeout delay at the Link Partner (see Section 4.1.1.2.6). Router A may re-read register 12 or it may read other SB Registers during this phase.

Router A shall then decide the following Lane attributes using the decision criteria in Table 4-30.

Table 4-30. Lane Attributes

Attribute	Action
Enabling	<p>If <i>Enabling Request</i> = 1b in the SB Register Space of the Adapters of both Router A and Router B, Router A shall:</p> <ul style="list-style-type: none"> • Proceed to initialize the Lane. • Set the local <i>Enabling Decision</i> bit for the Adapter to 1b. <p>Else, Router A shall:</p> <ul style="list-style-type: none"> • Not initialize the Lane. The Adapter shall remain in CLd state. • Set the local <i>Enabling Decision</i> bit for the Adapter to 0b.
Bonding	<p>Router A shall set the <i>Bonding Enabled</i> bit in the USB4 Port Capability to 1b if all the following are true:</p> <ul style="list-style-type: none"> • The USB4 Ports of Router A and Router B both have the <i>Enabling Request</i> bit set to 1b for both Lanes of the USB4 Port. • The USB4 Ports of Router A and Router B both support Lane bonding (i.e. the <i>Bonding Support</i> bit is 1b in the SB Register Space of the Adapters on both sides of the Lane). <p>Otherwise, Router A shall set the <i>Bonding Enabled</i> bit to 0b.</p>
Lane Speed	<p>Speed Selection:</p> <p>Router A shall operate at Gen 4 Lane speed if all the following are true:</p> <ul style="list-style-type: none"> • The Adapters on both sides of the Lane support Gen 4 speed (i.e. the <i>Gen 4 Support</i> bit is set to 1b). • The cable over which Router A and Router B are communicating supports Gen 4 speed. • Both Lanes are enabled on each side of the Link (i.e. the <i>Enabling Request</i> bit for both Lanes is set to 1b). <p>Else, Router A shall operate at Gen 3 Lane speed if all the following are true:</p> <ul style="list-style-type: none"> • The Adapters on both sides of the Lane support Gen 3 speed (i.e. the <i>Gen 3 Support</i> bit is set to 1b). • The cable over which Router A and Router B are communicating supports Gen 3 speed. <p>Otherwise, Router A shall operate at Gen 2 Lane speed.</p> <p>Router A shall set the <i>Current Link Speed</i> field in the Lane Adapter Configuration Capability to reflect whether it is operating at Gen 2, Gen 3, or Gen 4 Lane speed.</p>
RS-FEC	<p>Gen 2 Speed:</p> <p>Router A shall enable RS-FEC if both sides of the Link request it (i.e. the <i>RS-FEC Request (Gen 2)</i> bit is set to 1b in the SB Register Space of both the local USB4 Port and its Link Partner). Otherwise, RS-FEC shall not be enabled.</p> <p>Router A shall set the <i>RS-FEC Enabled (Gen 2)</i> bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.</p> <p>Gen 3 Speed:</p> <p>Router A shall enable RS-FEC if both sides of the Link request it (i.e. the <i>RS-FEC Request (Gen 3)</i> bit is set to 1b in the SB Register Space of both the local USB4 Port and its Link Partner). Otherwise, RS-FEC shall not be enabled.</p> <p>Router A shall set the <i>RS-FEC Enabled (Gen 3)</i> bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.</p> <p>Gen 4 Speed:</p> <p>Router A shall enable RS-FEC.</p>

Attribute	Action
Asymmetric	<p>Symmetric vs. Asymmetric (3 Tx/1 Rx or 3 Rx/1 Tx)</p> <p>Router A shall operate in Asymmetric (3 Tx/1 Rx) mode if all the following are true:</p> <ul style="list-style-type: none"> The <i>Asymmetric Support 3 Tx</i> bit is set to 1b in Router A and the <i>Asymmetric Support 3 Rx</i> bit is set to 1b in Router B. The cable over which Router A and Router B are communicating supports an Asymmetric Link. The <i>Request Asymmetric Tx</i> bit is set to 1b in Router A's SB Register. The <i>Request Asymmetric Rx</i> bit is set to 1b in Router B's SB Register. <p>Else, Router A shall operate in Asymmetric (3 Rx/1 Tx) mode if all the following are true:</p> <ul style="list-style-type: none"> The <i>Asymmetric Support 3 Rx</i> bit is set to 1b in Router A and the <i>Asymmetric Support 3 Tx</i> bit is set to 1b in Router B. The cable over which Router A and Router B are communicating supports an Asymmetric Link. Router A requests 3 receivers (i.e. the <i>Request Asymmetric Rx</i> bit is set to 1b in Router A's SB Register). Router B requests 3 transmitters (i.e. the <i>Request Asymmetric Tx</i> bit is set to 1b in Router B's SB Register). <p>Else, Router A shall operate in Symmetric mode.</p>

Note: The values that are read from the Link Configuration registers in Phase 3 determine the Link characteristics for the rest of the Lane Initialization sequence. If the values in the Link Configuration registers change after they are read in Phase 3, the new values do not take effect until the next Lane Initialization.

4.1.2.4 Phase 4 – Lane Parameters Synchronization and Transmit Start

During Phase 4, a USB4 Port sets the Lane speed and starts transmission. The following sequence takes place on the Sideband Channel between Router A and Router B:

- Router A shall finish establishing common mode voltages on its enabled transmitters.
- Router A shall send a Broadcast RT Transaction every *tLaneParams* with the parameter values in Table 4-30. Router A shall continue sending Broadcast RT Transactions until all the following conditions are true, then continue to Step 3:
 - At least *tLTPHase4* time has passed from completion of Phase 2.
 - Router A has sent Broadcast RT Transactions at least twice.
 - Router A has received a Broadcast RT Transaction from Router B.
- If the negotiated speed is Gen 2 or Gen 3:
 - Router A shall activate the transmitter on each enabled Lane at the selected speed and shall send SLOS1 as defined in Section 4.2.1.3.
 - After its transmitter is transmitting a valid signal, Router A shall then send an LT_Resume Transaction for each enabled Lane in the USB4 Port and shall set to 1b the *Tx Active* bit in the Tx Status byte of the TxFFE register in the SB Register Space to indicate that it has started transmission on the target Lane. The *LSELane* field in the LT_Resume Transaction shall equal the Lane number associated with the transmitter.

Note: The behavior of the transmitter is undefined prior to setting the Tx Active bit to 1b.

- Router A's USB4 Port goes to Phase 5.

4. If the negotiated speed is Gen 4, both Router A and Router B execute the following steps. For simplicity, only Router A's steps are described:

Note: The progress of Router A through the following steps depends on Router B's progress through the steps

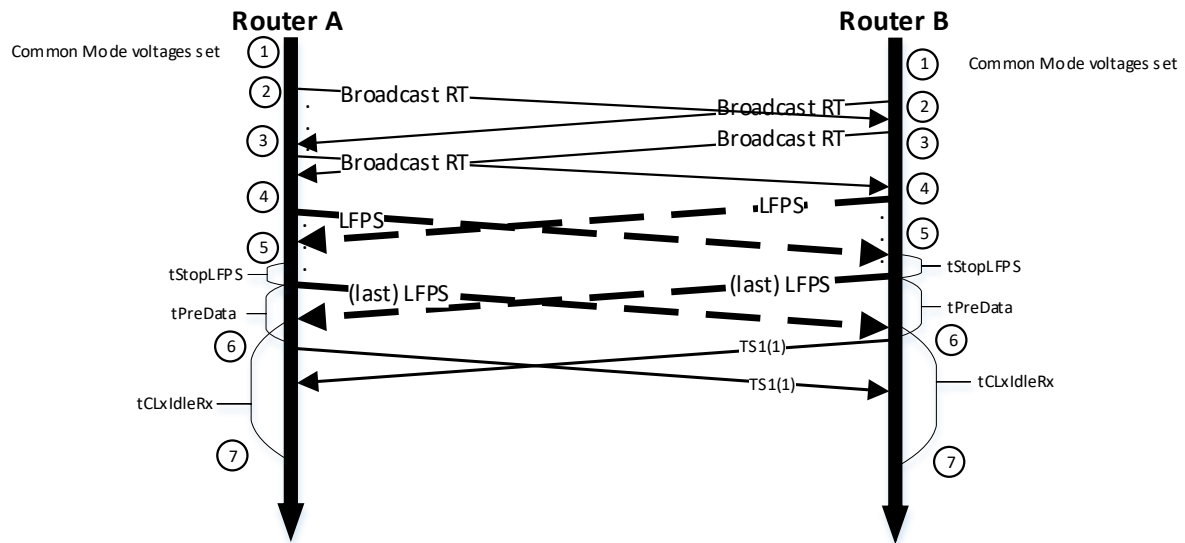
- a. Router A shall set the *Start TxFFE* bit in the Tx Status byte of the Gen 4 TxFFE register in the SB Register Space of the adjacent Router/Re-timer to indicate that it is ready to start the TxFFE Receiver flow described in Section 4.1.2.5.1.2.
- b. Router A's USB4 Port shall send LFPS on the Lane 0 transmitter. Transmitting the LFPS shall start after common voltages are set.
- c. Router A's USB4 Port shall stop sending LFPS within $t_{\text{StopLFPS1}}$ time after all the following conditions are met:
 - Router A's USB4 Port receiver detects LFPS on the Lane 0 Adapter.
 - Router A's USB4 Port sent at least 16 LFPS cycles on the Lane 0 transmitter after detected LFPS on the Lane 0 receiver.
- d. After the Lane 0 transmitter stops sending LFPS, it shall return to Electrical Idle for t_{PreData} , then all enabled transmitters shall start sending back-to-back Gen 4 TS1 with the *Indication* field set to 1h.

Note: Router A's USB4 Port receivers of Lanes other than Lane 0, may ignore any data before Router A's USB4 Port transmitters start sending back-to-back Gen 4 TS1 with the indication field set to 1h following the phase of Electrical Idle for t_{PreData} .

- e. After Router A's receiver detects the last LFPS cycle on the Lane 0 Adapter, all enabled receivers shall be enabled for high-speed signal reception. The receivers shall be enabled $t_{\text{CLxIdleRx}}$ time after the end of the last LFPS cycle is received.
- f. Router A's USB4 Port goes to Phase 5.

Figure 4-7 shows an example of the LFPS behavior in Phase 4.

Figure 4-7. Example of LFPS Behavior in Gen 4 Link



The following describes the steps shown in Figure 4-7:

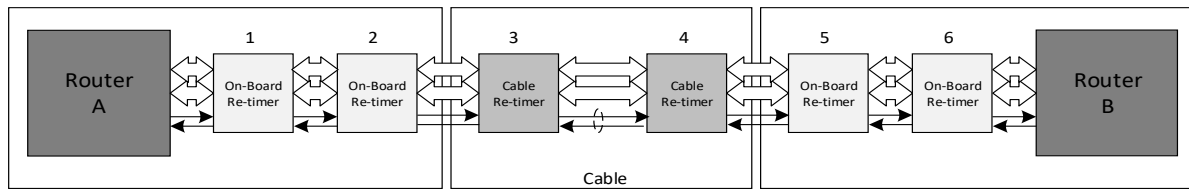
1. Router A has Common Mode voltages set.
2. Router A sends Broadcast RT transactions.
3. Router A receives Broadcast RT transaction.
4. Router A sends LFPS after sending and receiving Broadcast RT Transactions.
5. Router A detected LFPS and sent more than 16 LFPS cycles, it stops sending LFPS within t_{StopLFPS} .
6. t_{PreData} after having stopped sending LFPS Router A enables the USB4 Port's transmitters and starts sending Gen 4 TS1 with the *Indication* field set to 1h.
7. $t_{\text{CLxIdleRx}}$ after detecting last LFPS, Router A enables the USB4 Port's receivers, move to Phase 5 and transitions to Training state.

The behavior described in the example above is also relevant to Router B's behavior.

4.1.2.5 Phase 5 – Link Equalization

The fifth phase of Lane Initialization consists of negotiating transmitter Feed-Forward Equalization (TxFFE) parameters between each Router or Re-timer and a Router or Re-timer adjacent to it. During TxFFE negotiation, the receiver cycles through one or more of the potential Preset numbers defined in Table 3-4. The receiver examines its behavior for each Preset and selects one Preset value to use. The receiver may follow any order while cycling through the Preset numbers.

Figure 4-8 shows two Routers that share a Link that includes six Re-timers. In Figure 4-8, Router A's transmitters perform TxFFE negotiation with the receivers of On-Board Re-timer 1. The transmitters in On-Board Re-timer 6 perform TxFFE negotiation with the receivers of Router B.

Figure 4-8. Progression of Link Equalization

Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.1. A Router shall use Addressed RT Transactions with the *Index* field set to 0 to access the SB Register Space of the adjacent component, which can be either an On-Board Re-timer, a Cable Re-timer, or Router B.

Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.1.2. The Router shall use Addressed RT Transactions with the *Index* field set to 0b to access the SB Register Space of the adjacent component, which can be either an On-Board Re-timer, a Cable Re-timer, or Router A.

Note: TxFFE negotiation is executed only after a disconnect and not when exiting a CLx state or during Recovery flows.

A Router shall set the *Clock Switch Done* bit to 1b in the SB Register Space of the Adapters of a USB4 Port after all the USB4 Port's receivers complete the equalization flow.

The equalization flow for Re-timers is defined in the USB4 Re-Timer Specification.

4.1.2.5.1 Symmetric TxFFE Negotiation

During symmetric TxFFE negotiation, the transmitter negotiates TxFFE parameters with a connected receiver. Both the transmitter and receiver can issue commands to access the SB Register Space of their negotiation partner.

4.1.2.5.1.1 Transmitter Flow

The transmitter flow for a Gen 2 or Gen 3 Link is described in Section 4.1.2.5.1.1.1.

The transmitter flow for a Gen 4 Link is described in Section 4.1.2.5.1.1.2.

4.1.2.5.1.1.1 Gen 2 and Gen 3 Transmitter Flow

1. The transmitter shall start with the following default values in the *Tx Status* byte of the TxFFE register
 - *Tx Active* bit = 1b (see Section 4.1.2.4).
 - *Request Done* bit = 0b.
2. The transmitter shall read the *Rx Status & TxFFE Request* byte of the receiver. To do this, the transmitter sends a read Command that targets the receiver's TxFFE register.
3. On reception of a Response from the receiver, the transmitter shall do the following:
 - If *Rx Locked*=1, then negotiation is complete and no further TxFFE negotiation steps are taken.
 - Else, if *New Request*=0, the receiver has not provided a new request yet. The transmitter shall retry Step 2 within tPollTXFFE of receiving the Response.
 - Else, this is a new request to update TxFFE parameters. Continue on to Step 4.

4. The transmitter shall update its transmitter parameters based on the new parameters in the received Response. To do this, the transmitter loads one of 16 predefined TxFFE configurations that matches the *TxFFE Request* field in the Response. Table 3-4 contains the structure of the Transmit Equalization Presets.
 - The transmitter shall update its *Tx Status* byte with the following values:
 - *TxFFE Setting* = the index (from 16 possible values) loaded above to the TxFFE configuration configured at the transmitter.
 - *Request Done* = 1b.

It is recommended that the transmitter loads the requested TxFFE Preset and updates Tx Status byte within 1 ms from reception of the new request to update TxFFE parameters.
5. The transmitter shall read the *Rx Status & TxFFE Request* byte of the receiver. To do this, the transmitter sends a read Command that targets the receiver's TxFFE register.
6. On reception of a Response from the receiver, the transmitter shall do the following:
 - If *New Request*=1, the receiver is still trying to lock on a previous request. The transmitter shall retry Step 5 within tPollTXFFE of receiving the Response.
 - Else, the transmitter shall set the *Request Done* bit in the *Tx Status* byte to 0b, and return to Step 2.

4.1.2.5.1.1.2 Gen 4 Transmitter Flow

1. When the *New Request* bit is set to 1b in the local *Gen 4 Partner Rx Status & TxFFE Request* byte, the transmitter shall do the following:
 - a. Load one of the ~~50-42~~ predefined Gen 4 TxFFE configurations that matches the *Gen 4 TxFFE Request* field.
 - b. When using the requested Preset chosen by the receiver, set the *Request Done* bit to 1b and the *Gen 4 TxFFE Setting* field to the index loaded above in the *Gen 4 Partner Tx Status* byte of its adjacent Router/Re-timer. To do this, the transmitter sends a write Command that targets the Link Partner's *Gen 4 TxFFE* register within tTxFFEResponse after receiving the write Command that set *New Request* bit to 1b.
2. When the *New Request* bit is set to 0b in the *Gen 4 Partner Rx Status & TxFFE Request* byte, the transmitter shall set *Request Done* bit to 0b in the *Gen 4 Partner Tx Status* byte of its adjacent Router/Re-timer. To do this, the transmitter sends a write Command that targets the Link Partner's *Gen 4 TxFFE* register within tTxFFEResponse after receiving the write Command that set *New Request* bit to 0b.
3. Go back to step 1.

Although the flow described above is independent for each transmitter, after receiving a write Command that sets the *New Request* bit to 1b in more than one transmitter, it is recommended to wait until all the relevant transmitters use the requested Presets and then send one write Command to set the appropriate *Request Done* bit.

4.1.2.5.1.2 Receiver Flow

The receiver flow for Link in Gen 2 or Gen 3 is described in Section 4.1.2.5.1.2.1. The receiver flow for Link in Gen 4 is described in Section 4.1.2.5.1.2.2.

4.1.2.5.1.2.1 Gen 2 and Gen 3 Receiver Flow

1. The receiver shall start with the following default values in the *Rx Status & TxFFE Request* byte of the TxFFE register:
 - *Rx Locked* = 0b.
 - *New Request* bit = 0b.
 - *Rx Active* bit = 0b.
2. The receiver shall read the transmitter's *Tx Status* byte. It does so by sending a read Command to the transmitter that targets its TxFFE register.
3. On reception of a Response from the transmitter, the receiver shall do the following:
 - If *Tx Active* = 1b, then enable the receiver, set the *Rx Active* bit to 1b, and continue on to Step 4.
 - Else, repeat Step 2 within tPollTXFFE of receiving the Response.
4. The receiver shall evaluate its receiver behavior and shall set the *Rx Locked* bit to 1b if equalization is complete.
5. The receiver shall do the following:
 - If *Rx Locked* = 1, then TXFFE negotiation is complete and no further negotiation steps are taken.
 - Else, the receiver shall:
 - Select a new set of TxFFE parameters and shall set the *TxFFE Request* field to the index of the selected set of TXFFE parameters.
 - Set the *New Request* bit to 1b.
 - Continue with the steps below.
6. The receiver shall read the transmitter's *Tx Status* byte. It does so by sending a read Command to the transmitter that targets its TxFFE register.
7. On reception of a Response from the transmitter, the receiver shall do the following:
 - If (*Tx Active* = 1b) AND (*Request Done* = 1b) AND (*TxFFE Setting* = value of *TxFFE request* in the local *Rx Status & TxFFE Request* byte), then continue on to Step 8.
 - Else, repeat Step 6 within tPollTXFFE of receiving the Response.
8. The receiver shall evaluate its receiver behavior and set the *Rx Locked* bit to 1b if equalization is complete.
9. The receiver shall set the *New Request* bit to 0b.
10. The receiver shall read the transmitter's *Tx Status* byte by sending a read Command to the transmitter that targets its TxFFE register.
11. On reception of a Response from the transmitter, the receiver shall do the following:
 - If (*Tx Active* = 1b) and (*Request Done* = 0b), then go to Step 5.
 - Else, repeat Step 10 within tPollTXFFE of receiving the Response.

4.1.2.5.1.2 Gen 4 Receiver Flow

1. When the *Start TxFFE* field is set to 1b in the local *Gen 4 Partner Tx Status* byte, the receiver shall continue to step 2.
2. The receiver shall select a set of TxFFE parameters defined in Table 3-24. It shall set the *Gen 4 TxFFE Request* field to the selected Preset (0-41) and set the *New Request* bit to 1b in the *Gen 4 Rx Status & TxFFE Request* byte of its adjacent Router/Re-timer. To do this, the receiver sends a write Command that targets the Link Partner's Gen 4 TxFFE register.
3. When the *Request Done* bit is set to 1b in the local *Gen 4 Partner Tx Status* byte, the receiver shall:
 - a. Set the *New Request* bit to 0b in the *Gen 4 Rx Status & TxFFE Request* byte of its adjacent Router/Re-timer. To do this, the receiver sends a write Command that targets the Link Partner's Gen 4 TxFFE register.
 - b. Verify that the *Gen 4 TxFFE Setting* field in the local *Gen 4 Partner Tx Status* byte is set to the same value it selected in step 2. If not, go to step 4.
 - c. Evaluate its receiver behavior. If the equalization is complete, go to step 5.

Note: If the Router is adjacent to a USB Type-C connector and is connected to its adjacent Router/Re-timer via an LRD Cable, the receiver should take into account the self-tuning of the LRD as described in the USB Type-C Specification.

4. The receiver shall go to step 2 after the *Request Done* bit is set to 0b in the local *Gen 4 Partner Tx Status* byte.
5. The receiver shall clear the Start TxFFE bit after the Request Done bit is set to 0. TxFFE negotiation is done.

4.2 Logical Layer State Machine

The behavior of the Logical Layer in an Adapter is described by the state machine defined in Section 4.2.1. Section 4.2.1.6.5.4 defines the behavior of a USB4 Link and how the Link is affected by Adapter state.

4.2.1 Lane Adapter State Machine

The state machine in Figure 4-9 describes the behavior of the Logical Layer in a Lane Adapter when the Link in Gen 2 or Gen 3. The state machine in Figure 4-10 describes the behavior of the Logical Layer in a Lane Adapter when the Link in Gen 4. A detailed description of the states and transitions between states follows.

- Disabled state – The Lane Adapter disables the Lane.
- CLd state – Lane Adapter transmitter and receiver are inactive.
- Training state – The Lane Adapter performs Symbol synchronization and transfer of Lane parameters.
- CL0 state – The Lane Adapter can transmit and receive Transport Layer Packets across the Lane.
- Lane Bonding state – bonds two Single-Lane Links into a Symmetric Link.

Note: This state does not exist for a Gen 4 Link. Instead, Lanes are bonded as part of the Lane Initialization process.

- CL0s, CL1, CL2 states – Low Power states.

Figure 4-9. The Lane Adapter State Machine for a Gen 2 and Gen 3 Link

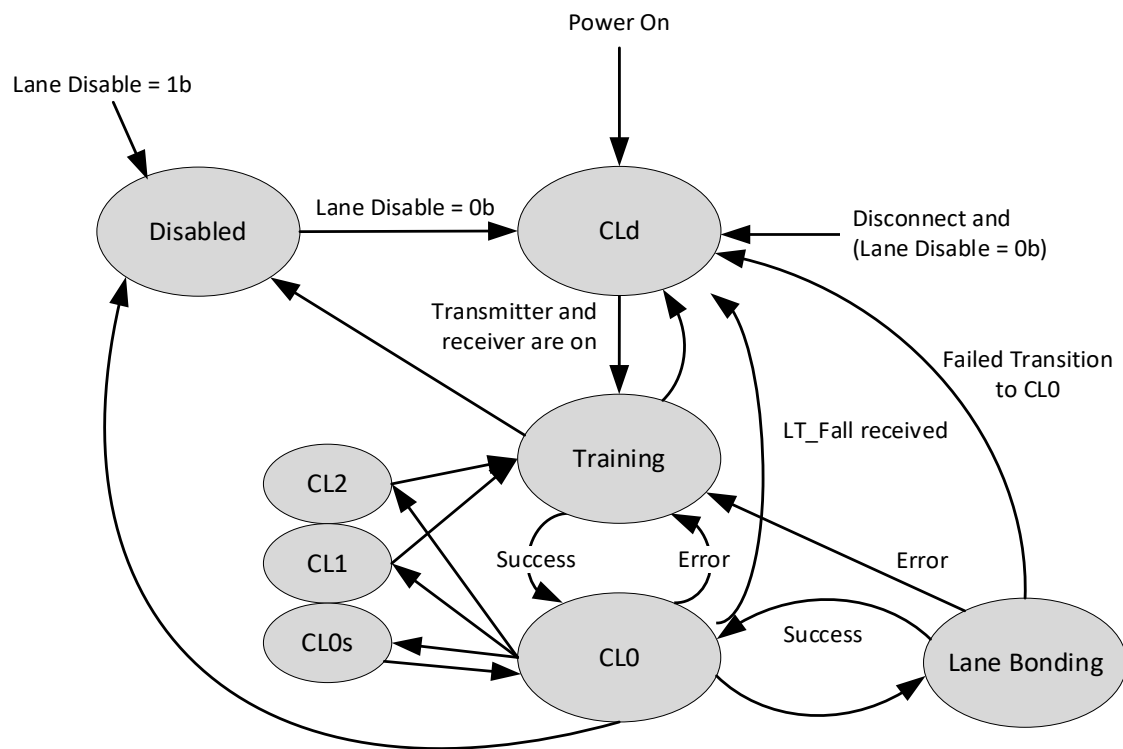
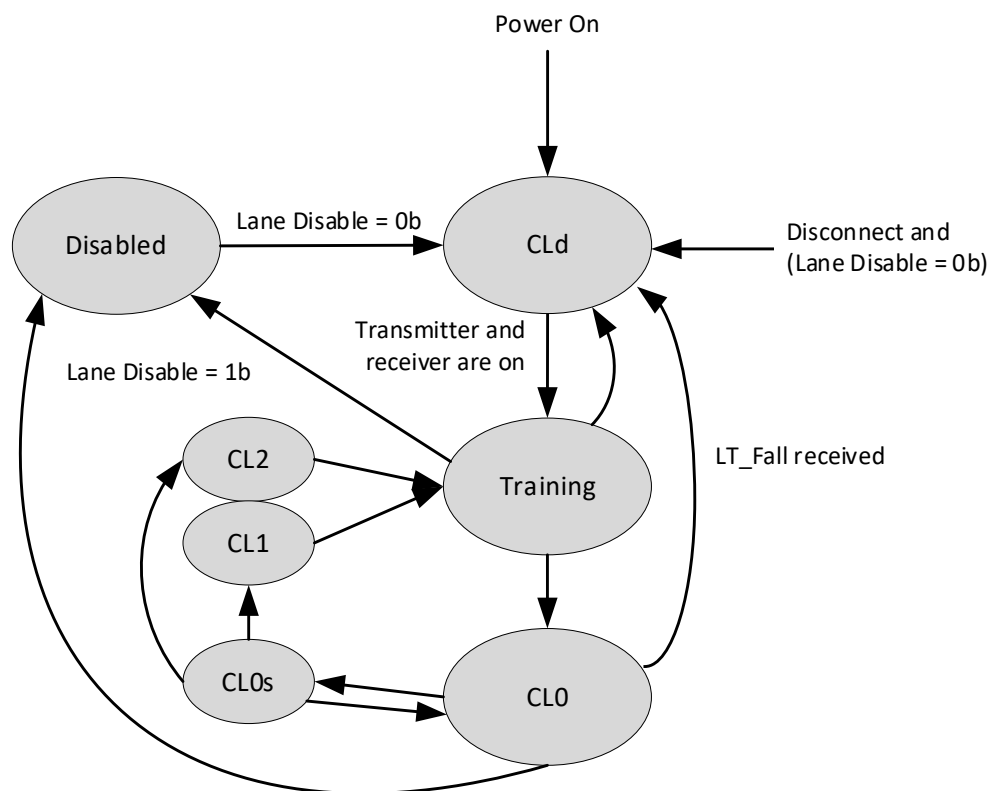


Figure 4-10. The Lane Adapter State Machine for a Gen 4 Link



4.2.1.1 Disabled

4.2.1.1.1.1 Entry to State

An Adapter shall enter this state from CLd state, Training state or CL0 state when the *Lane Disable* bit in the Lane Adapter Configuration Capability is set to 1b. See Section 4.4.6 for details.

A Lane Adapter shall set the *Plugged* bit to 0b upon transitioning to Disabled state.

4.2.1.1.1.2 Behavior in State

Lane common mode voltages do not need to be maintained while in this state.

4.2.1.1.1.3 Exit from State

An Adapter shall exit this state when the *Lane Disable* bit in the Lane Adapter Configuration Capability is set to 0b. See Section 4.4.6 for details.

Note: This is the only event on which the Lane Adapter exits the Disabled state.

A disabled Adapter shall stay in the Disabled state for a minimum of t_{Disabled} . If the *Lane Disable* bit is set to 0b less than t_{Disabled} after sending the LT_Fall Transaction, the Adapter shall not transition to the CLd state until t_{Disabled} has elapsed.

4.2.1.2 CLd

4.2.1.2.1 Entry to State

A Lane Adapter shall enter this state on any of the following events:

- Router power-on.
- The USB4 Port is disconnected and *Lane Disable* bit in the Lane Adapter Configuration Capability is set to 0b (see Section 4.4.5).
- Router enters sleep state (see Section 4.5.1).
- The USB4 Port starts the Gen 4 Link Recovery flow (see Section 4.4.7).

In addition to the events listed above, a Lane Adapter that is not the Upstream Adapter shall enter this state on any of the following events:

- Adapter exits from the Disabled state.
- Adapter receives an LT_Fall Transaction.

A Lane Adapter shall set the *Plugged* bit to 0b upon transitioning to the CLd state unless the transition is part of Gen 4 Recovery flow.

4.2.1.2.2 Behavior in State

During this state, Lane common mode voltages do not need to be maintained. A Lane Adapter is in this state when Lane Initialization begins. Lane Initialization is described in Section 4.1.2.

Unless specified otherwise, a Lane Adapter that enters this state due to a disconnect shall perform Lane Initialization starting from Phase 1. A Lane Adapter shall set the *Plugged* bit to 0b in this state if it detects a disconnect.

A Lane Adapter that enters this state from the Disabled State performs Lane Initialization after the Lane is enabled. The Lane Adapter shall start Lane Initialization from Phase 4. The USB4 Port shall maintain any state acquired in Phases 1 through 3 of previous Lane Initialization. See Section 4.4.6 for more information on Lane Disable and Enable.

A Lane Adapter that enters this state due to the Router entering sleep state performs Lane Initialization after a wake event. The Lane Adapter shall start Lane Initialization from Phase 2. The Adapter shall start Lane Initialization with the last set of TxFFE parameters used prior to entry to sleep state. See Section 4.4.7 for more information on Router sleep and wake.

Note: The Link Partner may not necessarily start Phase 5 with the last set of TxFFE parameters used prior to entry to sleep state. Therefore, a receiver needs to verify the TxFFE parameters initiated at the Link Partner's transmitter (see Section 4.5.4).

A Lane Adapter that enters this state due to Link training timeout shall perform Lane Initialization starting from Phase 1.

4.2.1.2.3 Exit from State

A Lane Adapter shall exit this state when its transmitter is transmitting (completion of Phase 4 of Lane Initialization, see Section 4.1.2.4) and its receiver is enabled.

After exiting the CLd state, a Lane Adapter that negotiated a Gen 2 or Gen 3 Link shall transition to the Training.LOCK1 sub-state. A Lane Adapter that negotiated a Gen 4 Link shall transition to the Training.TS1 sub-state after exiting CLd state.

4.2.1.3 Training

4.2.1.3.1 Entry to State

A Lane Adapter shall enter this state on any of the following events:

- After exiting the CLd state.
- For a Gen 2 or Gen 3 Link, when recovering from a USB4 Link error.
- After exiting the CL2 or CL1 states.

4.2.1.3.2 Behavior in State

During this state Symbols are synchronized and Lane parameters are transferred between the two ends of the Lane. The transmitter and receiver are on while in this state.

4.2.1.3.2.1 Gen 2 and Gen 3 Behavior

A Lane Adapter that negotiated a Gen 2 or Gen 3 Link shall follow the Training sub-state machine described in Figure 4-11 with the behavior described in Table 4-31 and the sub-state transitions described in Table 4-32. If the transition to Training state is from a CLx state, the sub-state transitions shall occur within tTrainingTransition time from receiving the last bit of the relevant Symbols.

Figure 4-11. Gen 2 and Gen 3 Training Sub-State Machine

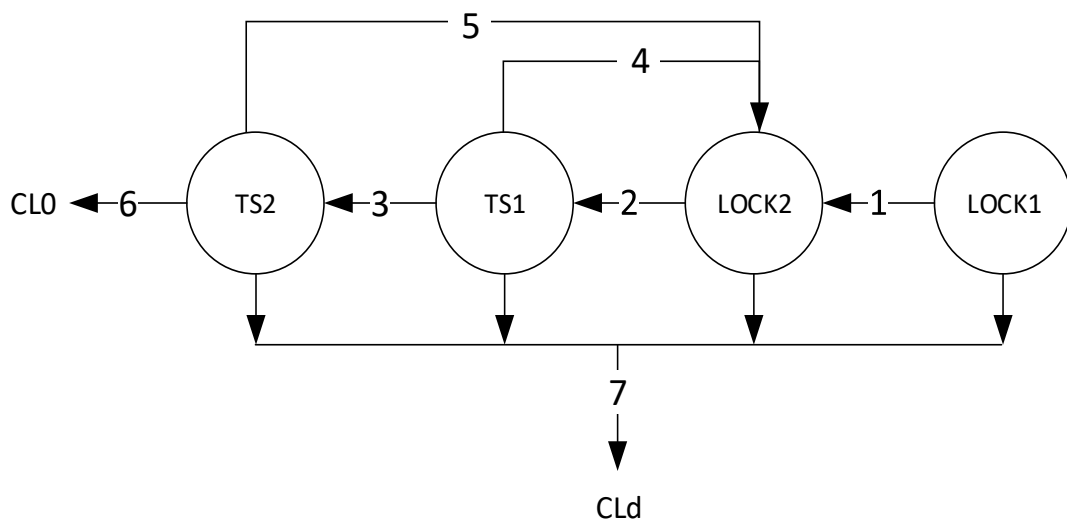


Table 4-31. Transmitter Behavior in Gen 2 and Gen 3 Training Sub-states

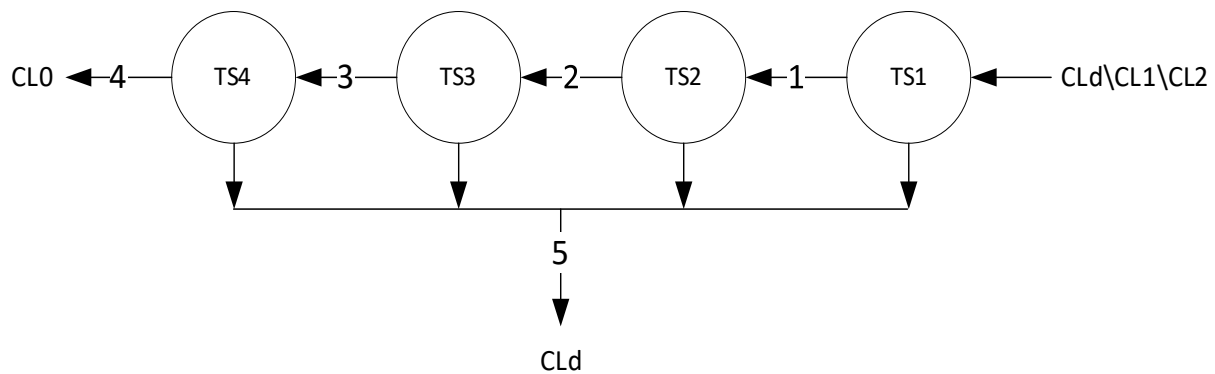
State	Transmitter Behavior
LOCK1	Transmitter shall send back-to-back SLOS1. When a Lane Adapter transitions to the Training state from the CL0 state, its transmitter may transmit up to 16 Symbol Times of random bits before sending the first SLOS1 that is not RS-FEC encoded.
LOCK2	Transmitter shall send back-to-back SLOS2.
TS1	Transmitter shall send back-to-back TS1 Ordered Sets.
TS2	Transmitter shall send back-to-back TS2 Ordered Sets.

Table 4-32. Gen 2 and Gen 3 Training Sub-State Machine Transitions

Transition	From State	To State	Conditions ¹
1	LOCK1	LOCK2	<ul style="list-style-type: none"> Received 2 SLOS Symbols (SLOS1 and/or SLOS2) in a row. Sent at least 2 complete SLOS1. Receiver completed TxFFE negotiation (i.e. <i>Rx Locked</i> = 1b).
2	LOCK2	TS1	<ul style="list-style-type: none"> Received 2 SLOS2 Symbols in a row. Sent at least 2 complete SLOS2. It is recommended to count the transmitted SLOS2 after receiving 2 SLOS2 Symbols in a row.
3 ²	TS1	TS2	Gen 2: <ul style="list-style-type: none"> Received 2 TS1 Ordered Sets in a row. Sent at least 32 TS1 Ordered Sets. Gen 3: <ul style="list-style-type: none"> Received 2 TS1 Ordered Sets in a row. Sent at least 16 TS1 Ordered Sets.
4	TS1	LOCK2	<ul style="list-style-type: none"> Received 2 SLOS1 Symbols in a row.
5	TS2	LOCK2	<ul style="list-style-type: none"> Received 2 SLOS Symbols (SLOS1 and/or SLOS2) in a row.
6	TS2	CL0	Gen 2: <ul style="list-style-type: none"> Received 2 TS2 Ordered Sets in a row. Sent at least 16 TS2 Ordered Sets. Gen 3: <ul style="list-style-type: none"> Received 2 TS2 Ordered Sets in a row. Sent at least 8 TS2 Ordered Sets.
7	Any	CLd	<ul style="list-style-type: none"> Adapter remains in Training state for tTrainingAbort1 or tTrainingAbort2 time.
8	Any	LOCK1	<ul style="list-style-type: none"> A timeout error (see Section 4.4.2). <i>Note: This transition is optional.</i>
Notes: 1. All conditions need to be met before transition takes place. 2. Router may also optionally transition from TS1 state to TS2 state after receiving 2 TS2 Ordered sets and sending the required number of TS1 Ordered Sets.			

4.2.1.3.2.2 Gen 4 Behavior

A Lane Adapter that negotiated a Gen 4 Link shall follow the Training sub-state machine described in Figure 4-12 with the behavior described in Table 4-33 and the sub-state transitions described in Table 4-34. If the transition to Training state is from CLx states, the sub-state transitions shall occur within tTrainingTransition time from receiving the last bit of the relevant Symbols. All active transmitters shall transmit the same Training Sequence (TS). Receivers may lose alignment and re-align in each sub-state.

Figure 4-12. Gen 4 Training Sub-State Machine**Table 4-33. Transmitter Behavior in Gen 4 Training Sub-states**

State	Transmitter Behavior
TS1	Transmitters shall send back-to-back Gen 4 TS1. The <i>Indication</i> field shall be 1h while any receiver is not ready for PAM3. <i>Indication</i> field shall be 2h when all enabled receivers are ready for PAM3.
TS2	Transmitters shall send back-to-back Gen 4 TS2. The <i>Indication</i> field shall be 3h while any receiver is executing the TxFFE negotiation. <i>Indication</i> field shall be 4h after all enabled receivers complete TxFFE negotiation <u>and the Port is ready for Clock Switch</u> .
TS3	Transmitters shall send back-to-back Gen 4 TS3. If not in Compliance mode, the <i>Indication</i> field shall be 5h before all enabled receivers detect Gen 4 TS3. The <i>Indication</i> field shall be 6h when in Compliance mode or after all enabled receivers detect Gen 4 TS3.
TS4	Transmitters shall send back-to-back Gen 4 TS4. The <i>Counter</i> field value shall be 0h before activating SSC and tSSCActivated time after activating SSC. The <i>Counter</i> field shall be incremented from 1h to Fh on each Gen 4 TS4, starting simultaneously on all enabled transmitters, tSSCActivated time after SSC is activated. Transmitters shall activate SSC within tActivateSSC time after sending the first trit of the first TS4.

Table 4-34. Gen 4 Training Sub-State Machine Transitions

Transition	From State	To State	Conditions ¹
1	TS1	TS2	<ul style="list-style-type: none"> If not in RX Compliance mode, received Gen 4 TS1 with the <i>Indication</i> field set to 2h or Gen 4 TS2 on all enabled receivers. If in RX Compliance mode, received SET_RX_COMPLIANCE Port Operation with the <i>Transmitter State</i> field set to 010b. Sent at least 16 Gen 4 TS1 with the <i>Indication</i> field set to 2h on all enabled transmitters. <p><i>Note: This means the receiver completed TxFFE negotiation in PAM2 and is ready for PAM3.</i></p>
2	TS2	TS3	<ul style="list-style-type: none"> If not in RX Compliance mode: <ul style="list-style-type: none"> All enabled Receivers completed TxFFE negotiation. Received Gen 4 TS2 with the <i>Indication</i> field set to 4h or Gen 4 TS3 on all enabled receivers. If in RX Compliance mode, the receiver under test completed TxFFE negotiation. Sent at least 16 Gen 4 TS2 with the <i>Indication</i> field set to 4h on all enabled transmitters.
3	TS3	TS4	<ul style="list-style-type: none"> If not in RX Compliance mode and not in TX Compliance mode, received Gen 4 TS3 with the <i>Indication</i> field set to 6h or Gen 4 TS4 on all enabled receivers. Sent at least 16 Gen 4 TS3 with the <i>Indication</i> field set to 6h on all enabled transmitters.

Transition	From State	To State	Conditions ¹
4	TS4	CL0	<ul style="list-style-type: none"> Sent Gen 4 TS4 with the <i>Counter</i> field set to Fh.
5	Any	CLd	<ul style="list-style-type: none"> Adapter remains in Training state for tTrainingAbort1 or tTrainingAbort2² time.
Notes: <ol style="list-style-type: none"> All conditions need to be met before a transition takes place. For a Gen4 Link that has the Enable Gen 4 Link Recovery bit in PORT_CS_19 set to 0b, if the Adapter transitions from CLx state to Training state the count starts from the CLx Exit event (see Section 4.2.1.6.5.4) and not from the entering to Training state. 			

During Lane Initialization a USB4 Port~~When the Port is not in RX Compliance mode or TX Compliance mode it~~ shall meet the following timing requirements:

- Transition to the TS2 sub-state within tGen4TS1 time after entering the TS1 sub-state.
- Transition to the TS3 sub-state within tGen4TS2 time after entering the TS2 sub-state.

During CLx exit flow a USB4 Port shall meet the following requirements:

- Start transmitting Gen 4 TS1 with *Indication* field set to 2h within tRXLock + tTrainingTransition time from receiving the first Gen 4 TS1.
- Start transmitting Gen 4 TS2 with *Indication* field set to 4h within tGen4TS2Lock + tTrainingTransition time after receiving the first Gen 4 TS2.
- Start transmitting Gen 4 TS3 with *Indication* field set to 5h within tLFPStoTS3 time after detecting the first LFPS on the USB Type C-Port.

The following formulas describes tLFPStoTS3 for a Router Assembly with *N_{obr}* On-Board Retimers:

$$tLFPStoTS3 = tWarmUpCLx + 32xtPeriod + 2xtStopLFPS2 + tGen4TS2Lock + tRxLock + 3xtTrainingTransition + N_{obr} \times (tSwitchNoSSC + tOBCLxForwardLFPS)$$

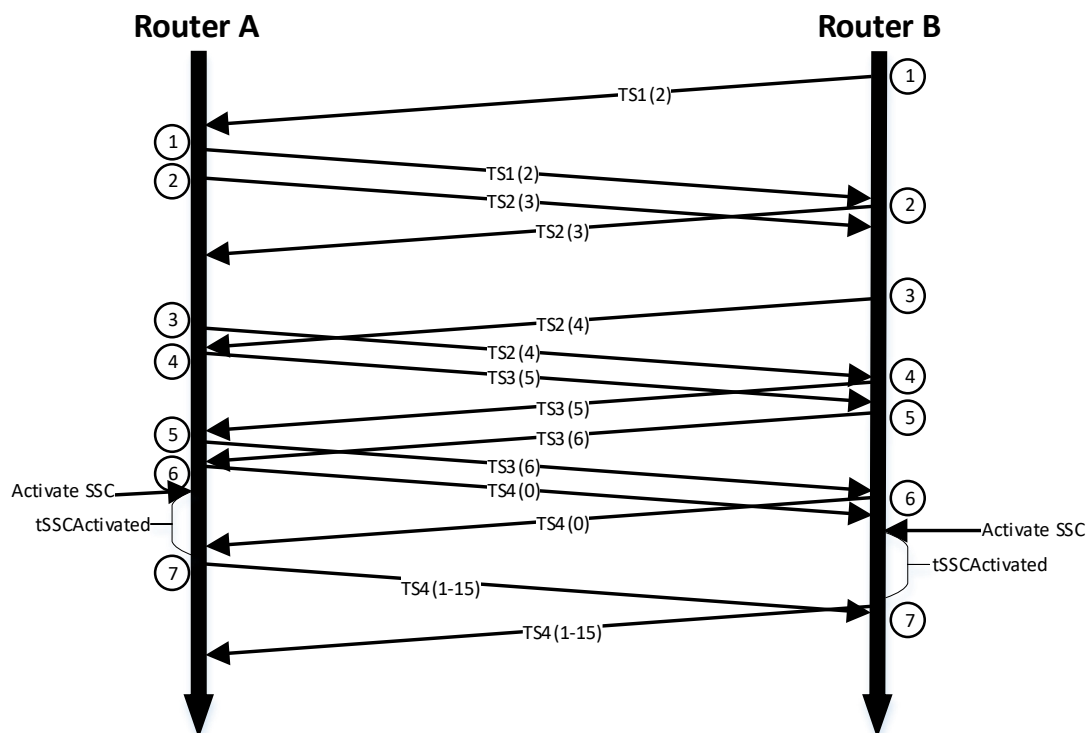
Notes:

- tWarmUpCLx represents tWarmUpCL1 or tWarmUpCL2 for CL1 or CL2 exit respectively.
- tOBCLxForwardLFPS represents tOBCL1ForwardLFPS or tOBCL2ForwardLFPS for CL1 or CL2 respectively. These vaues stand for the LFPS forwarding by on-board retimers in a Router Assembly as described in the USB4 Re timer Specification.
- A USB4 Port may meet the requirements of Table 4-33 and start transmitting Gen 4 TS1 with *Indication* field set to 2h before receiving the first Gen 4 TS1.

A USB4 Port shall start RS-FEC encoding, Pre-coding, and scrambling upon transitioning from the TS4 sub-state to CL0 state.

Note: A receiver that finished PAM2 TxFFE negotiation should detect TS2 before sending a new TxFFE Preset for PAM3 TxFFE negotiation.

Figure 4-13 shows an example of the flow executed in Training state.

Figure 4-13. Example of Gen 4 Training Sub-State Transitions

The following describes the steps in Figure 4-13:

1. When the receiver is ready for the transition to PAM3, the transmitter sends back-to-back Gen 4 TS1 with the *Indication* field set to 2h.
2. After the transmitter sends at least 16 Gen 4 TS1 with the *Indication* field set to 2h and the receiver detects Gen 4 TS1 with the *Indication* field set to 2h, the transmitter sends back-to-back TS2 with the *Indication* field set to 3h.
3. When the receiver finishes its equalization, the transmitter sends back-to-back Gen 4 TS2 with the *Indication* field set to 4h.
4. After the transmitter sends at least 16 Gen 4 TS2 with the *Indication* field set to 4h and the receiver detects Gen 4 TS2 with the *Indication* field set to 4h, the transmitter sends back-to-back TS3 with the *Indication* field set to 5h.
5. After the receiver detects Gen 4 TS3 with the *Indication* field set to 5h, the transmitter sends back-to-back TS3 with the *Indication* field set to 6h.
6. After the transmitter sends at least 16 Gen 4 TS3 with the *Indication* field set to 6h and the receiver detects Gen 4 TS3 with the *Indication* field set to 6h, the transmitter sends back-to-back TS4 with *Counter* set to 0h. The transmitter then transitions to a clock with SSC.
7. tSSCActivated time after the transmitter started using the clock with SSC, it sends back-to-back Gen 4 TS4 with the *Counter* value increasing from 1h to Fh.

After sending Gen 4 TS4 with the *Counter* field set to Fh, the Lane Adapter activates RS-FEC encoding, pre-coding, and scrambling. The Lane Adapter then transitions to CL0 state. The first RS-FEC block sent by the USB4 Port is a De-skew Block as defined in Section 4.4.4.

The following is an informative description of Phase 5 of Lane Initialization for a Gen 4 Link where the Lane Adapters are in the Training state (see Section 4.1.2.5 and 4.2.1.3.2 for more information):

- Phase 5 starts with the Lane Adapters in the TS1 sub-state. If one or more enabled receivers are not ready to receive PAM3 signaling, all enabled transmitters send back-to-back Gen 4 TS1 with the *Indication* field set to 1h. During this time each enabled receiver evaluates its signal and can ask the transmitter in its Link Partner to modify its configuration using TxFFE negotiation as described in Section 4.1.2.5.1. When all enabled receivers are ready to receive PAM3 signaling, all enabled transmitters change the *Indication* field in the Gen 4 TS1 to 2h. Note that this doesn't mean that the receivers finished the TxFFE negotiation—the receivers may continue to ask for new configurations while in the TS2 sub-state. After all enabled receivers detect Gen 4 TS1 with the *Indication* field set to 2h and all enabled transmitters have transmitted at least 16 Gen 4 TS1 with the *Indication* field set to 2h, the Lane Adapter moves to TS2 sub-state. In the TS1 sub-state, the transmitters use PAM2 signaling.
- In the TS2 sub-state, all enabled transmitters send back-to-back Gen 4 TS2 with the *Indication* field set to 3h while any receiver is performing TxFFE negotiation. When all enabled receivers finish TxFFE negotiation, the transmitters change the *Indication* field in the Gen 4 TS2 to 4h. After all enabled receivers detect Gen 4 TS2 with the *Indication* field set to 4h and all enabled transmitters have transmitted at least 16 Gen 4 TS2 with the *Indication* field set to 4h, all the Lane Adapters transition to the TS3 sub-state.
- In the TS3 sub-state, all enabled transmitters send back-to-back Gen 4 TS3 with the *Indication* field set to 5h until all enabled receivers detect Gen 4 TS3. During this time, if there are any Re-timers on the Link, the Gen 4 TS3 propagate through the Re-timers and cause each one of them to switch to Forward state and transmit received data with the recovered clock instead of a generated Gen 4 TS2 with the local clock. This behavior is described in the USB4 Re-Timer Specification. When all enabled receivers detect Gen 4 TS3, meaning all Re-timers on the Link made the switch to Forward state, all enabled transmitters change the *Indication* field in the Gen 4 TS3 to 6h. After all the enabled receivers detect Gen 4 TS3 with the *Indication* field set to 6h and all enabled transmitters have sent at least 16 Gen 4 TS3 with the *Indication* field set to 6h, the Lane Adapter moves to the TS4 sub-state.
- In the TS4 sub-state, the transmitter sends back-to-back Gen 4 TS4 with the *Counter* field set to 0h for as long as SSC is disabled. After enabling SSC, the transmitter keeps the *Counter* field set to 0h for tSSCActivated time. While transmitting back-to-back Gen 4 TS4 with the *Counter* field set to 0h, the transmitter transitions to a clock with SSC. tSSCActivated time after enabling SSC, all enabled transmitters change the *Counter* field to a running counter that counts from 1h to Fh. A Gen 4 TS4 with the *Counter* field set to a value other than 0h can be used in the receiver to detect any skew between the enabled Lanes. After sending Gen 4 TS4 with the *Counter* field set to Fh, the Lane Adapter activates RS-FEC encoding, Pre-coding, and scrambling as described in Section 4.3.2. The Lane Adapter then transitions to CL0 and sets the current Link Width in the *Negotiated Link Width* field in Adapter Configuration Space. The first RS-FEC block sent by the USB4 Port is a De-skew Block as defined in Section 4.4.4.

4.2.1.3.3 Exit from State

A Lane Adapter that transitions from CLd state to Training state shall complete training and transition to the CL0 state within tTrainingAbort1 after entering the Training state. If the Adapter does not transition to CL0 state within tTrainingAbort1, the Router shall initiate a Disconnect by driving SBTx to a logical low state for tDisconnectTx.

A Lane Adapter that transitions from a state other than CLd to Training state shall complete training and transition to the CL0 state within tTrainingAbort2 after entering the Training state. For a Gen 4 Link that has the Enable Gen 4 Link Recovery bit in PORT_CS_19 set to 0b, if the Adapter transitions from CLx state to Training state the count starts from the CLx Exit event (see Section 4.2.1.6.5.4) and not from the entering to Training state. If the Adapter does not transition to CL0 state within tTrainingAbort2, the Router shall initiate a Disconnect by driving SBTx to a logical low state for tDisconnectTx.

For a Gen 4 Link that has the *Enable Gen 4 Link Recovery* bit in PORT_CS_19 set to 1b, if the Adapter transitions from CLx state to Training state and does not transition to CL0 state within tTrainingError starting from the CLx Exit event (see Section 4.2.1.6.5.4), the Router shall initiate Gen 4 Link Recovery as described in Section 4.4.7.

A Hot Plug Event Packet shall be sent upon transitioning to CL0 state if all of the following are true:

- The Adapter is part of a Downstream Facing Port.
- The Adapter entered Training state from the CLd state.
- The transition is not part of a Gen 4 Recovery flow.

A Lane Adapter shall set the *Plugged* bit to 1b when it transitions from the Training state to the CL0 state.

4.2.1.3.4 Gen 2 and Gen 3 Ordered Sets

4.2.1.3.4.1 SLOS1 and SLOS2

The Symbol Lock Ordered Sets (SLOS) are used to establish bit and Symbol lock, both for initial Lane training and for re-establishing bit/Symbol lock on a previously trained USB4 Link. These Ordered Sets have a high number of transitions to facilitate bit lock and easily detected Symbol boundaries to facilitate Symbol lock. There are two Ordered Sets used for Symbol Lock, SLOS1 and SLOS2, each of which consists of a defined series of bit patterns. The SLOS1 bit pattern is generated using a known pseudo-random binary sequence (PRBS11). A PRBS11 of length 2047 with the following characteristics is used:

- PRBS11 polynomial: $G(x) = x^{11} + x^9 + 1$
- PRBS11 initial state: 400h

The bit pattern for SLOS1 is composed of <0b, 2047 bits of PRBS11>. The bit pattern for SLOS2 is composed of <1b, 2047 bits of logically inverted PRBS11>.

When operating in Gen 2 mode with RS-FEC encoding disabled, SLOS shall be encoded using 64b/66b encoding. When operating in Gen 2 mode with RS-FEC encoding enabled, SLOS that are not RS-FEC encoded shall be encoded using 128b/132b encoding.

When operating in Gen 3 mode, SLOS that are not RS-FEC encoded shall be encoded using 128b/132b encoding.

Section 4.3.1.6 defines the structure of SLOS that are RS-FEC encoded.

The SLOS1 and SLOS2 for 64b/66b encoding are transmitted as 32 66-bit Symbols, where the nth Symbol equals <b10b, n'th 64b word of the bit pattern>. See Table 4-35 for SLOS1 with 64b/66b encoding and Table 4-36 for SLOS2 with 64b/66b encoding.

The SLOS1 and SLOS2 for 128b/132b encoding are transmitted as 16 132-bit Symbols, where the nth Symbol equals <b1010b, n'th 128b word of the bit pattern>. See Table 4-37 for SLOS1 with 128b/132b encoding and Table 4-38 for the SLOS2 with 128b/132b encoding.

Note: A Symbol containing part of a SLOS is referred to as a "SLOS Symbol".

The SLOS1 and SLOS2 shall not be scrambled, and the scrambler shall not advance upon receive/transmit.

When transmitting SLOS1 or SLOS2 using 64b/66b encoding, a Router shall transmit all 32 SLOS Symbols in their entirety. When using 128b/132b encoding, a Router shall transmit all 16 SLOS Symbols in their entirety. A Router shall not transmit an incomplete SLOS.

Table 4-35. SLOS1 (64b/66b Encoding)

Symbol number	Sync Bits	SLOS1 Contents (63:0)
0	10	01000000001010000001000100001010 10100100000001101000001110010001
1	10	10111010111010100010100001010001 00100010101101010000110000100111
2	10	10010111001110010111101110010010 10111011000010101110010000101110
3	10	10010010100110110001111011101100 10101011110000001001100001011111
4	10	00100100011101101011010110001100 01110111101101010010110000110011
5	10	10011111101111000010100110010001 11111010110000100011100101011011
6	10	10000110101100111000111110110110 00101101110100110101001111000011
7	10	10011001101111111110100000001001 00000101101000100110010101111110
8	10	00010000110010100111110001110001 10110110111011011010101101100000
9	10	11011100011101011011010001101100 10111011110010101001110000011101
10	10	10001101011101110001010101101000 00011001000011111010011000100111
11	10	11010111000100010110101010011000 00011111000011000110011110111111
12	10	00101000011100010011011010111101 10001001011101011001010001111000
13	10	10110011010011111100111000011110 11001100101111111100100000011101
14	10	00001101001001110011011101111101 01010001000000101010000100000100
15	10	10100010110001010011101000111010 01011010011001100111111111110000
16	10	00000110000000111100000110011000 11111111011000000101110000100101
17	10	10010110011110011111001111000111 10011011001111101111100010100011
18	10	01000101110010100101110001100101 10111110011010001111100101100011
19	10	10011101101111010110100100011001 10101111111000100000110101000111
20	10	00001011011001001101111011110100 10100100110001101111101110100010
21	10	10100101000001100010001111010101 10010000011110100011001001011111
22	10	01100100010111101010010010000110 11010011101100111010111110100010
23	10	00100101010101100000000111000000 11011000011101110011010101111100
24	10	00010001100010101111010000100100 10010110110110011011011111101101
25	10	00001011001001001111011011100101 10101110011000101111110100100001
26	10	00110100101111001100100111111101 11000001010110001000011101010011
27	10	01000011110010011001110111111101 01000001000010001010010101000110
28	10	00001011110001001001101011011110 00110100110111001111010111100100
29	10	01001110101011101000001010010001 00011010101011100000001011000001
30	10	00111000101110110100101011001100 00111111100110000011111100011000
31	10	01101111001110100111101001110010 0111011101110101010101010000000000

Table 4-36. SLOS2 (64b/66b Encoding)

Symbol number	Sync Bits	SLOS2 Contents (63:0)
0	10	10111111110101111110111011110101 010110111111110010111110001101110
1	10	01000101000101011101011110101110 11011101010010101111001111011000
2	10	01101000110001101000010001101101 01000100111101010001101111010001
3	10	01101101011001001110000100010011 01010100001111110110011110100000
4	10	11011011100010010100101001110011 10001000010010101101001111001100
5	10	01100000010000111101011001101110 00000101001111011100011010100100
6	10	01111001010011000111000001001001 11010010001011001010110000111100
7	10	01100110010000000001011111110110 11111010010111011001101010000001
8	10	11101111001101011000001110001110 01001001000100100101010010011111
9	10	00100011100010100100101110010011 01000100001101010110001111100010
10	10	01110010100010001110101010010111 11100110111100000101100111011000
11	10	00101000111011101001010101100111 11100000111100111001100001000000
12	10	11010111100011101100100101000010 01110110100010100110101110000111
13	10	01001100101100000011000111100001 00110011010000000011011111100010
14	10	11110010110110001100100010000010 1010111011111101010111101111011
15	10	01011101001110101100010111000101 10100101100110011000000000001111
16	10	11111001111111000011111001100111 00000000100111111010001111011010
17	10	01101001100001100000110000111000 01100100110000010000011101011100
18	10	10111010001101011010001110011010 01000001100101110000011010011100
19	10	01100010010000101001011011100110 01010000000111011111001010111000
20	10	11110100100110110010000100001011 01011011001110010000010001011101
21	10	01011010111110011101110000101010 011011111100001011100110110100000
22	10	10011011101000010101101101111001 00101100010011000101000001011101
23	10	11011010101010011111111000111111 00100111100010001100101010000011
24	10	11101110011101010000101111011011 01101001001001100100100000010010
25	10	11110100110110110000100100011010 01010001100111010000001011011110
26	10	11001011010000110011011000000010 00111110101001110111100010101100
27	10	10111100001101100110001000000010 101111101111011101011010111001
28	10	11110100001110110110010100100001 11001011001000110000101000011011
29	10	10110001010100010111110101101110 11100101010100011111110100111110
30	10	11000111010001001011010100110011 11000000011001111100000011100111
31	10	10010000110001011000010110001101 10001000100010101010101111111111

Table 4-37. SLOS1 (128b/132b Encoding)

Symbol number	Sync Bits	SLOS1 Contents (127:0)
0	1010	01000000001010000001000100001010 10100100000001101000001110010001 10111010111010100010100001010001 00100010101101010000110000100111
1	1010	10010111001110010111101110010010 10111011000010101110010000101110 10010010100110110001111011101100 10101011110000001001100001011111
2	1010	00100100011101101011010110001100 01110111101101010010110000110011 10011111101111000010100110010001 11111010110000100011100101011011
3	1010	10000110101100111000111110110110 00101101110100110101001111000011 10011001101111111110100000001001 00000101101000100110010101111110
4	1010	00010000110010100111110001110001 10110110111011011010101101100000 11011100011101011011010001101100 10111011110010101001110000011101
5	1010	10001101011101110001010101101000 00011001000011111010011000100111 11010111000100010110101010011000 00011111000011000110011110111111
6	1010	00101000011100010011011010111101 10001001011101011001010001111000 10110011010011111100111000011110 11001100101111111100100000011101
7	1010	00001101001001110011011101111101 01010001000000101010000100000100 10100010110001010011101000111010 01011010011001100111111111110000
8	1010	00000110000000111100000110011000 11111111011000000101110000100101 10010110011110011111001111000111 10011011001111101111100010100011
9	1010	01000101110010100101110001100101 10111110011010001111100101100011 10011101101111010110100100011001 10101111111000100000110101000111
10	1010	00001011011001001101111011110100 10100100110001101111101110100010 10100101000001100010001111010101 10010000011110100011001001011111
11	1010	01100100010111101010010010000110 11010011101100111010111110100010 00100101010101100000000111000000 11011000011101110011010101111100
12	1010	00010001100010101111010000100100 10010110110110011011011111101101 00001011001001001111011011100101 10101110011000101111110100100001
13	1010	00110100101111001100100111111101 11000001010110001000011101010011 01000011110010011001110111111101 01000001000010001010010101000110
14	1010	00001011110001001001101011011110 00110100110111001111010111100100 01001110101011101000001010010001 00011010101011100000001011000001
15	1010	00111000101110110100101011001100 00111111100110000011111100011000 01101111001110100111101001110010 0111011101110101010101010000000000

Table 4-~~384-384-384-384-38~~. SLOS2 (128b/132b Encoding)

Symbol number	Sync Bits	SLOS2 Contents (127:0)
0	1010	10111111110101111110111011110101 01011011111110010111110001101110 01000101000101011101011110101110 11011101010010101111001111011000 1
1	1010	01101000110001101000010001101101 01000100111101010001101111010001 01101101011001001110000100010011 01010100001111110110011110100000 2
2	1010	11011011100010010100101001110011 10001000010010101101001111001100 01100000010000111101011001101110 00000101001111011100011010100100 3
3	1010	01111001010011000111000001001001 11010010001011001010110000111100 011001100100000000001011111110110 11111010010111011001101010000001 4
4	1010	11101111001101011000001110001110 01001001000100100101010010011111 00100011100010100100101110010011 01000100001101010110001111100010 5
5	1010	01110010100010001110101010010111 11100110111100000101100111011000 00101000111011101001010101100111 11100000111100111001100001000000 6
6	1010	11010111100011101100100101000010 01110110100010100110101110000111 01001100101100000011000111100001 00110011010000000011011111100010 7
7	1010	11110010110110001100100010000010 10101110111111010101111011111011 01011101001110101100010111000101 10100101100110011000000000001111 8
8	1010	1111100111111000011111001100111 00000000100111111010001111011010 01101001100001100000110000111000 01100100110000010000011101011100 9
9	1010	10111010001101011010001110011010 01000001100101110000011010011100 01100010010000101001011011100110 01010000000111011111001010111000 10
10	1010	11110100100110110010000100001011 01011011001110010000010001011101 01011010111110011101110000101010 01101111100001011100110110100000 11
11	1010	10011011101000010101101101111001 00101100010011000101000001011101 11011010101010011111111000111111 00100111100010001100101010000011 12
12	1010	11101110011101010000101111011011 01101001001001100100100000010010 11110100110110110000100100011010 01010001100111010000001011011110 13
13	1010	11001011010000110011011000000010 00111110101001110111100010101100 10111100001101100110001000000010 101111101111011101011010111001 14
14	1010	11110100001110110110010100100001 11001011001000110000101000011011 10110001010100010111110101101110 11100101010100011111110100111110 15
15	1010	11000111010001001011010100110011 11000000011001111100000011100111 10010000110001011000010110001101 10001000100010101010101111111111

4.2.1.3.4.2 TS1 and TS2 Ordered Sets

Unless specified otherwise, a transmitter shall not use a value in this section that is marked as “Reserved”. The target of an Ordered Set shall ignore an Ordered Set that has any of its defined fields set to a Reserved value and proceed as if the Ordered Set was never received. For Gen 2 and Gen 3 Links, a TS1 Ordered Set and a TS2 Ordered Set shall have the structure in Table 4-39.

Table 4-39. TS1 and TS2 Ordered Sets

Bits	Name	Description
63:59	<i>Reserved</i>	Reserved. Transmitter may send any value and receiver shall ignore. It is recommended that this field be zero.
58:56	<i>Lane Bonding Target</i>	Lane Bonding Target. Used to set the target Link width (see also Section 4.2.1.5). A transmitter shall set this field according to the value of the <i>Target Link Width</i> field of the Lane Adapter Configuration Capability 000b – Establish two Single-Lane Links 001b – Establish a Symmetric Link All other values are reserved and shall not be used.

Bits	Name	Description
55:48	<i>Lane Number</i>	Lane Number. Transmitter shall set this value to match the Lane number. 00h – Lane 0 01h – Lane 1 All other values are reserved and shall not be used.
47:32	<i>Reserved</i>	Reserved. Transmitter may send any value and receiver shall ignore. It is recommended that this field be zero.
31:29	<i>Reserved</i>	Reserved. Transmitter shall write 0 and receiver shall ignore.
28:26	<i>Lane Bonding Target 2</i>	Lane Bonding Target 2. Transmitter shall set this value to match the <i>Lane Bonding Target</i> field. Receiver shall ignore this field.
25:16	<i>Reserved</i>	Reserved. Transmitter may send any value and receiver shall ignore. It is recommended that this field be zero.
15:10	<i>TSID</i>	TSID. Training Sequence ID 10 0110b – TS1 01 1001b – TS2
9:0	<i>SCR</i>	SCR – Shall be set to 00 1111 0010b to indicate that Ordered Set contents are scrambled.

4.2.1.3.5 Gen 4 Training Sequences

Lane Initialization of a Gen 4 Link uses Gen 4-specific Training Sequences (Gen 4 TS). The basic structure of a Gen 4 TS (except for a Gen 4 TS2.clksw) is described in Figure 4-14 and Table 4-40. The Gen 4 TS2.clksw is described in Section 4.2.1.3.5.3. None of the Gen 4 Training Sequences are scrambled. The first bit/trit on the wire shall be the most significant bit/trit of the Gen 4 TS. PAM2 signaling uses Vdd and -Vdd voltages, which are encoded to 2t and 0t respectively. PAM3 signaling uses Vdd, 0 and -Vdd voltages, which are encoded to 2t, 1t and 0t respectively. Unless specified otherwise, a transmitter shall not use a value in this section that is marked as “Reserved”. The target of a Gen 4 Training Sequence shall ignore a Gen 4 Training Sequence that has any of its defined fields set to a Reserved value and proceed as if the Gen 4 Training Sequence was never received.

Figure 4-14. Gen 4 Training Sequence

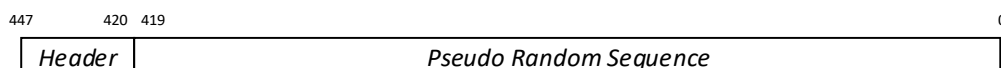


Table 4-40. Gen 4 Training Sequence

Trits	Name	Description
447:420	<i>Header</i>	Used to inform Re-timers/Router on the Link of the progress of the Lane Initialization.
419:0	<i>Pseudo Random Sequence</i>	TS1 – PRBS11 TS2, TS3, TS4 – PRTS7

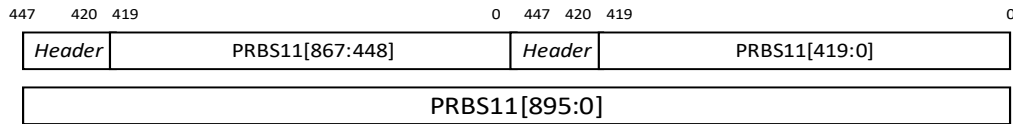
The *Header* of a Gen 4 Training Sequence shall use PAM2 signaling. The *Header* for each Training Sequence is described in the subsections below. The fields in the *Header* that are defined in hexadecimal base shall be converted to binary base and use PAM2 signaling.

Note: A receiver should ignore a Training Sequence with errors in its *Header*.

The *Pseudo Random Sequence* shall use PAM2 signaling for TS1. The *Pseudo Random Sequence* shall use PAM3 signaling for TS2, TS3, and TS4. The Pattern transmitted in the Training Sequences shall advance for each transmitted trit/bit. However, when transmitting bits 447:420 of the Training Sequence, the *Header* content is transmitted instead of the *Pseudo Random Sequence*. Therefore, the PRBS11 or PRTS7 are not transmitted in their entirety.

Figure 4-15 shows an example of two Gen 4 TS1 that are sent back-to-back, assuming that PRBS11[895:0] represents 896 consecutive bits of PRBS11, where bit 895 is the first bit of the PRBS11.

Figure 4-15. Example of Two Gen 4 TS1



4.2.1.3.5.1 Gen 4 TS1

The format for a Gen 4 TS1 is described in Table 4-41.

Table 4-41. Gen 4 TS1

Bits	Name	Description
447:436	<i>Cursor</i>	Cursor. 7E0h.
435:432	<i>Indication</i>	Indication. Used to notify the adjacent Router or Re-timer about the progress of the Lane Initialization: 1h – Receiver is not ready to receive PAM3 signaling. 2h – Receiver is ready to receive PAM3 signaling. All other values are reserved and shall not be used.
431:428	<i>Bitwise Complement of Indication</i>	Bitwise Complement of Indication. Used to detect errors in the <i>Indication</i> field.
427:420	<i>Counter</i>	Counter. A transmitter shall set these bits to 0Fh.
419:0	<i>PRBS11</i>	PRBS11. Shall use PAM2 signaling. Each transmitter shall load its seed as described in Table 4-66 upon transitioning to the Training.TS1 sub-state.

4.2.1.3.5.2 Gen 4 TS2

The format for a Gen 4 TS2 is described in Table 4-42.

Table 4-42. Gen 4 TS2

Trits	Name	Description
447:436	<i>Cursor</i>	Cursor. 7E0h.
435:432	<i>Indication</i>	Indication. Used to notify the adjacent Router or Re-timer about the progress of the Lane Initialization: 3h – PAM3 TxFFE is being executed. 4h – Receiver finished PAM3 TxFFE negotiation. All other values are reserved and shall not be used.
431:428	<i>Bitwise Complement of Indication</i>	Bitwise Complement of Indication. Used to detect errors in the <i>Indication</i> field.
427:420	<i>Counter</i>	Counter. A transmitter shall set these bits to 0Fh.
419:0	<i>PRTS7</i>	PRTS7. Shall use PAM3 signaling. Each transmitter shall load its seed as described in Table 4-66 upon transitioning to the Training.TS2 sub-state.

4.2.1.3.5.3 Gen 4 TS2.clksw

Gen 4 TS2.clksw are transmitted by a Re-timer when switching from the local clock to a recovered clock. A Gen 4 TS2.clksw does not contain a header and consists of the following repeating 28 trits sequence:

{1t, 2t, 0t, 2t, 2t, 1t, 0t, 2t, 2t, 0t, 1t, 2t, 0t, 0t, 2t, 1t, 0t, 2t, 0t, 0t, 1t, 2t, 0t, 0t, 2t, 1t, 0t, 2t}

The sequence is sent from MST to LST, first trit on the wire is 1t.

See Section 3.2.3.10 and the USB4 Re-Timer Specification for more information on when a Re-timer transmits this pattern.

4.2.1.3.5.4 Gen 4 TS3

The format for a Gen 4 TS3 is described in Table 4-43.

Table 4-43. Gen 4 TS3

Trits	Name	Description
447:436	<i>Cursor</i>	Cursor. 7E0h.
435:432	<i>Indication</i>	Indication. Used to notify the adjacent Router or Re-timer about the progress of the Lane Initialization: 5h – Indication to Re-timers to execute clock switch. 6h – Receiver detected Gen 4 TS3 Headers (clock switch done on all Re-timers). All other values are reserved and shall not be used.
431:428	<i>Bitwise Complement of Indication</i>	Bitwise Complement of Indication. Used to detect errors in the <i>Indication</i> field.
427:420	<i>Counter</i>	Counter. A transmitter shall set these bits to 0Fh.
419:0	<i>PRTS7</i>	PRTS7. Shall use PAM3 signaling.

4.2.1.3.5.5 Gen 4 TS4

The format for a Gen 4 TS4 is described in Table 4-44.

Table 4-44. Gen 4 TS4

Trits	Name	Description
447:436	<i>Cursor</i>	Cursor. 7E0h.
435:428	<i>Indication</i>	Indication. A Transmitter shall set these bits to F0h.
427:424	<i>Counter</i>	Counter. Initialization 0h – Transmitter shall set this field to 0h until tSSCActivated time after SSC was activated. 1h-Fh – Transmitter shall increment each Gen 4 TS4 from 1h to Fh to allow the Link Partner to de-skew the Lanes
423:420	<i>Bitwise Complement of Counter</i>	Bitwise Complement of Counter. Used to detect errors in the <i>Counter</i> field.
419:0	<i>PRTS7</i>	PRTS7. Shall use PAM3 signaling.

4.2.1.4 CL0

4.2.1.4.1 Entry to State

A Lane Adapter shall enter this state upon any of the following events:

- Successful completion of Lane training.
- Successful completion of Lane Bonding in Gen 2 and Gen 3 Links.
- Exit from CL0s state.

4.2.1.4.2 Behavior in State

When a Lane Adapter is in the CL0 state, the Transport Layer may utilize the USB4 Link for data transfer. The transmitter and receiver are on while in this state. For a Gen 4 Link, the first RS-FEC block sent by the USB4 Port upon transitioning to CL0 from Training or Low Power states is a De-skew Block, which is defined in Section 4.4.4.

4.2.1.4.3 Exit from State

A Lane Adapter shall exit this state after one of the following occurs:

- Adapter Disable. A Lane Adapter that exits this state due to an Adapter disable shall transition to either the Disabled state or the CLd state as defined in Section 4.4.6.
- Adapter disconnect. A Lane Adapter that exits this state due to a disconnect shall transition to the CLd state (see Section 4.4.5).
- Reception of an LT_Fall Transaction. The Lane Adapter shall transition to the CLd state.
- For a Gen 4 Link, transition to CLd state when the Gen 4 Link Recovery flow is executed.
- For a Gen 2 or Gen 3 Link, transition to Training state when either:
 - An error event occurs that transitions the Lane Adapter to the Training.LOCK1 sub-state. Section 4.4.2 describes potential error events and how they are handled.
 - Reception of any 2 SLOS Symbols in a row transitions the Lane Adapter to either the Training.LOCK1 sub-state or the Training.LOCK2 sub-state.
- Transition to CL0s, CL1, or CL2 states (see Section 4.2.1.6.1.2).
- For a Gen 2 or Gen 3 Link, transition to Lane Bonding state when either:
 - The *Lane Bonding* bit in the Lane Adapter Configuration Capability register of the Lane 0 Adapter in the USB4 Port is set to 1b.
 - 3 TS1 Ordered Sets are received in a row.

A Lane Adapter shall not exit this state to enter Lane Bonding state while it is sending a Transport Layer Packet. The Adapter shall complete sending the Packet before entering Lane Bonding state.

4.2.1.5 Lane Bonding

This state is not applicable in Gen 4 Links.

4.2.1.5.1 Entry to State

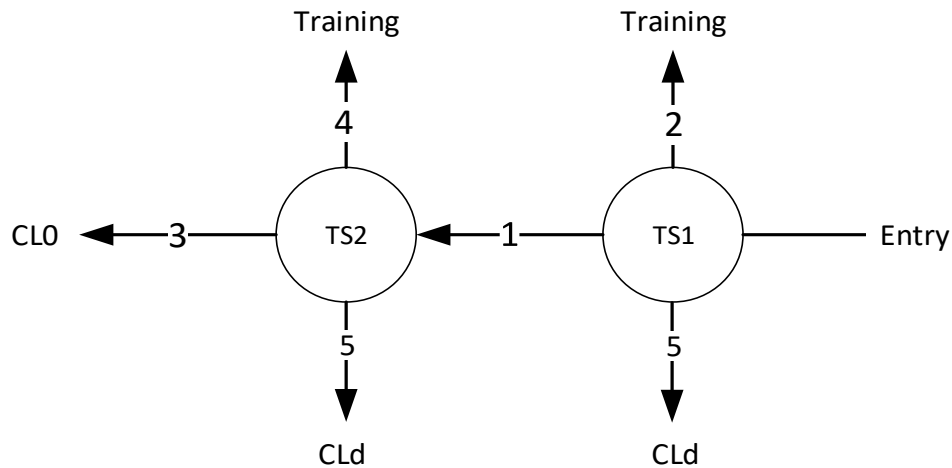
A Lane Adapter shall enter this state from CL0 state on any of the following events:

- The *Lane Bonding* bit in the Lane Adapter Configuration Capability register of the Lane 0 Adapter of the USB4 Port is set to 1b.
- Three TS1 Ordered Sets are received in a row.

4.2.1.5.2 Behavior in State

Lane Bonding is the state that bonds two Single-Lanes Links into a Symmetric Link. See Section 4.2.2.2 for details on transitioning from two Single-Lane Links to a Symmetric Link.

A Lane Adapter shall follow the Lane Bonding sub-state machine described in Figure 4-16 with the behavior described in Table 4-45 and the state transitions described in Table 4-46.

Figure 4-16. Lane Bonding Sub-State Machine**Table 4-45. Transmitter Behavior in Bonding Sub-States**

State	Transmitter Behavior
TS1	Transmitter shall send back-to-back TS1 Ordered Sets.
TS2	Transmitter shall send back-to-back TS2 Ordered Sets.

Table 4-46. Lane Bonding Sub-State Machine Transitions

Transition	From State	To State	Conditions ¹
1	TS1	TS2	Gen 2: <ul style="list-style-type: none"> Received 2 TS1 Ordered Sets in a row. Sent at least 32 TS1 Ordered Sets. Gen 3: <ul style="list-style-type: none"> Received 2 TS1 Ordered Sets in a row. Sent at least 16 TS1 Ordered Sets.
2	TS1	Training.LOCK2	<ul style="list-style-type: none"> Received 2 SLOS1 Symbols in a row. <i>Note: at Gen 3 speed, it is sufficient to match either the high 64 bits or the low 64 bits of a 128 bit Symbol when determining whether 2 SLOS1 Symbols are received in a row.</i>
3	TS2	CL0	Gen 2: <ul style="list-style-type: none"> Received 2 TS2 Ordered Sets in a row. Sent at least 16 TS2 Ordered Sets. Gen 3: <ul style="list-style-type: none"> Received 2 TS2 Ordered Sets in a row. Sent at least 8 TS2 Ordered Sets.
4	TS2	Training.LOCK2	<ul style="list-style-type: none"> Received 2 SLOS Symbols (SLOS1 and/or SLOS2) in a row.
5	TS1/TS2	CLd	<ul style="list-style-type: none"> Did not transition to CL0 state after tBonding time.
Notes: 1. All conditions need to be met before transition takes place.			

The transmitter and receiver are on while in this state.

4.2.1.5.3 Exit from State

A Lane Adapter shall exit this state as defined in Table 4-46.

A Lane Adapter that exits this state due to successful completion (i.e. Transition 3 in Table 4-46) transitions to the CL0 state. A Lane Adapter that transitions to CL0 state shall continue sending TS2 Ordered Sets until the other Lane Adapter in the USB4 Port enters CL0 state.

A Lane Adapter that exits this state due to receiving SLOS Symbols (i.e. Transitions 2 and 4 in Table 4-46) transitions to the Training.LOCK2 sub-state.

A Lane Adapter that exits this state due to bonding timeout (i.e. Transition 5 in Table 4-46) transitions to CLd state.

4.2.1.6 Low Power States (CL0s, CL1, and CL2)

The CL0s, CL1, and CL2 Low Power states are used to reduce transmitter and receiver power when a Lane is idle. Support for the CLx Low Power states is optional.

The behavior of the Lane Adapter when the Link is Gen 2 or Gen 3 speed is described in Sections 4.2.1.6.1, 4.2.1.6.5.1.1, 4.2.1.6.5.2, and 4.2.1.6.5.3. The behavior of the Lane Adapter when the Link is Gen 4 speed is described in Sections 4.2.1.6.2, 4.2.1.6.5.1.2, and 4.2.1.6.5.4.

4.2.1.6.1 Gen 2 and Gen 3 Low Power States

When a Lane Adapter supports CLx states, it shall enter or reject a CLx state as described in Section 4.2.1.6.1.2. When a Lane Adapter does not support CLx states, it shall reject entry to CLx state as described in Section 4.2.1.6.1.2.

4.2.1.6.1.1 Ordered Sets

The following Ordered Sets are used to enter and exit a Low Power state:

- CL2_REQ Ordered Set is used to request entry to CL2 state. See Table 4-47.
- CL1_REQ Ordered Set is used to request entry to CL1 state. See Table 4-48.
- CL2_ACK Ordered Set is used to approve entry to CL2 state. See Table 4-49.
- CL1_ACK Ordered Set is used to approve entry to CL1 state. See Table 4-50.
- CL0s_ACK Ordered Set is used to approve entry to CL0s state. See Table 4-51.
- CL_NACK Ordered Set is used to reject entry to a Low Power state. See Table 4-52.
- CL_OFF Ordered Set is used to complete entry to Low Power state. See Table 4-53.
- CL_WAKE1.X and CL_WAKE2.X Ordered Sets are used to exit a Low Power state. See Section 4.2.1.6.1.1

Table 4-47. CL2_REQ Ordered Set

Bits	Value	Description
63:10	11 1011 0000 0100 1011 1011 0000 0100 1011 1011 0000 0100 1011 1000b	Ordered Set contents.
9:0	00 1111 0010b	SCR – Shall be set to this value to indicate that the Ordered Set contents are scrambled.

Table 4-48. CL1_REQ Ordered Set

Bits	Value	Description
63:10	11 1011 0000 0100 0111 1011 0000 0100 0111 1011 0000 0100 0111 1011b	Ordered Set contents.
9:0	00 1111 0010b	SCR – Shall be set to this value to indicate that the Ordered Set contents are scrambled.

Table 4-49. CL2_ACK Ordered Set

Bits	Value	Description
63:10	10 1011 0000 0100 1010 1011 0000 0100 1010 1011 0000 0100 1011 1100b	Ordered Set contents.
9:0	00 1111 0010b	SCR – Shall be set to this value to indicate that the Ordered Set contents are scrambled.

Table 4-50. CL1_ACK Ordered Set

Bits	Value	Description
63:10	10 1011 0000 0100 0110 1011 0000 0100 0110 1011 0000 0100 0110 1011b	Ordered Set contents.
9:0	00 1111 0010b	SCR – Shall be set to this value to indicate that the Ordered Set contents are scrambled.

Table 4-51. CL0s_ACK Ordered Set

Bits	Value	Description
63:10	10 1011 0000 0100 0101 0110 1011 0000 0100 0101 0110 1011 0000 0100b	Ordered Set contents.
9:0	00 1111 0010b	SCR – Shall be set to this value to indicate that the Ordered Set contents are scrambled.

Table 4-52. CL_NACK Ordered Set

Bits	Value	Description
63:10	11 1111 0000 0100 0111 1111 0000 0100 0111 1111 0000 0100 0100 0100b	Ordered Set contents.
9:0	00 1111 0010b	SCR – Shall be set to this value to indicate that the Ordered Set contents are scrambled.

Table 4-53. CL_OFF Ordered Set

Bits	Value	Description
63:10	00 0011 1111 1100 0011 1111 1100 0011 1111 1100 0011 1111 1100 0100b	Ordered Set contents.
9:0	00 1111 0010b	SCR – Shall be set to this value to indicate that the Ordered Set contents are scrambled.

4.2.1.6.1.1.1 CL_WAKE1.X Ordered Sets

CL_WAKE1.X Ordered Sets are sent by Re-timers.

When operating in Gen 2 mode with RS-FEC encoding disabled, a CL_WAKE1.X Ordered Set Symbol has the structure of an SLOS1 Symbol with 64b/66b encoding and the following modifications:

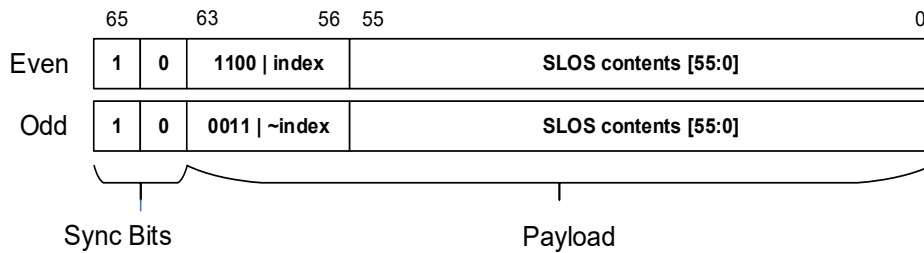
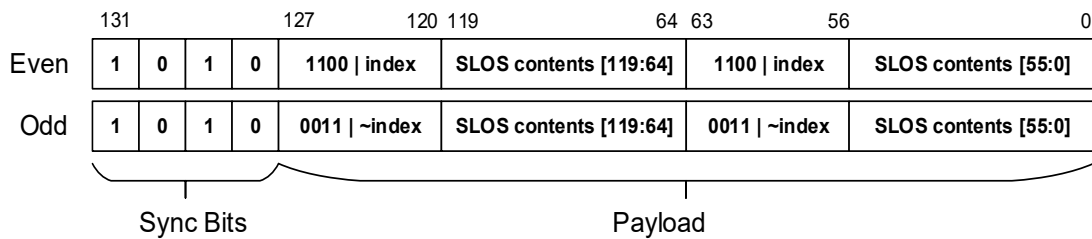
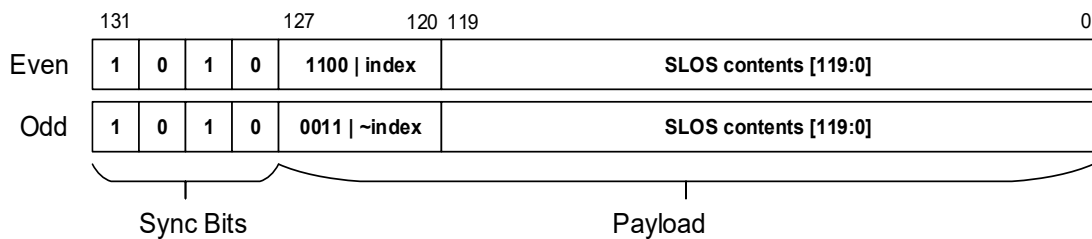
- Bits [63:56] of an even numbered Symbol payload are CXh, where “X” is the hexadecimal Re-timer Index of the Re-timer that generated the Ordered Set.
- Bits [63:56] of an odd numbered Symbol payload are the logical inverse of CXh, where “X” is the hexadecimal Re-timer Index of the Re-timer that generated the Ordered Set.

When operating in Gen 2 mode with RS-FEC encoding enabled, a CL_WAKE1.X Ordered Set Symbol has the structure of an SLOS1 Symbol with 128b/132b Encoding and the following modifications (see Figure 4-17):

- Bits [127:120] of an even numbered Symbol payload are CXh, where “X” is the hexadecimal Re-timer Index of the Re-timer that generated the Ordered Set.
- Bits [63:56] of an even numbered Symbol payload are CXh, where “X” is the hexadecimal Re-timer Index of the Re-timer that generated the Ordered Set.
- Bits [127:120] of an odd numbered Symbol payload are the logical inverse of CXh, where “X” is the hexadecimal Re-timer Index of the Re-timer that generated the Ordered Set.
- Bits [63:56] of an odd numbered Symbol payload are the logical inverse of CXh, where “X” is the hexadecimal Re-timer Index of the Re-timer that generated the Ordered Set.

When operating in Gen 3 mode, a CL_WAKE1.X Ordered Set Symbol has the structure of an SLOS1 Symbol with 128b/132b Encoding and the following modifications (see Figure 4-17):

- Bits [127:120] of an even numbered Symbol payload are CXh, where “X” is the hexadecimal Re-timer Index of the Re-timer that generated the Ordered Set.
- Bits [127:120] of an odd numbered Symbol payload are the logical inverse of CXh, where “X” is the hexadecimal Re-timer Index of the Re-timer that generated the Ordered Set.

Figure 4-17. Structure of a CL_WAKE1.X Ordered Set Symbol**(a) CL_WAKE1.X Ordered Set Symbol in Gen 2 mode and RS-FEC disabled****(b) CL_WAKE1.X Ordered Set Symbol in Gen 2 mode and RS-FEC enabled****(c) CL_WAKE1.X Ordered Set Symbol in Gen 3 mode**

A CL_WAKE1.X Ordered Set shall not be scrambled, and the scrambler shall not advance upon receive/transmit. Unless otherwise mentioned, a CL_WAKE1.X Ordered Set shall be transmitted in its entirety.

4.2.1.6.1.1.2 CL_WAKE2.X Ordered Sets

A CL_WAKE2.X Ordered Sets are sent by Routers.

When operating in Gen 2 mode with RS-FEC encoding disabled, a CL_WAKE2.X Ordered Set Symbol has the structure of an SLOS2 Symbol with 64/66b encoding and the following modifications:

- Bits [63:56] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
- Bits [63:56] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.

When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set Symbol has the structure of an SLOS2 Symbol with 128b/132b encoding and the following modifications:

- Bits [127:120] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.

- Bits [63:56] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
- Bits [127:120] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
- Bits [63:56] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.

When operating in Gen 3 mode, a CL_WAKE2.X Ordered Set Symbol has the structure of an SLOS2 Symbol with 128b/132b Encoding and the following modifications:

- Bits [127:120] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
- Bits [127:120] of an odd numbered Symbol payload shall be the logical inverse of CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.

A CL_WAKE2.X Ordered Set shall not be scrambled, and the scrambler shall not advance upon receive/transmit. Unless otherwise mentioned, a CL_WAKE2.X Ordered Set shall be transmitted in its entirety.

4.2.1.6.1.2 Entry to State

The Lane Adapters in a USB4 Port either enter or reject entry to a CLx state as described in this section. The Lane Adapters in a Downstream Facing Port of a Hub Router shall not initiate entry to CL2.

A USB4 Port uses a set of objections to prevent its Adapters from entering into a Low Power state. When a USB4 Port asserts an objection, its Lane Adapters cannot enter a Low Power state. When a USB4 Port does not assert an objection, its Lane Adapters may optionally enter a Low Power state. Objections are defined in Section 4.2.1.6.3.

For a Single Lane Link, only the Lane 0 Adapter executes the flow in this section. For a Symmetric Link, both the Lane 0 Adapter and the Lane 1 Adapter execute the flow. The USB4 Port that initiates the transition to a CLx state is referred to as the “Requesting Port.” The USB4 Port on the other side of the Link is referred to as the “Responding Port.”

- In the Requesting Port, an Adapter requests entry to a Low Power state by sending a request Ordered Set as follows. The request Ordered Set shall be sent back-to-back until a response Ordered Set is received from the Link Partner.
 - A Lane Adapter uses the CL2_REQ Ordered Set to request entry to the CL2 state. An Adapter shall send CL2_REQ Ordered Sets when its USB4 Port does not assert any objections to enter CL2 state.
 - A Lane Adapter uses the CL1_REQ Ordered Set to request entry to the CL1 state. An Adapter shall send CL1_REQ Ordered Sets when its USB4 Port asserts an objection to enter CL2 state but does not assert any objections to enter CL1 state.
 - If a Lane Adapter receives a CL1_REQ Ordered Set or a CL2_REQ Ordered Set from its Link Partner, it shall not request entry to a Low Power state until after transitioning back to CL0.
 - If the Requesting Port asserts an objection after the Lane Adapter has sent a request Ordered Set, the Lane Adapter shall ignore the objection until the Lane Adapter is either in a CLx state or receives a CL_NACK Ordered Set.

Note: If the Requesting Port receives a Transport Layer Packet during this time and flow control for the Packet is enabled, the Transport Layer Packet is queued and causes the Port to assert an objection. The Lane Adapters in the Port will process the objection after receiving a CL_NACK or transitioning to the CLx state. The Packet will be transmitted when the Lane Adapters are in CL0 state.

- In the Responding Port, a Lane Adapter responds to a request to enter a Low Power state by sending back-to-back response Ordered Sets as follows:
 - A Lane Adapter shall reject a request to enter a Low Power state when all the following are true:
 - The Adapter has already sent a request to enter the same Low Power state.
 - The *PM Secondary* bit in the Lane 0 Adapter of the Responding Port is set to 0b.

The Lane Adapter shall send CL_NACK Ordered Sets for as long as it receives the request Ordered Set from the Link Partner. After the Adapter stops receiving request Ordered Sets, it may send request Ordered Sets.

- A Lane Adapter that receives a CL1_REQ Ordered Set after it has sent a CL2_REQ Ordered Set, shall accept the request by responding with CL1_ACK Ordered Sets. The Adapter shall stop sending CL2_REQ Ordered Sets.
- A Lane Adapter that receives a CL2_REQ Ordered Set after it has sent a CL1_REQ Ordered Set, shall not respond to the request and shall continue sending CL1_REQ Ordered Sets.
- Else, if the Responding Port does not assert an objection to enter CL2 state, it shall respond to CL2_REQ Ordered Sets with a CL2_ACK Ordered Set. The first CL2_ACK shall be sent within tCLxRequest after receiving the request. The CL2_ACK Ordered Set shall be sent 375 times. After the last CL2_ACK, the Responding Port shall shut down its transmitter within tTxOff time. The Adapter may send additional CL2_ACK Ordered Sets during the tTxOff period.
 - If RS-FEC is enabled, the transmitter may shut down before the current RS_FEC block ends.
- Else, if the Responding Port does not assert an objection to enter CL1 state, it shall respond to CL2_REQ or CL1_REQ Ordered Sets with a CL1_ACK Ordered Set. The first CL1_ACK shall be sent within tCLxRequest after receiving the request. The CL1_ACK Ordered Set shall be sent 375 times. After the last CL1_ACK, the Responding Port shall shut down its transmitter within tTxOff time. The Adapter may send additional CL1_ACK Ordered Sets during the tTxOff period.
 - If RS-FEC is enabled, the transmitter may shut down before the current RS_FEC block ends.
- Else, if the *CL0s Enable* bit is set to 1b in the Lane 0 Adapter of the Responding Port, and the Responding Port can meet the timing of both tCL0sEntry (Equation 4-1) and tCL0sExit (Equation 4-3 or Equation 4-4), a Lane Adapter shall respond to a request to enter a Low Power state with a CL0s_ACK Ordered Set. The first CL0s_ACK shall be sent within tCLxRequest after receiving the request. The CL0s_ACK Ordered Set shall be sent 16 times.

Note: Unless otherwise noted, the Connection Manager can change the value of the CL0s Enable bit at any time.

- Else, a Lane Adapter shall respond to a request to enter a Low Power state with CL_NACK Ordered Sets within a time that is less than (tCL0sEntry + tCL0sExit). The CL_NACK Ordered Sets shall be sent 16 times. The Adapter shall resume regular CL0 operation in the transmit direction once it stops sending the CL_NACK Ordered Sets.
- After sending a CL_NACK Ordered Set, a port shall be able to meet tCL0sEntry and tCL0sExit requirements within tCLxSetup time, and shall continue to meet these timing requirements for a duration of tCLxAccept.
- If the Responding Port asserts an objection after the Lane Adapter has sent a CLx_ACK response Ordered Set, but before the transition to CLx state is complete,

the Lane Adapter shall ignore the objection until it transitions to the CLx state. After transitioning to CLx state, the objection will cause the Adapter to exit the CLx state as defined in Section 4.2.1.6.5.



IMPLEMENTATION NOTE

There could be rare circumstances at which the Responding Port cannot guarantee CL0s resumption to CL0 within the expected time. In such cases the port may reject CLx entry request to avoid any timing sensitive application failure (such as PCI e LTR). Since subsequent attempts to enter CLx may be initiated by the remote port, the value of tCLxSetup is defined to limit the duration at which the Responding Port may reject such requests, thus ensuring CL0s entry is not being deferred indefinitely.

- In the Requesting Port, a Lane Adapter shall stop sending a request to enter a Low Power state when it receives a response Ordered Set from the Link Partner.
 - If the response is a CL2_ACK, a CL1_ACK, or a CL0s_ACK Ordered Set, the Lane Adapter shall send 375 CL_OFF Ordered Sets. The CL_OFF Ordered sets shall be sent back-to-back. The first CL_OFF Ordered Set shall be sent within tCLxResponse after detection of the response. If the response is a CL2_ACK or a CL1_ACK Ordered Set, the Adapter shall also shut down its receiver.
 - If the response is a CL_NACK Ordered Set, the Adapter shall not send another CL2_REQ Ordered Set or CL1_REQ Ordered Set for tCLxRetry after receiving the CL_NACK Ordered Set.
 - If the response is a CL_NACK Ordered Set, all Lane Adapters in the Requesting Port shall resume regular CL0 operation.
- If the Requesting Port detects Link errors in the direction of the Link Partner before receiving a response Ordered Set from the Link Partner, it shall:
 - Stop sending the request to enter a Low Power state.
 - Transition its Lane Adapters to the Training.LOCK1 sub-state and send the first SLOS within tCLxResponse of detecting the Link error.
- In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets:
 1. Shut down its transmitter within tTxOff time. The Adapter may send additional CL_OFF Ordered Sets during the tTxOff period.
 - If RS-FEC is enabled, the transmitter may shut down before the current RS_FEC block ends.
 2. Transition state as follows:
 - If the response from the Link Partner was CL2_ACK, transition to CL2 state.
 - If the response from the Link Partner was CL1_ACK, transition to CL1 state.
 - If the response from the Link Partner was CL0s_ACK, transition to CL0s state.
 3. Enable exit from CLx state as follows:
 - If the response from the Link Partner was CL2_ACK or CL1_ACK, wait tEnterLFPS1 time after the state transition in Step 2), then enable transmission and detection of Low Frequency Periodic Signaling (LFPS) (see Section 4.2.1.6.4).

- If the response from the Link Partner was CL0s_ACK, wait $t_{EnterLFPS4}$ time after the state transition in Step 2), then enable transmission of Low Frequency Periodic Signaling (LFPS).
- In the Responding Port, a Lane Adapter shall shut down its receiver after receiving a CL_OFF Ordered Set. If the Adapter sent CL0s_ACK Ordered Sets, it shall also transition to the CL0s state. The Adapter shall then enable exit from the Low Power state as follows:
 - If the Adapter sent CL2_ACK or CL1_ACK, wait $t_{EnterLFPS2}$ time after shutting down the receiver, then enable transmission and detection of Low Frequency Periodic Signaling (LFPS).
 - If the Adapter sent CL0s_ACK, wait $t_{EnterLFPS5}$, then enable detection of Low Frequency Periodic Signaling (LFPS).

A Lane Adapter may transition to Training.LOCK1 sub-state as a result of Logical Layer errors during the entry to Low Power state with the following exceptions:

- After sending the first CL2_ACK, CL1_ACK, or CL0s_ACK Ordered Set, a Lane Adapter shall not enter Training state as a result of Logical Layer errors in its receivers. It is recommended that the Adapter turn off RS-FEC immediately when it detects Logical Layer errors in order to detect SLOS.
- A Lane Adapter that is sending CL_OFF Ordered Sets shall complete the transition to CL2, CL1, or CL0s state. The Adapter may then initiate an exit from the Low Power state to the Training state.

If a Lane Adapter receives SLOS at any time during the entry flow, it shall abort the entry flow and transition to either the Training.LOCK1 sub-state or the Training.LOCK2 sub-state as defined in Section 4.2.1.4.3.

Entry time to a CLx state is calculated by the following equations:

Equation 4-1. Entry Time to CL0s State

$$t_{CL0sEntry} \cong t_{CLxRequest} + t_{CLxResponse} + 375 \text{ Symbol Time} + t_{TxOff} + t_{EnterLFPS4}$$

Equation 4-2. Entry Time to CL1/ CL2 State

$$t_{CLxEntry} \cong t_{CLxRequest} + t_{CLxResponse} + t_{EnterLFPS2}$$

Note: If there are Re-timers on the Link, the Re-timer latency can add up to 2 μ s to the calculated CLx entry time.

See Appendix C.1 for examples of CL2, CL1, and CL0s entry.

**CONNECTION MANAGER NOTE**

A Connection Manager shall not do any of the following for a Gen 2 or Gen 3 Link:

- *Set the CL0s Enable, CL1 Enable, and/or CL2 Enable bit to 1b when USB4 Port has two Single-Lane Links that are not yet bonded.*
- *Set the CL0s Enable, CL1 Enable, and/or CL2 Enable bits to 1b when an Active Cable that does not support Low Power states is used.*
- *Set the CL0s Enable bit to 0b while the CL1 Enable bit is 1b.*
- *Set the CL1 Enable bit to 0b while the CL2 Enable bit is 1b.*
- *Set different values for the CL0s Enable bits at the two ends of a Link.*
- *Set different values for the CL1 Enable bits at the two ends of a Link.*
- *Set different values for the CL2 Enable bits at the two ends of a Link.*
- *Set either the CL0s Enable, CL1 Enable, or CL2 Enable bit to 1b in a USB4 Port operating with Bi-Directional Time Sync Handshakes.*
- *Set either the CL0s Enable, CL1 Enable, or CL2 Enable bit to 1b in a USB4 Port that is part of an Inter-Domain Link.*

A Connection Manager may set the CL0s Enable, CL1 Enable, and CL2 Enable bits to 1b for a Lane 0 Adapter when the Lane 1 Adapter is in the Disabled state or CLd state.

A Connection Manager shall not do any of the following for a Gen 4 Link:

- ~~*Set the CL0s Enable bit to 0b while the CL1 Enable bit is 1b.*~~
- ~~*Set the CL0s Enable bit to 0b while the CL2 Enable bit is 1b.*~~
- *Set the CL1 Enable bit or CL2 Enable bit to 1b on one side of the Link while the CL0s Enable bit is 0b on the other side of the Link.*
- *Set the CL1 Enable bit to 1b on one side of the Link while, on the other side of the Link, the CL2 Enable bit is 1b and the CL1 Enable bit is 0b.*
- *Set either the CL0s Enable, CL1 Enable, or CL2 Enable bit to 1b in a USB4 Port that is part of an Inter-Domain Link.*



CONNECTION MANAGER NOTE

For a Gen 2 or Gen 3 Links, a Connection Manager shall set the PM Secondary bit to 1b in a Lane Adapter that is part of the Upstream Facing Port. For a Downstream Facing Port, the Connection Manager shall set the PM Secondary bit as follows:

- *If the Downstream Facing Port connects to an Upstream Facing Port, set the PM Secondary bit to 0b in at least one of the Adapters in the Downstream Facing Port.*
- *If the Downstream Facing Port connects to another Downstream Facing Port:*
 - *In one Downstream Facing Port, set the PM Secondary bit to 0b in at least one Lane Adapter.*
 - *In the other Downstream Facing Port, keep the PM Secondary bit to 1b in both Lane Adapters.*

4.2.1.6.2 Gen 4 Low Power States

When a Lane Adapter supports CL1 or CL2 states, it shall initiate entry to a CLx state as described in Section 4.2.1.6.2.2. When a Lane Adapter supports CL0s state, it shall behave as a Receiver Port when its Link Partner initiates entry to a CLx state.

4.2.1.6.2.1 Ordered Sets

The following Ordered Sets are used to enter and exit a Low Power state:

- CL_OFF is used to enter Low Power state (see Section 4.3.2.6.1).
- CL0s_EXIT is used to exit CL0s Low Power state (see Section 4.3.2.6.2).

4.2.1.6.2.2 Entry to State

For a Gen 4 Link, the Lane Adapters in a USB4 Port enter a CLx state as described in this section.

A USB4 Port uses a set of objections to prevent its Adapters from entering into a Low Power state. When a USB4 Port asserts an objection, its Lane Adapters shall not initiate an entry to a Low Power state. When a USB4 Port is performing the CL0s (RX) exit flow, its Lane Adapters shall not initiate entry to a Low Power state. When a USB4 Port does not assert an objection, its Lane Adapters may optionally initiate an entry to a Low Power state. Objections are defined in Section 4.2.1.6.3.

A Downstream Facing Port of a Hub Router shall not initiate entry to CL0s (TX) with option to enter CL2 unless it is in CL0s (RX) with option to enter CL2.

All active transmitters shall execute the entry flow described below. The USB4 Port that initiates the transition to a CLx state is referred to as the “Initiating Port.” The USB4 Port connected to the Initiating Port is referred to as the “Receiver Port”.

- If the Initiating Port decides to enter CL0s with option to enter CL1 or CL2, it shall do the following:
 - On each active transmitter, send 126 CL_OFF Ordered Sets with the *Index* field set to 0t. The *CLx State* field shall be set to 2t if the Port has no objection to entering CL2. Otherwise, it shall be set to 1t. The Ordered Sets shall be sent without Redundancy Symbols. Each transmitter may replace any of the last 102 CL_OFF Ordered Sets with any valid Data Set.
 - If there are Re-timers on the Link, the Initiating Port shall send on each active transmitter 126 CL_OFF for each Re-timer on the Link with the same *CLx State* value as the first CL_OFF Ordered Sets. The *Index* field shall increment from 1 to the number of Re-timers on the Link for each 126 Ordered Sets on each

transmitter. For example, if there are 2 Re-timers on the Link, the *Index* field will be set to 1t in the first additional 126 Ordered Sets on each active transmitter and 2t in the second additional 126 Ordered Sets. The Ordered Sets shall be sent without Redundancy Symbols. Each transmitter may replace any of the last 102 CL_OFF Ordered Sets (for each Re-timer) with any valid Data Set.

Note: The option to replace the CL_OFF Ordered Sets with Data Sets allows the transmitter to use the same data path, which includes RS-FEC encoding, on the Low Power state entry flow. The receiver does not need to process any of the Data Symbols inserted by the transmitter as a substitute for the CL_OFF Ordered Sets.

- After sending the required sequence on the Lane 0 transmitter, the Initiating Port shall shut down all enabled transmitters while meeting the tTxOff period defined in Table 4-73. The Adapters may send any valid symbols during the tTxOff period.

Note: Due to Lane-to-Lane skew, it is possible that Rx1 and/or Rx2 will not receive the entire 126 CL_OFF Ordered Sets before their adjacent transmitters shut down.

- The Initiating Port shall enable LFPS transmission tEnterLFPS1 time after shutting down the Lane 0 transmitter.
- If the Initiating Port is already in CL0s (RX) state:
 - If the Initiating Port sent CL_OFF Ordered Sets with the *CLx State* field set to 2t and when it entered CL0s (RX) state it received CL_OFF Ordered Sets with the *CLx State* field set to 2t, it shall transition to CL2 state.
 - Otherwise it shall transition to CL1 state.
- Else, it shall transition to CL0s (TX) state.

When the Receiver Port detects CL_OFF Ordered Sets with the *Index* field set to 0t on Lane 0, it shall:

- De-activate RS-FEC decoding. The detection of CL_OFF shall not require RS-FEC decoding.
- Shut down all of its enabled receivers.
- Enable LFPS detection tEnterLFPS2 time after receiving the first CL_OFF Ordered set on the Lane 0 receiver.
- If the Receiver Port is already in CL0s (TX) state:
 - If the Initiating Port sent CL_OFF Ordered Sets with the *CLx State* field set to 2t and when the Receiver Port entered CL0s (TX) state it transmitted CL_OFF Ordered Sets with the *CLx State* field set to 2t, it shall transition to CL2 state.
 - Otherwise it shall transition to CL1 state.
- Else, it shall transition to CL0s (RX) state.

Entry time to a CLx state is tEnterLFPS3.

Note: The maximal entry time to a CLx state can be up to the maximal value of tEnterLFPS3.

4.2.1.6.3 Objections

A USB4 Port shall assert an objection to enter CL2 state if:

- The *CL2 Support* bit in the Lane 0 Adapter is 0b.
- The *CL2 Enable* bit in the Lane 0 Adapter is 0b.

Note: Unless otherwise noted, the Connection Manager can change the value of the CL2 Enable bit at any time.

- There is a Transport Layer Packet to be sent over the USB4 Port.

Note: Link-level flow control credits do not need to be available in order to assert this objection.

- The Link is operating at Gen 4 speed, and the Port's receiver receives Gen 4 Training Sequence.
- The Link is operating at Gen 4 speed, and the Port's receiver in the process of CL0s (Rx) Exit flow (See 4.2.1.6.5.1.2)
- If the Link is Gen 4 speed and less than tTimeInCL0 time has passed since the Lane 0 Adapter transitioned from CLx to CL0.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a PCIe Adapter's Routing Table and the PCIe Adapter is not in PCIe L1 state.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of the Upstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message transmitted upstream is smaller than the sum of the CL2 entry and exit latency.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Downstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message received by the Downstream PCIe Adapter is smaller than the sum of the CL2 entry and exit latency.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a DP IN Adapter's Routing Table.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a DP OUT Adapter's Routing Table and a Packet is issued from the DP OUT Adapter.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Gen X Adapter's Routing Table and the Internal USB3 Component is not in U2 or U3 state.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Gen X Adapter's Routing Table, the Internal USB3 Component is in U2 state, and CL2 entry is disabled in U2 state.

Note: Whether or not to enable CL2 entry when the Internal USB3 Component is in U2 state is a device-specific decision. The method for managing CL2 entry in U2 state is outside the scope of this specification.

- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Gen X Adapter's Routing Table, the Internal USB3 Component is in U3 state, and CL2 entry is disabled in U3 state.

Note: Whether or not to enable CL2 entry when the Internal USB3 Component is in U3 state is a device-specific decision. The method for managing CL2 entry in U3 state is outside the scope of this specification.

- ~~All~~Any of the USB3 Gen T Ports that are mapped to Paths that goes through the Lane 0 Adapter are not in Disabled, U2 or U3 state.
- ~~One~~Any of the USB3 Gen T Ports that are mapped to Paths that goes through the Lane 0 Adapter is in U2 state, and the *U2CL2 Enable* bit in USB3 Gen T Adapter Configuration Space is set to 0b.

- When not using Enhanced Uni-Directional mode, entry to CL2 state would delay a pending Time Sync handshake. This objection shall be asserted until the Time Sync handshake is complete.
- When using Enhanced Uni-Directional Time Sync handshake:
 - While using Inversed Bi-Directional mode.
 - The Downstream Facing Port sent a Delay Response and the Follow-Up Packet has not yet been sent.
 - The Downstream Facing Port missed more than *Replenish Threshold* Time Sync handshakes, the Lane Adapter is not in CL2, CL1, or CL0s (Tx) state, and the TMU has not yet completed *ReplenishN* consecutive handshakes.
 - The Downstream Facing Port is using Adaptive Uni-Directional mode and its Link Partner is not converged.

Note: The Link Partner is required to converge within $t_{Converge}$ time after the TMU is enabled or resumed after exiting CL2 and within $t_{CLxConverge}$ time after exiting CL1 or CL0s (TX). See Section 7.5 for more details.

- Host Routers only:
 - The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Host Interface Adapter's Routing Table, whose Path corresponds to a Transmit Descriptor Ring that disables CL2 entry.
 - The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Host Interface Adapter's Routing Table and the Host Interface has a Packet to send over the Adapter.

Note: End-to-end flow control credits are not required to be available in order to assert this objection.

- Device Routers only:
 - One of its Ports is in the process of CL0s, CL1 or CL2 exit flow.
- Hub Routers only:
 - If a Downstream Facing Port with CLx enabled is not in CL2, the Upstream Facing Port shall object CL2.
 - The *PM Packet Support* bit is set to 1b for one of the Paths that traverses the Lane Adapter and the last packet transmitted on the Path was not a PM Packet for CL2. For the purpose of this objection, Credit Sync Packets are ignored and do not affect the decision whether or not to assert this objection.

A USB4 Port shall assert an objection to enter CL1 state if:

- The *CL1 Support* bit in the Lane 0 Adapter is 0b.
- The *CL1 Enable* bit in the Lane 0 Adapter is 0b.

Note: Unless otherwise noted, the Connection Manager can change the value of the CL1 Enable bit at any time.

- There is a Transport Layer Packet to be sent over the USB4 Port.

Note: Link-level flow control credits do not need to be available in order to assert this objection.

- If the Link is Gen 4 speed and less than $t_{TimeInCL0}$ time has passed since the Lane 0 Adapter transitioned from CLx to CL0.

- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a PCIe Adapter's Routing Table and the PCIe Adapter is not in PCIe L1 state.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of the Upstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message transmitted upstream is smaller than the sum of the CL1 entry and exit latency.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Downstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message received by the Downstream PCIe Adapter is smaller than the sum of the CL1 entry and exit latency.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a DP IN Adapter's Routing Table and entry to CL1 state would delay traffic from the DP IN Adapter.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a DP OUT Adapter's Routing Table and a Packet is issued from the DP OUT Adapter.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Gen X Adapter's Routing Table and the Internal USB3 Component is not in U2 or U3 state.
- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Gen X Adapter's Routing Table, the Internal USB3 Component is in U2 state, and CL1 entry is disabled in U2 state.

Note: Whether or not to enable CL1 entry when the Internal USB3 Component in U2 state is a device-specific decision. The method of managing CL1 entry in U2 state is outside the scope of this specification.

- The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Gen X Adapter's Routing Table, the Internal USB3 Component is in U3 state, and CL1 entry is disabled in USB U3 state.

Note: Whether or not to enable CL1 entry when the Internal USB3 Component in U3 state is a device-specific decision. The method of managing CL1 entry in U3 state is outside the scope of this specification.

- ~~Any~~Any of the USB3 Gen T Ports that are mapped to Paths that goes through the Lane 0 Adapter are not in Disabled, U2 or U3 state.
- When not using Enhanced Uni-Directional Time Sync handshake, entry to CL1 state would delay a pending Time Sync handshake. The objection shall be asserted until the Time Sync handshake is complete.
- When using Enhanced Uni-Directional Time Sync handshake:
 - While using Inversed Bi-Directional mode.
 - The Downstream Facing Port sent a Delay Response and the Follow-Up Packet has not yet been sent.
 - The Downstream Facing Port missed *Replenish Timeout* number of Time Sync handshakes and has not yet completed a Time Sync handshake.
 - The Downstream Facing Port missed more than *Replenish Threshold* Time Sync handshakes, the Lane Adapter is not in CL2, CL1, or CL0s (Tx) state, and the TMU has not yet completed *ReplenishN* consecutive handshakes.
 - A Downstream Facing Port is using Adaptive Uni-Directional mode and its Link Partner is not converged.

Note: The Link Partner is required to converge within $t_{Converge}$ time after TMU is enabled or resumed after exiting CL2 and within $t_{CLxConverge}$ time after exiting CL1 or CL0s (TX). See Section 7.5 for more details.

- Host Routers only:
 - The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Host Interface Adapter's Routing Table, whose Path corresponds to a Transmit Descriptor Ring that disables CL1 entry.
 - The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Host Interface Adapter's Routing Table and the Host Interface has a Packet to send over the Adapter.

Note: End-to-end flow control credits are not required to be available in order to assert this objection.

- Device Routers only:
 - One of its Ports is in the process of CL0s, CL1 or CL2 exit flow.
- Hub Routers only:
 - If the Upstream Facing Port is not in CL1 or CL0s (RX), the Downstream Facing Ports shall object to entering CL1.
 - If a Downstream Facing Port with CL1 enabled is not in CL1, CL2 or CL0s (RX), the Upstream Facing Port shall object CL1.
 - The *PM Packet Support* bit is set to 1b for one of the Paths that traverses the Lane Adapter and the last packet transmitted on the Path was not a PM Packet for CL2 or CL1. For the purpose of this objection, Credit Sync Packets are ignored and do not affect the decision whether or not to assert this objection.

A Lane Adapter may also assert implementation-specific objections to CL1 and/or CL2 entry.

4.2.1.6.4 Behavior in State

While in CL2 state, the transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.

While in CL1 state, the transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.

While in CL0s state, the transmitter at the requesting USB4 Port shall be in electrical idle. Lane common mode voltages shall be maintained.

Receiver termination shall be maintained in CL0s CL1, and CL2 states.

4.2.1.6.5 Exit from State

A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when:

- An objection is set in the USB4 Port that would have prevented the Adapter from entering the Low Power state.
- The Adapter is in CL0s state and a CL2_REQ Ordered Set or a CL1_REQ Ordered Set is received from the Link Partner.
- The Adapter is in CL0s state and it detects Link errors that cause the Adapter to transition to Training state.
- The Adapter is in a CL1 state or a CL2 state and it is referenced in an *Egress Adapter* field of a Lane Adapter's Routing Table and the other Adapter's receiver is exiting from CL0s, CL1, or CL2 states.
- The Adapter is in CL0s state and it is referenced in an *Egress Adapter* field of a Lane Adapter's Routing Table and the other Adapter's receiver is exiting from CL0s, CL1, or CL2 states.

A Lane Adapter may also exit from CL0s, CL1, or CL2 states by means which are implementation specific.

While in CL2 or CL1 state, the USB4 Ports at either end of the Lane may initiate exit from the state. While in CL0s state, only the USB4 Port whose transmitter is in electrical idle may initiate exit from the state.

See Appendix C for examples of end-to-end flows describing the behavior of Adapters and Re-timers during CL2, CL1, or CL0s exit.

4.2.1.6.5.1.1 Gen 2 and Gen 3 Exit flow from CL0s state

The USB4 Port initiating exit from CL0s state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on all Lanes for the duration of at least 16 LFPS cycles (see Section 3.4) and for no more than tLFPSDuration.
2. Return to Electrical Idle for tPreData (see Table 3-33).
3. Start transmitting SLOS1 on each Lane of the USB4 Port. Any received CL_WAKE Ordered Sets shall be ignored.
 - A USB4 Port may exit CL0s state with SSC enabled or disabled.
4. On detection of 2 back-to-back TS2 Ordered Sets, continue sending SLOS1 for tTXSLOS time, then stop sending SLOS1 and send at least 16 TS2 Ordered Sets. The first TS2 Ordered Set shall be sent within tTrainingTransition after detection of the second TS2 Ordered Set. Before transmitting the first TS2 Ordered Set:
 - The scrambler shall load a new seed as defined in Section 4.3.1.5.
 - Activate RS-FEC as defined in Section 4.3.1.6.1.
 - Enable SSC if SSC is disabled.

Note: If the Adapter is in Training state (due to receiving Link errors while in CL0s state), then the Adapter proceeds with the Training state-machine rather than sending the TS2 Ordered Sets.

If the receiver did not detect 2 back-to-back TS2 Ordered Sets within tTrainingAbort2 time after the transmitter started sending SLOS1 it shall initiate a Disconnect by driving SBTx to a logical low state for tDisconnectTx.

5. Transition to CL0 state:
 - If the USB4 Port operated with a Symmetric Link prior to entry to CL0s state, the USB4 Port shall resume operation with a Symmetric Link independent of the setting of the TS2 Ordered Sets. A de-skew Ordered Set shall be sent as defined in Section 4.4.4. The scrambler shall load a new seed as defined in Section 4.3.1.5.
 - If the Router initiated exit from CL0s state due to receiving CL1_REQ or CL2_REQ Ordered Sets, then the Router shall not send any Transport Layer Packets before responding to the request Ordered Sets according to the rules in Section 4.2.1.6.2 or with CL_NACK. The Router shall resume regular CL0 operation once it stops sending the CL_NACK Ordered Sets.

Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall:

1. Enable the receiver to start bit and symbol synchronization not earlier than $t_{CLxIdleRx}$ after the last LFPS cycle received. An Adapter shall complete Symbol lock within $t_{WarmUpCL0s}$ time from the reception of the first LFPS cycle.
2. On reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols by the Lane 0 Adapter, the transmitter shall transmit at least 8 back-to-back CL_WAKE2.X Ordered Set Symbols on each enabled Lane of the USB4 Port. Note that Transport Layer traffic is momentarily interrupted to transmit the Symbols. The first CL_WAKE2.X Ordered Set Symbol shall be sent within $t_{WakeResponse}$ after receiving the last bit of the third CL_WAKE1.X Ordered Set Symbol.
 - If the receiver loses Symbol alignment lock after the transmitter sends the CL_WAKE2.X Ordered Set the receiver shall regain Symbol alignment lock within $t_{SymbolLock}$ time.
 - If RS-FEC is on in the transmitting direction, then the transmitted CL_WAKE2.X Ordered Set Symbols are RS-FEC encoded. If RS-FEC is off in the transmitting direction, then the transmitted CL_WAKE2.X Ordered Set Symbols are not RS-FEC encoded.
 - If 3 back-to-back CL_WAKE1.(X+1) Ordered Set Symbols or 3 back-to-back SLOS Symbols are not received within $t_{CL0sSwitch}$ time after receiving a CL_WAKE1.X Symbol, then the Adapter shall transition to the Training.LOCK1 sub-state.
 - If the Link is operating at Gen 2 speed, the Adapter may transmit a partial CL_WAKE2.X Ordered Set in order to send the required number of CL_WAKE2.X Ordered Set Symbols. Otherwise, the Wake Ordered Set shall be transmitted in its entirety.
 - If the Router initiated exit from CL0s state by sending CL1_REQ or CL2_REQ Ordered Sets, then the Router shall continue sending the Ordered Sets instead of sending Transport Layer Packets. The Router shall not send any Transport Layer Packets after sending the first CL1_REQ or a CL2_REQ Ordered Set.
3. On detection of 3 back-to-back SLOS Symbols by all enabled Adapters of the USB4 Port, transmit 16 TS2 Ordered Sets in each enabled Lane of the USB4 Port.
 - If the Router initiated exit from CL0s state by sending CL1_REQ or CL2_REQ Ordered Sets, then the Router may send more than 16 TS2 Ordered Sets on each enabled Lane.
4. On detection of 2 back-to-back TS2 Ordered Sets, transition to CL0 state.
 - If the Router initiated exit from CL0s state by sending CL1_REQ or CL2_REQ Ordered Sets, then the Router shall continue to send the Ordered Sets. The Router shall not send any Transport Layer Packets before completing the CLx entry flow.
 - If the Adapter does not detect 2 back-to-back TS2 Ordered Sets in $t_{TS2Timeout}$ from transmitting TS2 Ordered Sets, the Lane Adapters in the Port shall enter the Training state.

Exit time from CL0s is calculated using the following equations:

Equation 4-3. CL0s Exit Time without Re-timers

$$t_{CL0sExit} \cong t_{WarmUpCL0s} + 3 \times t_{TrainingTransition}$$

Equation 4-4. CL0s Exit Time with Re-timers on Link

$$t_{CL0sExit} \cong t_{WarmUpCL0s} + N_{Retimers} \times (t_{WakeResponse} + t_{SymbolLock}) + (N_{Retimers} - 1) \times t_{SwitchNoSSC} + t_{SwitchSSC} + 3 \times t_{TrainingTransition}$$

Note: $t_{SwitchNoSSC}$ and $t_{SwitchSSC}$ are defined in the USB4 Re-timer specification.

Note: If there are Re-timers on the Link, the Re-timer latency can add up to 2 μ s to the calculated CLx exit time.

In order to limit the CL0s exit time to 245 μ s, a Router shall comply with the following equation:

$$t_{WarmUpCL0s} + 6 \times t_{WakeResponse} + t_{TrainingTransition} < 80\mu s$$

4.2.1.6.5.1.2 Gen 4 CL0s Exit Flow

Only the USB4 Port that initiated the CL0s entry can initiate CL0s exit. If the CL0s exit flow started during entry to CL0s (TX) of the Link Partner, the exit flow happens after the Link is in CL1 or CL2 and according to the flow described in Section 4.2.1.6.5.4.

The USB4 Port initiating exit from CL0s state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on Lane 0. The LFPS duration shall be at least 16 LFPS cycles (see Section 3.4).
 - a. If the receiver detects a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 00t, it shall continue to step 2.
 - b. If the receiver detects LFPS after receiving Gen 4 CL_OFF Ordered Sets, it shall perform the CL1/2 exit flow (starting from Step 1), which is described in Section 4.2.1.6.5.4.
2. Stop transmitting LFPS within $t_{StopLFPS2}$ and return to Electrical Idle for $t_{PreData}$ (see Table 3-33).
3. Start transmitting Gen 4 TS1 with the *Indication* field set to 2h without SSC on all enabled transmitters. The TxFFE Preset shall be the same Preset used prior entry to CL0s.
4. When detecting CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 01t, the USB4 Port shall start transmitting Gen 4 TS2 with the *Indication* field set to 4h on all enabled transmitters. The first Gen 4 TS2 shall be transmitted within $t_{TrainingTransition}$ time after detection of the first CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 01t.
5. When detecting CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 02t, the USB4 Port shall start transmitting Gen 4 TS3 with the *Indication* field set to 5h on all enabled transmitters. The first Gen 4 TS3 shall be transmitted within $t_{TrainingTransition}$ time after detection of the first CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 02t.
6. When detecting CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 10t, the USB4 Port shall start transmitting Gen 4 TS4 with the *Counter* field set to 0h on all enabled transmitters. The first Gen 4 TS4 shall be transmitted within $t_{TrainingTransition}$ time after detection of the first CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 10t.

7. All enabled transmitters shall activate SSC while transmitting Gen 4 TS4 with the *Counter* field set to 0h. The activation of SSC shall be within tActivateSSC time after the first trit of the first TS4. tSSCActivated time after activating the SSC, all enabled transmitters shall start increasing the *Counter* field in the Gen 4 TS4 from 1h to Fh, with one Gen 4 TS4 being transmitted per transmitter for each increment of the *Counter* field.
8. After sending Gen 4 TS4 with the *Counter* field set to Fh, the USB4 Port shall transition to CL0 and activate RS-FEC encoding, Scrambler, and Pre-Coding. The first RS-FEC block shall be a De-skew Block as defined in Section 4.4.4.

If the Enable Gen 4 Link Recovery bit in PORT_CS_19 is set to 1b and the initiating Port does not transition to CL0 state within tTrainingError time after sending the first LFPS, the Port shall initiate a Gen 4 Link Recovery as described in Section 4.4.7.

If the Enable Gen 4 Link Recovery bit in PORT_CS_19 is set to 0b and initiating Port does not transition to CL0 state within tTrainingAbort2 time after sending the first LFPS, the Port shall initiate a Disconnect by driving SBTX to a logical low state for a minimum of tDisconnectTx.

A USB4 Port that is in CL0s (RX) and is not initiating an entry to CL0s (TX) shall do the following when it detects LFPS on its receiver:

1. Transmit 24 CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 00t at the beginning of an RS-FEC block. ~~The first CL0s_EXIT Ordered Set shall be transmitted within tTrainingTransition time after detecting the LFPS.~~ The CL0s_EXIT Ordered Sets shall be distributed among all active transmitters.
 - a. ~~The first CL0s_EXIT Ordered Sets shall be transmitted within tTrainingTransition time after detecting the LFPS on the USB4 Port.~~
 - b. ~~The first CL0s_EXIT Ordered Sets shall be transmitted within tCL0sLFPSResponse timer after detecting the LFPS on the USB Type-C Port, where:~~

$$tCL0sLFPSResponse = N_{obr} \times tOBCL1ForwardLFPS + tTrainingTransition$$
2. Activate all enabled receivers in PAM2, tCLxIdleRx time after the last LFPS was received.
3. When detecting Gen 4 TS1 with the *Indication* field set to 2h, switch all enabled receivers to PAM3 and transmit 24 CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 01t at the beginning of an RS-FEC block. The detection of Gen 4 TS1 shall be within tWarmUpCL0s time after the first LFPS. The first CL0s_EXIT Ordered Set shall be transmitted within tTrainingTransition time after detecting the Gen 4 TS1 with the *Indication* field set to 2h.
4. When detecting Gen 4 TS2 with the *Indication* field set to 4h, transmit 24 CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 02t at the beginning of an RS-FEC block. The first CL0s_EXIT Ordered Set shall be transmitted within tTrainingTransition time after detecting the Gen 4 TS2 with the *Indication* field set to 4h.
5. When detecting Gen 4 TS3 with the *Indication* field set to 5h, transmit 24 CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 10t at the beginning of an RS-FEC block. The first CL0s_EXIT Ordered Set shall be transmitted within tTrainingTransition time after detecting the Gen 4 TS3 with the *Indication* field set to 5h.
6. The receivers shall transition to CL0 after receiving Gen 4 TS4 with the *Counter* field set to Fh.

The Responding Port shall not initiate entry to Low Power state during the above flow.

If the Enable Gen 4 Link Recovery bit in PORT_CS_19 is set to 1b and the Responding Port does not transition to CL0 state within tTrainingError time after detecting the first LFPS, the Port shall initiate a Gen 4 Link Recovery as described in Section 4.4.7.

If the Enable Gen 4 Link Recovery bit in PORT_CS_19 is set to 0b and Responding Port does not transition to CL0 state within tTrainingAbort2 time after detecting the first LFPS, the Port shall initiate a Disconnect by driving SBTX to a logical low state for a minimum of tDisconnectTx.

Exit time from CL0s is calculated by the following equation:

Equation 4-5. CL0s Exit Time with Re-timers on Link

$$t_{CL0sExit} \cong t_{WarmUpCL0s} + N_{Retimers} \times t_{SwitchNoSSC} + 6 \times t_{TrainingTransition} + t_{ActivateSSC} + t_{SSCActivated}$$

Note: The USB4 Port requirements in this specification can only be verified for Router Assemblies without On-Board Re-timers, by monitoring the USB Type-C Port associated with the USB4 Port due to lack of observability. However, for Router Assemblies with On-Board Re-timers the USB4 Ports are still expected to meet the behavior and timing requirements in this specification to satisfy the CLx exit time assumptions.

The timing requirements for a Router Assembly which includes On-Board Re-timers are subject to the following assumptions:

- Each On Board Re-timer is forwarding LFPS per direction within tOBCL1ForwardLFPS as recommended in the USB4 Re-Timer Specification. Note that the actual LFPS forwarding latency cannot be qualified for On-Board Re-Timer in Router Assemblies and only taken as an assumption for end-to-end latency calculations.

4.2.1.6.5.2 Gen 2 and Gen 3 Exit flow from CL1 or CL2 state (No Re-timers on the Link)

This section applies when there are no USB4 Re-timers on the Link.

The USB4 Port initiating exit from CL1 or CL2 state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until the receiver detects LFPS. If the receiver did not detect LFPS after tTrainingAbort2 time the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
2. Return to Electrical Idle for tPreData.
3. Start transmitting SLOS1 on the Lane.
 - A USB4 Port may exit CL2 or CL1 state with SSC enabled or disabled.
4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
5. Transition the Lane Adapter to Training.LOCK1 sub-state.
 - On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.

If the Adapter did not reach Training.LOCK1 sub-state tTrainingAbort2 time after LFPS transmission has started, the Router should initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.



IMPLEMENTATION NOTE

A single tTrainingAbort2 Timer used for step 1 and up to step 5 can be implemented.

Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on the Lane for a duration of at least 5 LFPS cycles (see Section 3.7) and for no more than $t_{LFPSDuration}$. If the Lane Adapter is in CL1 state, the first LFPS shall be sent within $t_{WarmUpCL1}$ after receiving the first LFPS cycle. If the Lane Adapter is in CL2 state, the first LFPS shall be sent within $t_{WarmUpCL2}$ after receiving the first LFPS cycle.
2. Return to Electrical Idle for $t_{PreData}$.
3. Start transmitting SLOS1 on the Lane.
 - A USB4 Port may exit CL2 or CL1 state with SSC enabled or disabled.
4. Enable the receiver to start bit and symbol synchronization not earlier than $t_{CLxIdleRx}$ after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within t_{RxLock} time.
5. Transition to Training.LOCK1 sub-state.
 - On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.

Exit time from CL1 and CL2 states is calculated by the following equations:

Equation 4-64-5. CL1 Exit Time with no Re-timers

$$t_{CL1Exit} = t_{WarmUpCL1} + t_{LFPSDuration} + t_{RxLock} + 4 \times t_{TrainingTransition}$$

Equation 4-74-6. CL2 Exit Time with no Re-timers

$$t_{CL2Exit} = t_{WarmUpCL2} + t_{LFPSDuration} + t_{RxLock} + 4 \times t_{TrainingTransition}$$

4.2.1.6.5.3 Gen 2 and Gen 3 Exit flow from CL1 or CL2 state (Re-timers on the Link)

This section applies when there is at least one USB4 Re-timer on the Link.

The USB4 Port initiating exit from CL1 or CL2 state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until its receiver detects LFPS. If the receiver did not detect LFPS after $t_{TrainingAbort2}$ time the Router shall initiate a Disconnect by driving SBTX to a logical low state for $t_{DisconnectTx}$.
2. Return to Electrical Idle for $t_{PreData}$.
3. Start transmitting SLOS1 on the Lane.
 - A USB4 Port may exit CL2 or CL1 state with SSC enabled or disabled.
4. Enable the receiver to start bit and symbol synchronization not earlier than $t_{CLxIdleRx}$ after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within t_{RxLock} time.
5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The first CL_WAKE2.X Ordered Set Symbol shall be sent within $t_{WakeResponse}$ after receiving the third CL_WAKE1.X Ordered Set Symbol. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Ordered Set Symbols interleaved with CL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set Symbols. If the receiver loses Symbol alignment lock after the transmitter sends the CL_WAKE2.X Ordered Set, the receiver shall regain Symbol alignment lock within $t_{SymbolLock}$ time.

6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, send SLOS1 for tTXSLOS time, then transition the Adapter to Training.LOCK1 sub-state within tWakeResponse time.
 - On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.

If the Adapter did not reach Training.LOCK1 sub-state tTrainingAbort2 time after LFPS transmission has started, the Router should initiate a Disconnect by driving SBTx to a logical low state for tDisconnect Tx.



IMPLEMENTATION NOTE

A single tTrainingAbort2 Timer used for step 1 and up to step 6 can be implemented.

Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on the Lane for a duration of at least 5 LFPS cycles (see Section 3.7) and for no more than tLFPSDuration. If the Lane Adapter is in CL1 state, the first LFPS shall be sent within tWarmUpCL1 after receiving the first LFPS cycle. If the Lane Adapter is in CL2 state, the first LFPS shall be sent within tWarmUpCL2 after receiving the first LFPS cycle.
2. Return to Electrical Idle for tPreData.
3. Start transmitting SLOS1 on the Lane.
 - A USB4 Port may exit CL2 or CL1 state with SSC enabled or disabled.
4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. An Adapter shall complete Symbol lock within tRxLock time.
5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The first CL_WAKE2.X Ordered Set Symbol shall be sent within tWakeResponse after receiving the third CL_WAKE1.X Ordered Set Symbol. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Ordered Set Symbols interleaved with CL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set Symbols. If the receiver loses Symbol lock after sending the CL_WAKE2.X Ordered Set it shall regain Symbol lock within tSymbolLock time.
6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, send SLOS1 for tTXSLOS time, then transition to Training.LOCK1 sub-state.
 - On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.

Exit time from CL1 and CL2 states is calculated by the following equations:

Equation 4-84-7. CL1 Exit Time with Re-timers on the Link

$$t_{CL1Exit} = t_{WarmUpCL1} + t_{LFPSDuration} + (N_{Re-timers} + 1) \times (t_{WakeResponse} + t_{SymbolLock}) + t_{SwitchSSC} + t_{CLxLock} + (N_{Re-timers} - 1) \times t_{SwitchNoSSC} + 4 \times t_{TrainingTransition}$$

Equation 4-94-8. CL2 Exit Time with Re-timers on the Link $t_{CL2Exit}$

$$= t_{WarmUpCL2} + t_{LFPSDuration} + (N_{Re-timers} + 1) \times (t_{WakeResponse} + t_{SymbolLock}) + t_{SwitchSSC} + t_{CLxLock} + (N_{Re-timers} - 1) \times t_{SwitchNoSSC} + 4 \times t_{TrainingTransition}$$

Note: $t_{SwitchNoSSC}$, $t_{SwitchSSC}$ and $t_{CLxLock}$ are defined in the USB4 Re-timer specification.

Note: If there are Re-timers on the Link, the Re-timer latency can add up to 2 μ s to the calculated CLx exit time.

4.2.1.6.5.4 Gen 4 Exit Flow from CL1 or CL2 State

A USB4 Port may initiate exit from CL1 or CL2 state due to an internal objection or detection of one or more LFPS cycles on its Lane 0 receiver. When initiating exit from CL1 or CL2 state, a USB4 Port shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on Lane 0 until all the following two conditions are met:
 - The receiver detected LFPS.
 - After the receiver detected LFPS, the transmitter sent at least 16 LFPS cycles.

If exit was initiated by detecting LFPS, the Port ~~may~~shall apply at least one of the third condition following conditions:

- The receiver no longer detects LFPS.
- $t_{EnterLFPS3}$ time passed since the Port shut down its transmitter.

If the Port is in CL0s (RX) and detected LFPS on its receiver while entering CL1 or CL2 by transmitting CL OFF, it shall behave as if the exit from CL1/2 was initiated by detecting LFPS even if it has an internal objection.

The Port shall stop sending LFPS within $t_{StopLFPS2}$ time after the conditions above are met.

If the exit from CL1 or CL2 was initiated by detecting LFPS on the Lane 0 receiver, the Port shall transmit the LFPS on the Lane 0 transmitter within $t_{WarmupCL1}$ or $t_{WarmupCL2}$ respectively.

If the Enable Gen 4 Link Recovery bit in PORT_CS_19 is set to 1b and the Port did not transition to CL0 state within $t_{TrainingError}$ time, the Router shall initiate a Gen 4 Link Recovery as described in Section 4.4.7.

If the Enable Gen 4 Link Recovery bit in PORT_CS_19 is set to 0b and the Port did not transition to CL0 state within $t_{TrainingAbort2}$ time, the Router shall initiate a Disconnect by driving SBTX to a logical low state for $t_{DisconnectTx}$.

2. Return to Electrical Idle for $t_{PreData}$ (see Table 3-33).
3. Transition to the Training.TS1 sub-state using the TxFFE Preset that was used prior to CL1/2 entry.
4. Each Lane Adapter shall complete Symbol lock within t_{RxLock} time and proceed as described in 4.2.1.3.2.2, without performing the TxFFE negotiation flow, until the transition to CL0 state.
5. The first RS-FEC block shall be a De-skew Block as defined in Section 4.4.4.

The exit time from CL1 and CL2 states is calculated using the following equations:

Equation 4-10. CL1 Exit Time

$$t_{CL1_Exit} = t_{WarmUpCL1} + 32 \times t_{Period} + 2 \times t_{StopLFPS2} + t_{Gen4TS2Lock} + t_{RxLock} + N_{obr} \times (t_{SwitchNoSSC} + t_{OBCL1ForwardLFPS}) + (N_{Re-timer} - N_{obr}) \times (t_{SwitchNoSSC} + t_{CL1ForwardLFPS}) + 4 \times t_{TrainingTransition} + t_{ActivateSSC} + t_{SSCActivated}$$

Equation 4-11. CL2 Exit

$$t_{CL2_Exit} = t_{WarmUpCL2} + 32 \times t_{Period} + 2 \times t_{StopLFPS2} + t_{Gen4TS2Lock} + t_{RxLock} + N_{obr} \times (t_{SwitchNoSSC} + t_{OBCL2ForwardLFPS}) + (N_{Re-timer} - N_{obr}) \times (t_{SwitchNoSSC} + t_{CL2ForwardLFPS}) + 4 \times t_{TrainingTransition} + t_{ActivateSSC} + t_{SSCActivated}$$

4.2.2 USB4 Link Transitions

A USB4 Port shall support the following Link configurations:

- One Single-Lane Link (Gen 2 and Gen 3 Only).
 - Lane 0 Adapter is enabled and in CL0 state. Lane 1 Adapter is disabled.
 - *Negotiated Link Width* = x1.

Note: This is a fallback configuration that occurs if the Connection Manager disables Lane 1 after Lane Initialization or Lane Bonding fail. This Link Configuration is also referred to as "Symmetric x1 Lane".

- Two independent Single-Lane Links (Gen 2 and Gen 3 only).
 - Both the Lane 0 Adapter and Lane 1 Adapter are enabled and in CL0 state.
 - Lane 0 and Lane 1 are not bonded.
 - *Negotiated Link Width* = x1.

Note: This is a transient configuration that occurs between successful completion of Lane Initialization and successful completion Lane Bonding. This Link Configuration only occurs for a Gen 2 or Gen 3 Link.

- Symmetric Link.
 - Both the Lane 0 Adapter and Lane 1 Adapter are enabled and in CL0 state.
 - For a Gen 2 or Gen 3 Link, Lane 0 and Lane 1 are successfully bonded.
 - *Negotiated Link Width* = x2.
- Asymmetric Link (Gen 4 Only).
 - The USB4 Port on one side of the Link operates with 3 transmitters and 1 receiver. The USB4 Port on the other side of the Link operates with 3 receivers and 1 transmitter.
 - This Link Configuration is only supported when the Link is Gen 4 speed.

Note: This Link configuration can be initiated during Lane Initialization. It can also be initiated by the Connection Manager when the Link is in the Symmetric Link configuration.



CONNECTION MANAGER NOTE

A Connection Manager shall disable the Lane 1 Adapter if, after Lane Initialization, the Lane 1 Adapter is in CL0 state but the Lane 0 Adapter is not in CL0 state.

4.2.2.1 Transition from One Single-Lane Link to Two Single-Lane Links

A USB4 Port shall transition from one Single-Lane Link to two Single-Lane Links when the Lane 1 Adapter is enabled. The transition from one Single-Lane to two Single-Lane Links is complete when the Lane 1 Adapter transitions to the CL0 state.



CONNECTION MANAGER NOTE

A Connection Manager shall not enable any Path other than Path 0 in a USB4 Port with two Single-Lane Links that have not yet been bonded.

4.2.2.2 Transition from Two Single-Lane Links to Symmetric Link

A Connection Manager sets the *Lane Bonding* bit to 1b in the Lane Adapter Configuration Capability of the Lane 0 Adapter in a USB4 Port to initiate bonding two Single-Lane Links into a Symmetric Link. This causes the Lane Adapters in the USB4 Port to transition to the Lane Bonding state (see Section 4.2.1.5).



CONNECTION MANAGER NOTE

A Connection Manager shall only set the Lane Bonding bit to 1 if the Target Link Width fields in the Ports at both side of the Link allow a Symmetric Link.

A Connection Manager shall set the Lane Bonding bit to 1 in the Lane 0 Adapter of the Downstream Facing Port.

A USB4 Port shall transition its Lane Adapters to the Lane Bonding state when all the following are true:

- The *Supported Link Widths* field in the Lane Adapter Configuration Capability register of both Adapters is set to x2 support or more.
- The *Target Link Width* field in the Lane Adapter Configuration Capability register of both Adapters is set to establish a Symmetric Link.

The Logical Layer shall transition to a Symmetric Link when the following conditions are met:

- Both Adapters have transitioned successfully to CL0 state within *tBonding* time after sending the first TS1 Ordered Set with *Lane Bonding Target* set to 001b.
- Link Partner has responded on both Lanes with TS1 and TS2 Ordered Sets that have the *Lane Bonding Target* field set to 001b.

Note: If the Lane Adapter transitions from Bonding state to Training state due to an error on the Link and still manages to transition to CL0 state within tBonding time from entry to Bonding state, it is considered a successful transition.

If Lane bonding is successful, then a Router shall:

- Set the *Adapter State* field in the Lane Adapter Configuration Capability of the Lane 0 Adapter to CL0.

- Set the *Negotiated Link Width* field in the Lane Adapter Configuration Capability of the Lane 0 Adapter to indicate a USB4 Link width of x2.
- Send a Hot Plug Event Packet with the *UPG* bit set to 1b for the Lane 1 Adapter in the Downstream Facing Port.

Note: After successful Lane bonding, the Lane 1 Adapter is “unplugged” and the Configuration Space of the Lane 0 Adapter is used to configure the Link.

If one of the Lane Adapters is not in CL0 tBonding time after entry to the Lane Bonding state, the Router shall initiate a Disconnect by driving SBTx to a logical low state for tDisconnectTx.



CONNECTION MANAGER NOTE

A Connection Manager can conclude that Lane bonding failed if, after initiating Lane Bonding, it receives a Hot Plug Event Packet with UPG=1 for Lane 0.

The Connection Manager decides what to do after a bonding failure. The Connection Manager can retry Lane bonding, configure a Single-Lane Link, or take other measures based on the desired policy.

The Adapters of a Symmetric Link operate in CL0 state in tandem with the following dependencies:

- Any Ordered Set sent on the Link shall be sent simultaneously on both Lanes within the permitted transmit skew.
- When either Adapter of a Symmetric Link transitions to one of the Training sub-states, the other Adapter in the USB4 Port shall transition to the same Training sub-state.

4.2.2.2.1 Training a Symmetric Link

When an Adapter that is part of a Symmetric Link enters Training state, the other Adapter in the USB4 Port shall enter Training state as well. During the training state, Lane Bonding is re-initiated when the Adapters of a Symmetric Link enter Training state from CL0, CL1, or CL2 states. While attempting to bond the Lanes, the following values are sent during Training state in all TS1 and TS2 Ordered Sets:

- *Lane Bonding Target* is set to 001b.
- *Lane Bonding Target 2* is set to 001b.

The Logical Layer shall resume Symmetric Link operation if both Adapters meet the transition conditions in Step 6 of the Training state machine in Table 4-32 within tTrainingAbort2 time. The Adapter that transitions to the CL0 state first shall send TS2 Ordered Sets until the other Adapter in the USB4 Port exits the training state.

If either Adapter does not meet the transition conditions in Step 6 of the Training state machine within tTrainingAbort2 time, then the Adapters initiate a disconnect (see Section 4.2.1.3.3).

4.2.2.3 Transition from Symmetric Link to Two Single-Lane Links

When a USB4 Port that is operating with a Symmetric Link is reset, the USB4 Port transitions to two Single-Lane USB4 Links after the USB4 Port completes Lane Initialization of its Lanes (see Section 4.1.2 for Lane Initialization flow).

**CONNECTION MANAGER NOTE**

To transition a Link from a Symmetric Link to a Single-Lane Link, a Connection Manager should reset the Link and wait for Lane Initialization to complete. After Lane Initialization is complete, the Connection Manager can disable the Lane 1 Adapter to transition to a Single-Lane Link.

4.2.2.4 Transition from Two Single-Lane Links to One Single-Lane Link

A USB4 Port shall transition from two Single-Lane Links to one Single-Lane Link when one of its Adapters transitions to the Disabled state.

**CONNECTION MANAGER NOTE**

A Connection Manager disables the Lane 1 Adapter in a USB4 Port to transition to a Single-Lane Link. The Connection Manager shall transition a Symmetric Link to Two Single-Lane Links (see Section 4.2.2.3), before disabling the Lane 1 Adapter.

A Connection Manager shall not disable the Lane 0 Adapter of a USB4 Port until after it has disabled the Lane 1 Adapter.

4.2.2.5 Transition from Symmetric to Asymmetric Link

The transition to an Asymmetric Link is controlled by the Connection Manager. The transition to an Asymmetric Link is only possible if the current Link is a Symmetric Link.

Only a Gen 4 Link in a single Domain can support an Asymmetric Link. A USB4 Port may support the Asymmetric Link configuration with 3 transmitters and 1 receiver or 1 transmitter and 3 receivers.

**CONNECTION MANAGER NOTE**

The Connection Manager shall not initiate an Asymmetric transition on Inter-Domain Links.

The Connection Manager does the following before starting the transition from Symmetric Link to Asymmetric Link:

- *Disable CLx states on both sides of a Link. The Connection Manager may enable CLx states after the transition completes.*
- *Disable Gen 4 Link Recovery flow. The Connection Manager may enable Gen 4 Link Recovery flow after the transition completes.*
- *Set the Target Asymmetric Link field on both sides of the Link.*

The Connection Manager then sets the StartAsymmetricFlow field in the USB4 Port that switches from Tx1 to Rx2 to initiate the transition to an Asymmetric Link.

If the *Target Asymmetric Link* field is set to 01b, the USB4 Port transitions to operation with 3 transmitters and 1 receiver as described in Section 4.2.2.5.1. If the *Target Asymmetric Link* field is set to 10b, the USB4 Port transitions to operation with 1 transmitter and 3 receivers as described in Section 4.2.2.5.2. If the *Target Asymmetric Link* field is set to 00b, the USB4 Port transitions from an Asymmetric Link to a Symmetric Link as described in Section 4.2.2.6.

If the transition from Symmetric Link to Asymmetric Link does not finish within *tTrainingAbort1* time, the USB4 Port that received the UNBOND Ordered Sets will initiate a disconnect by driving SBTx to a logical low state for *tDisconnectTx*.

4.2.2.5.1 Transition from Symmetric Link to 3 Transmitters and 1 Receiver

A USB4 Port shall follow the steps below when transitioning to operation with 3 transmitters and 1 receiver:

1. After detecting an UNBOND Ordered Set on its receivers, the USB4 Port shall receive Data Sets only from the receiver of Lane 0 (Rx0) at the end of the RS-FEC block that holds the UNBOND Ordered Set.
2. After detecting a CL_OFF Ordered Set on the receiver of Lane 1 (Rx1), the USB4 Port shall shut down the receiver (Rx1) and prepare to switch it to a transmitter.
3. When the USB4 Port receives an LT_SwitchRx2Tx Transaction it shall:
 - a. Change the mapping of Gen 4 TxFFE register in the SB Register Space to “Asymmetric – USB4 Port has 3 Transmitters”.
 - b. Set the Common Mode voltage on the new transmitter.
 - c. Transmit an LT_SwitchAck Transaction within tSwitchAck after receiving the LT_SwitchRx2Tx Transaction.
4. The USB4 Port shall activate the new transmitter (Tx2) and start sending LFPS only on the new transmitter (Tx2). The first LFPS cycle shall be sent tActivateNewTx time after the LT_SwitchAck Transaction was sent. The transmitter shall continue sending LFPS until the USB4 Port’s receiver detects CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 00t.
5. When the USB4 Port receivers detect a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 00t, it shall stop sending LFPS on Tx2 within tStopLFPS1.
6. The new transmitter (Tx2) shall return to Electrical Idle for tPreData.
7. The new transmitter (Tx2) shall start transmitting back-to-back Gen 4 TS1 with the *Indication* field set to 2h. The new transmitter shall set the *Start TxFFE* bit in the Tx Status byte of the Gen 4 TxFFE register in the SB Register Space of the adjacent Router/Re-timer and execute the Gen 4 Transmitter flow for TxFFE negotiation as described in Section 4.1.2.5.1.1.2. Since all transmitters are using the same clock source, the new transmitter (Tx2) transmits the Gen 4 Training Sequences with the common SSC modulation. Note that the new receiver does not need to check Start TxFFE bit in its local Gen 4 Partner Tx Status byte before starts the receiver flow. It is not required that a Router write to the Start TxFFE as defined in Section 4.1.2.4 (Step 4a).
8. When the USB4 Port receivers detect a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 01t, the new transmitter shall start transmitting back-to-back TS2 with the *Indication* field set to 4h. The new transmitter shall continue executing the Gen 4 Transmitter flow for TxFFE negotiation as described in Section 4.1.2.5.1.1.2.
9. When the USB4 Port receivers detect a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 02t, indicating that TxFFE negotiation has finished, the new transmitter (Tx2) shall start transmitting back-to-back TS3 with the *Indication* field set to 5h.
10. When the USB4 Port receivers detect a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 10t, the new transmitter (Tx2) shall start transmitting back-to-back TS4 with the *Counter* field increasing in value from 0h to Fh. After sending the TS4 with *Counter* field set to Fh, the new transmitter shall activate its scrambler with the initial seed as described in Table 4-66 and with pre-coding.
11. The new transmitter shall transmit back-to-back DESKEW.0 Ordered Sets or Data Sets.
12. When Tx2 is transmitting DESKEW.0 Ordered Sets or Data Sets, upon an RS-FEC block start (either the first RS-FEC block start or upon any subsequent RS-FEC block start

while Tx2 is transmitting DESKEW.0 Ordered Set or Data Sets), the USB4 Port shall transmit a De-skew Block on all 3 transmitters. The De-skew Block is defined in Section 4.4.4.

13. After the De-skew Block is transmitted, the transition is finished. The USB4 Port shall distribute Data Sets between all 3 active transmitters. The USB4 Port shall send each Ordered Set on all 3 active transmitters. The USB4 Port shall set the *Negotiated Link Width* field to indicate an Asymmetric Link with 3 transmitters.

14. If the USB4 Port is a Downstream Facing Port, the Router shall send a Notification Packet with Event Code = ASYM_LINK to the Connection Manager (see Section 6.5).

If it takes longer than tTrainingAbort1 time from receiving the UNBOND Ordered Set to transmitting the De-skew Block, a USB4 Port shall initiate a disconnect by driving SBTX to logical low state for tDisconnectTx time.

4.2.2.5.2 Transition from Symmetric Link to 1 Transmitter and 3 Receivers

When the *StartAsymmetricFlow* bit is set to 1b, a USB4 Port shall follow the steps below to transition to operation with 1 transmitter and 3 receivers:

1. Set the *AsymmetricTransitionInProgress* bit to 1b.
2. Transmit an RS-FEC block with 120 UNBOND Ordered Sets and 6 Redundancy Sets. After transmitting the RS-FEC block with the UNBOND Ordered Sets, all subsequent RS-FEC blocks shall be transmitted on Tx0 only.
3. Tx1 shall initiate entry to CL0s state as follows:
 - a. Send 126 CL_OFF Ordered Sets with the *CLx State* field set to 1t and the *Index* field set to 00t. The transmitter may replace any of the last 102 CL_OFF Ordered Sets with any valid Data Set.
 - b. If there are Re-timers on the Link, send a series of 126 CL_OFF Ordered Sets with the *CLx State* field set to 1t for each Re-timer on the Link. The *Index* field in the first series of CL_OFF Ordered Sets shall be set to 01t. The *Index* field in each subsequent series of CL_OFF Ordered Sets shall increment by 1 for each series. For example, for a Link with 3 Re-timers, the first additional 126 CL_OFF Ordered Sets have the *Index* field set to 01t, the second additional 126 CL_OFF Ordered Sets have the *Index* field set to 02t, and the third additional 126 CL_OFF Ordered Sets have the *Index* field set to 03t. The transmitter may replace any of the last 102 CL_OFF Ordered Sets (for each Re-timer) with any valid Data Set.

Note: The receiver does not need to process any of the Data Symbols inserted by the transmitter as a substitute for the CL_OFF Ordered Sets.

- c. Disable Tx1 tTxOff time after sending the last CL_OFF Ordered Set. The Adapter may send any valid Symbols during the tTxOff period.
 - d. Enable Rx2 (which uses the same physical lines as Tx1). Receiver termination shall be applied when the new receiver is enabled.
4. Change the mapping of the Gen 4 TxFFE register in the SB Register Space to "Asymmetric – USB4 Port has 3 Receivers".
5. Send an LT_SwitchRx2Tx Transaction on the Sideband channel.
6. After receiving an LT_SwitchAck Transaction, enable LFPS detection on the new receiver (Rx2).
7. When the USB4 Port detects LFPS on Rx2, it shall do the following:
 - a. The USB4 Port shall transmit 24 CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 00t on its active transmitter at the beginning of an RS-FEC block.

- b. The new receiver (Rx2) shall enable high speed signal reception tCLxIdleRx time after the end of the last LFPS cycle is received and shall execute the Gen 4 receiver flow for TxFFE negotiation as described in Section 4.1.2.5.1.2.2. The receiver shall keep the *New Request* value of the Link Partner's transmitters (Tx0 and Tx1) set to 0b. Note that the new receiver does not need to check Start TxFFE bit in its local Gen 4 Partner Tx Status byte before starts the receiver flow. It is not required that a Router write to the Start TxFFE as defined in Section 4.1.2.4 (Step 4a).
 - c. When the new receiver (Rx2) is ready to switch to PAM3 and after detecting TS1 with the *Indication* field set to 2h, the USB4 Port shall transmit 24 CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 01t. The 24 CL0s_EXIT Ordered Sets shall be transmitted on the USB4 Port's active transmitter at the beginning of an RS-FEC block.
 - d. When it detects Gen 4 TS2, the USB4 Port shall continue executing the Gen 4 receiver flow for TxFFE negotiation as described in Section 4.1.2.5.1.2.2.
 - e. When the new receiver (Rx2) has finished the Gen 4 TxFFE negotiation and after detecting Gen 4 TS2 with the *Indication* field set to 4h, the USB4 Port shall transmit 24 CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 02t. The 24 CL0s_EXIT Ordered Sets shall be transmitted on the USB4 Port's active transmitter at the beginning of an RS-FEC block.
 - f. When it detects TS3 with the *Indication* field set to 5h, the USB4 Port shall transmit 24 CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 10t. The 24 CL0s_EXIT Ordered Sets shall be transmitted on the USB4 Port's active transmitter at the beginning of an RS-FEC block.
 - g. The USB4 Port shall start using all 3 receivers after a De-skew Block is received on all 3 receivers.
8. The USB4 Port shall set the *Negotiated Link Width* field to indicate an Asymmetric Link with 3 receivers.
 9. The USB4 Port shall set the *AsymmetricTransitionInProgress* bit to 0b.
 10. If the USB4 Port is a Downstream Facing Port, the Router shall send a Notification Packet with Event Code = ASYM_LINK to the Connection Manager (see Section 6.5)

If it takes longer than tTrainingAbort1 time from receiving the UNBOND Ordered Set to transmitting the De-skew Block, a USB4 Port shall initiate a disconnect by driving SBTx to logical low state for tDisconnectTx time.

4.2.2.6 Transition from Asymmetric Link to Symmetric Link

The Connection Manager controls the transition from an Asymmetric Link to a Symmetric Link. Section 4.2.2.6.1 describes the transition from an Asymmetric Link with 3 transmitters and 1 receiver. Section 4.2.2.6.2 describes the transition from an Asymmetric Link with 1 transmitter and 3 receivers.



CONNECTION MANAGER NOTE

The Connection Manager does the following before starting the transition from Asymmetric Link to Symmetric Link:

- *Disable CLx states on both sides of a Link. The Connection Manager may enable CLx states after the transition completes.*
- *Disable Gen 4 Link Recovery flow. The Connection Manager may enable Gen 4 Link Recovery flow after the transition completes.*
- *Set the Target Asymmetric Link field on both sides of the Link.*

The Connection Manager then sets the `StartAsymmetricFlow` field in the USB4 Port that switches from Tx2 to Rx1 to initiate the transition to a Symmetric Link.

If the transition from Asymmetric Link to Symmetric Link does not finish within `tTrainingAbort1` time, the USB4 Port that received the UNBOND Ordered Sets will initiate a disconnect by driving SBTx to a logical low state for `tDisconnectTx`.

4.2.2.6.1 Transition from 3 Transmitters and 1 Receiver to Symmetric Link

When the `StartAsymmetricFlow` bit is set to 1b, a USB4 Port shall follow the steps below to transition from operation with 3 transmitters and 1 receiver to a Symmetric Link:

1. Set the `AsymmetricTransitionInProgress` bit to 1b.
2. Transmit an RS-FEC block with 120 UNBOND Ordered Sets and 6 Redundancy Sets. After transmitting the RS-FEC block, the USB4 Port shall only transmit data on two transmitters (Tx0 and Tx1).
3. Tx2 shall initiate entry to CL0s as follows:
 - a. Send 126 CL_OFF Ordered Sets with the `CLx State` field set to 1t and the `Index` field set to 00t. The transmitter may replace any of the last 102 CL_OFF Ordered Sets with any valid Data Set.
 - b. If there are Re-timers on the Link, send a series of 126 CL_OFF Ordered Sets with the `CLx State` field set to 1t for each Re-timer on the Link. The `Index` field in the first series of CL_OFF Ordered Sets shall be set to 01t. The `Index` field in each subsequent series of CL_OFF Ordered Sets shall increment by 1 for each series. For example, for a Link with 3 Re-timers, the first additional 126 CL_OFF Ordered Sets have the `Index` field set to 01t, the second additional 126 CL_OFF Ordered Sets have the `Index` field set to 02t, and the third additional 126 CL_OFF Ordered Sets have the `Index` field set to 03t. The transmitter may replace any of the last 102 CL_OFF Ordered Sets (for each Re-timer) with any valid Data Set.

Note: The receiver does not need to process any of the Data Symbols inserted by the transmitter as a substitute for the CL_OFF Ordered Sets.

 - c. Disable Tx2 `tTxOff` time after sending the last CL_OFF Ordered Set. The Adapter may send any valid Data Symbols during the `tTxOff` period.
 - d. Enable Rx1 (which uses the same physical lines as Tx2). Receiver termination shall be applied when the new receiver is enabled.
4. Change the mapping of the Gen 4 TxFFE register in the SB Register Space to "Symmetric".
5. Send an LT_SwitchRx2Tx Transaction on the Sideband Channel.
6. After receiving an LT_SwitchAck Transaction, enable LFPS detection on the new receiver (Rx1).
7. When the USB4 Port detects LFPS on Rx1 it shall do the following:
 - a. The USB4 Port shall transmit 24 CL0s_EXIT Ordered Sets with the `CL0s Phase` field set to 00t. The 24 CL0s_EXIT Ordered Sets shall be transmitted on the Port's active transmitters at the beginning of an RS-FEC block.
 - b. The new receiver (Rx1) shall enable high speed signal reception `tCLxIdleRx` time after the end of the last LFPS cycle is received and shall execute the Gen 4 receiver flow for TxFFE negotiation as described in Section 4.1.2.5.1.2.2. The receiver shall keep the *New Request* value of the existing transmitter (Tx0) set to

- 0b. It is not required that a Router write to the Start TxFFE as defined in Section 4.1.2.4 (Step 4a).
- c. When the new receiver (Rx1) is ready to switch to PAM3 and after detecting TS1 with the *Indication* field set to 2h, the USB4 Port shall transmit 24 CL0s_EXIT Ordered Sets with the *CL0s Phase* field set to 01t. The 24 CL0s_EXIT Ordered Sets shall be transmitted on its active transmitters at the beginning of an RS-FEC block.
- d. When it detects Gen 4 TS2, the USB4 Port shall continue executing the Gen 4 receiver flow for TxFFE negotiation as described in Section 4.1.2.5.1.2.2.
- e. When the new receiver (Rx1) has finished the Gen 4 TxFFE negotiation and after detecting Gen 4 TS2 with the *Indication* field set to 4h, the USB4 Port shall transmit 24 CL0s_EXIT Ordered Set with *CL0s Phase* field set to 02t. The 24 CL0s_EXIT Ordered Sets shall be transmitted on its active transmitters at the beginning of an RS-FEC block.
- f. When it detects TS3 with the *Indication* field set to 5h, the USB4 Port shall transmit 24 CL0s_EXIT Ordered Set with *CL0s Phase* field set to 10t. The 24 CL0s_EXIT Ordered Sets shall be transmitted on its active transmitters at the beginning of an RS-FEC block.
- g. The USB4 Port shall start using 2 receivers after receiving a De-skew Block.
- 8. The USB4 Port shall set the *Negotiated Link Width* field to indicate a Symmetric Link.
- 9. The USB4 Port shall set the *AsymmetricTransitionInProgress* bit to 0b.
- 10. If the USB4 Port is a Downstream Facing Port, the Router shall send a Notification Packet with Event Code = ASYM_LINK to the Connection Manager (see Section 6.5).

If it takes longer than tTrainingAbort1 time from receiving the UNBOND Ordered Set to transmitting the De-skew Block, a USB4 Port shall initiate a disconnect by driving SBTX to logical low state for tDisconnectTx time.

4.2.2.6.2 Transition from 1 Transmitter and 3 Receivers to Symmetric Link

A USB4 Port shall follow the steps below when transitioning from operation with 1 transmitter and 3 receivers to a Symmetric Link:

1. After detecting UNBOND Ordered Sets on its receivers, the USB4 Port shall stop gathering Data Sets from its 3 receivers and receive Data Sets only from 2 receivers (Rx0 and Rx1) at the end of the RS-FEC block that holds the UNBOND Ordered Sets.
2. After detecting CL_OFF Ordered Sets on the third receiver (Rx2), the USB4 Port shall shut down the receiver (Rx2) and make the preparations to switch it to a transmitter.
3. When the USB4 Port receives an LT_SwitchRx2Tx Transaction it shall:
 - a. Change the mapping of the Gen 4 TxFFE register in the SB Register Space to "Symmetric".
 - b. Set the Common Mode voltage on the new transmitter.
 - c. Transmit an LT_SwitchAck Transaction within tSwitchAck from receiving the LT_SwitchRx2Tx Transaction.
4. Activate the new transmitter (Tx1) and start sending LFPS only on the new transmitter (Tx1). The first LFPS cycle shall be sent tActivateNewTx time after the LT_SwitchAck Transaction was sent. The transmitter shall continue sending LFPS until the USB4 Port's receiver detects a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 00t.

5. When the USB4 Port detects a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 00t on its receivers, it shall stop sending LFPS on Tx1 within tStopLFPS1.
6. The new transmitter (Tx1) shall return to Electrical Idle for tPreData.
7. The new transmitter (Tx1) shall start transmitting back-to-back Gen 4 TS1 with the *Indication* field set to 2h. The new transmitter shall set the *Start TxFFE* bit in the Tx Status byte of the Gen 4 TxFFE register in the SB Register Space of the adjacent Router/Re-timer and execute the Gen 4 Transmitter flow for TxFFE negotiation as described in Section 4.1.2.5.1.1.2. Since all transmitters are using the same clock source, the new transmitter (Tx1) transmits the Gen 4 Training Sequences with the common SSC modulation. Note that the new receiver does not need to check Start TxFFE bit in its local Gen 4 Partner Tx Status byte before starts the receiver flow. It is not required that a Router write to the Start TxFFE as defined in Section 4.1.2.4 (Step 4a).
8. When the USB4 Port receivers detect a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 01t, the new transmitter shall start transmitting back-to-back TS2 with the *Indication* field set to 4h. The new transmitter shall continue executing the Gen 4 Transmitter flow for TxFFE negotiation as described in Section 4.1.2.5.1.1.2.
9. When the USB4 Port receivers detect a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 02t, the new transmitter (Tx1) shall start transmitting back-to-back TS3 with the *Indication* field set to 5h.
10. When the USB4 Port receivers detect a CL0s_EXIT Ordered Set with the *CL0s Phase* field set to 10t, the new transmitter (Tx1) shall start transmitting back-to-back TS4 with the *Counter* field increasing in value from 0h to Fh. After sending the TS4 with the *Counter* field set to Fh, the new transmitter shall activate its scrambler and pre-coding.
11. The new transmitter shall transmit back-to-back DESKEW.0 Ordered Sets or Data Sets and wait for the existing transmitter (Tx0) to add it to the Link.
12. When Tx1 is transmitting DESKEW.0 Ordered Sets or Data Sets, upon an RS-FEC block start (either the first RS-FEC block start or upon any subsequent RS-FEC block start while Tx1 is transmitting DESKEW.0 Ordered Set or Data Sets), the USB4 Port shall transmit a De-skew Block on the two transmitters (Tx0 and Tx1). The De-skew Block is defined in Section 4.4.4.
13. After the De-skew Block is transmitted, the transition is finished. The USB4 Port shall distribute the Data Sets between the two active transmitters. The USB4 Port shall send each Ordered Set on both active transmitters. The USB4 Port shall set the *Negotiated Link Width* field to indicate a Symmetric Link.
14. If the USB4 Port is a Downstream Facing Port, the Router shall send a Notification Packet with Event Code = ASYM_LINK to the Connection Manager (see Section 6.5).

If it takes longer than tTrainingAbort1 time from receiving the UNBOND Ordered Set to transmitting the De-skew Block, a USB4 Port shall initiate a disconnect by driving SBTx to logical low state for tDisconnectTx time.

4.2.3 Logical Layer Link State

The Transport Layer sees a Link in one of three states: Active, Low Power, or Inactive. Adapter states are mapped into Transport Layer Link States as follows:

- For a Single-Lane Link, the Link is in Active state when its Lane 0 Adapter is in CL0 state.
- For a Gen 2 or Gen 3 Two Single-Lane Link, the Link is in Active state when its Lane 0 Adapter is in CL0 state. This is a transient Link configuration that occurs between successful completion of Lane Initialization and successful completion Lane Bonding.

- For a Gen 2 or Gen 3 Aggregated Link, the Link is in Active state after its Lanes are successfully bonded, both Adapters transition from either the Lane Bonding State or Training State to CL0 state, and the Adapters stop transmitting TS2 Ordered Sets.
- For Gen 4 Aggregated Link, the Link is in Active state when its Lane 0 Adapter is in CL0 state.
- A Link is in Low Power state when its Adapters are in CL2, CL1, or CL0s states.
- A Link is otherwise in Inactive state.

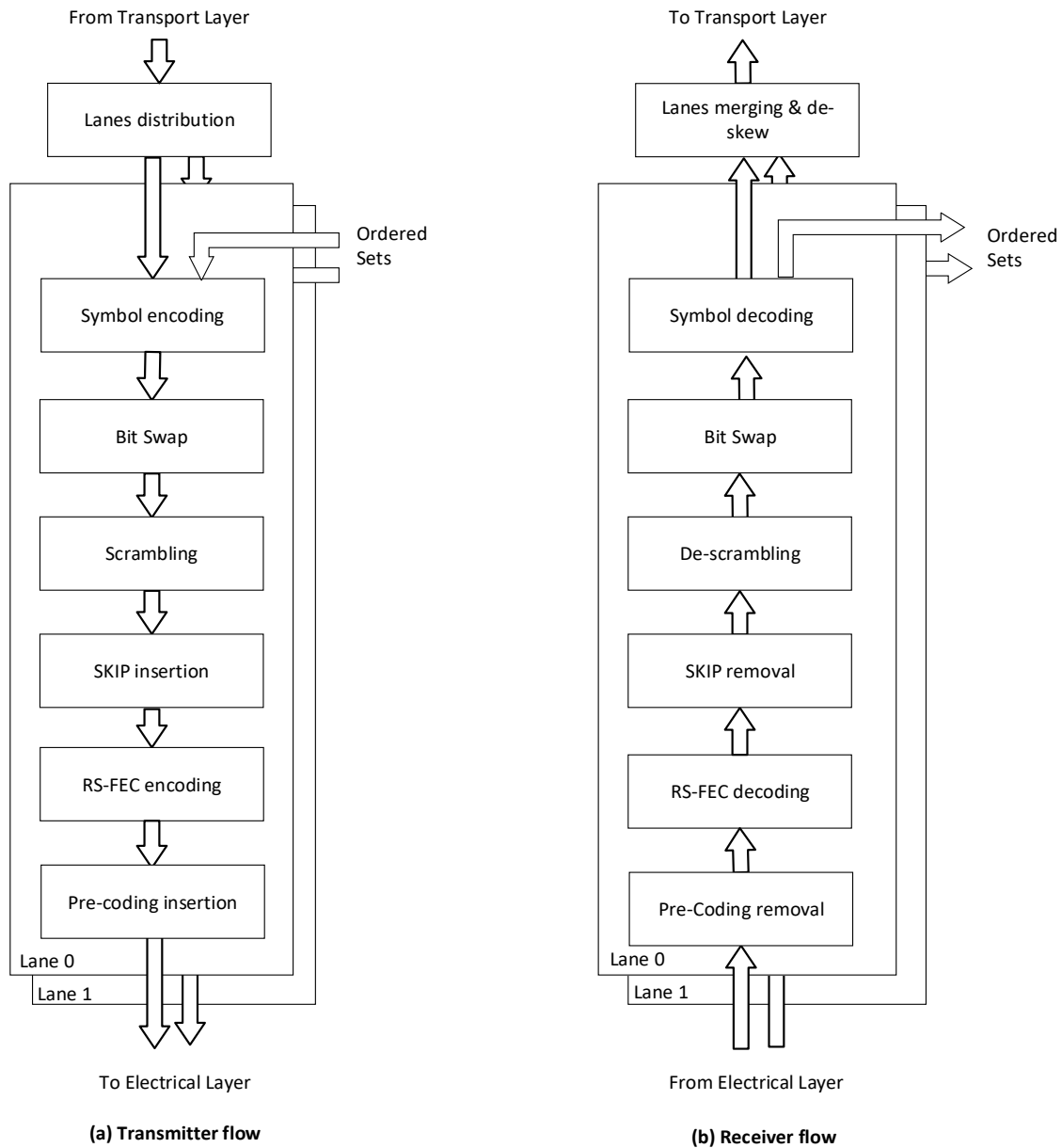
4.3 USB4 Link Encoding

The USB4 Link is responsible for Transport Layer Packet flow through the Logical Layer. The data encoding scheme depends on the Link speed. When the Link is Gen 2 or Gen 3 speed, the data encoding is described in Section 4.3.1. When the Link is Gen 4 speed, the data encoding is described in Section 4.3.2.

4.3.1 Gen 2 and Gen 3 Link Encoding

Figure 4-18 illustrates the logical flow of Transport Layer Packets (received from the Transport Layer) and Ordered Sets (generated by the Logical Layer) through the Logical Layer for a Gen 2 or Gen 3 Link. Actual implementations may differ as long as the logical order is maintained.

Note: The interface between the Transport Layer and the Logical Layer is a byte streaming interface. The Logical Layer is not aware of Tunneled Packets.

Figure 4-18. Packet Flow in the Logical Layer (Gen 2 and Gen 3)

The following steps are taken at the transmitter:

1. Lane Distribution – In a Symmetric Link, outgoing Transport Layer Packets are distributed among the Lanes. See Section 4.3.1.1 for more detail.
- Note: Following Lane distribution, both Lanes of a Symmetric Link go through the same stages. For example, Ordered Sets are inserted to both Lanes at the same time (within the transmit skew inaccuracy).*
2. Ordered Sets – Ordered Sets are inserted into the data flow, used for Logical Layer control purposes. See Section 4.3.1.3 for more detail.
 3. Symbol encoding – If RS_FEC encoding is off, bytes received from the Transport Layer shall be encoded with either 64b/66b encoding (Gen 2) or 128b/132b encoding (Gen 3). See Section 4.3.1.2 for more detail.
 4. Bit Swap – Contents of Ordered Sets and Transport Layer Symbols are rearranged to the order of transmission on the wire. See Section 4.3.1.4.

5. Scrambling – The stream of symbols is scrambled as defined in Section 4.3.1.5.
6. SKIP insertion – an optional stage to insert SKIP Ordered Sets (see Section 4.4.3).
7. RS-FEC – If on, Reed-Solomon encoding is performed per Section 4.3.1.6.
8. Pre-Coding – Performed per Section 4.3.1.6.2.

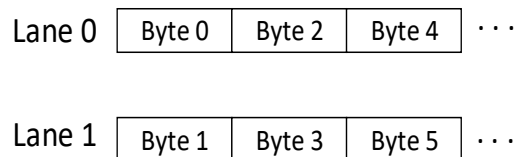
The following steps are taken at the receiver:

1. Pre-Coding removal is performed per Section 4.3.1.6.2.
2. RS-FEC – If on, Reed-Solomon decoding is performed per Section 4.3.1.6.
3. SKIP removal – SKIP Ordered Sets (if present) are removed.
4. De-scrambling – The stream of symbols is de-scrambled as defined in Section 4.3.1.5.
5. Bit Swap – Contents of Symbols are rearranged to eliminate the bit swap done by the transmitter.
6. Symbol decoding – Symbols are converted back into Transport Layer bytes.
7. Ordered Sets – any Ordered Sets are extracted from the stream of Symbols.
8. Lane Merging and de-skew – If a USB4 Link consists of more than one Lane, then the byte streams from the different Lanes are de-skewed and combined into a single byte stream per Section 4.4.4.

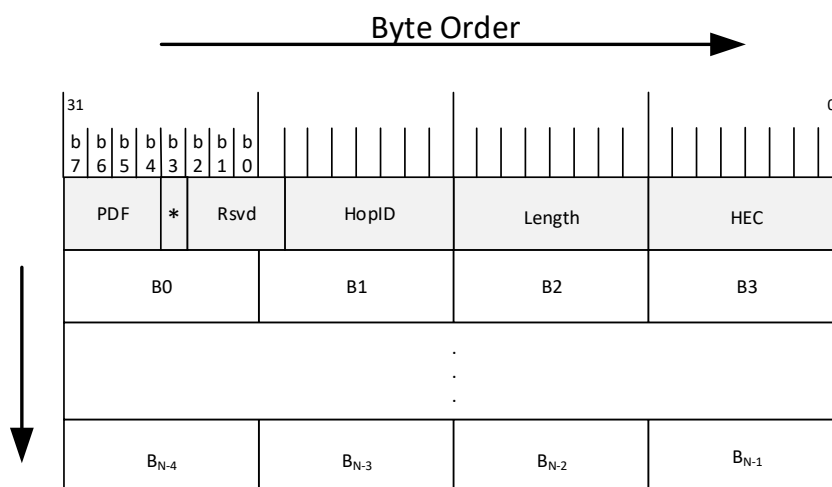
4.3.1.1 Lane Distribution

If a USB4 Link operates as a Symmetric Link, then distribution of Transport Layer bytes among the Lanes shall alternate as depicted in Figure 4-19.

Figure 4-19. Byte Transmission Order on Lanes



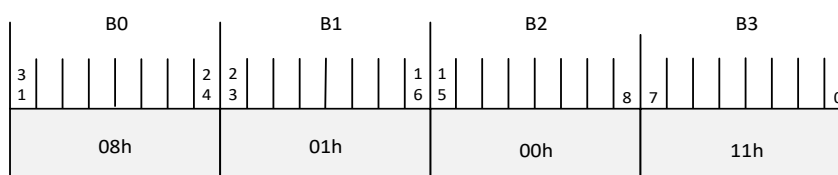
The bytes of a Transport Layer Packet are delivered to the Logical Layer as shown in Figure 4-20.

Figure 4-20. Byte Ordering of Transport Layer Packets to the Logical Layer

Bytes are sent from B0 (first) to B_{N-1} (last)

* SupplD

The bytes of an Idle Packet are delivered to the Logical Layer as shown in Figure 4-21.

Figure 4-21. Byte Ordering of Idle Packets to the Logical Layer

4.3.1.2 Symbol Encoding

The Logical Layer carries two types of payload traffic: Transport Layer Packets (which are received as a byte stream from the Transport Layer), and Ordered Sets (which are added by the Logical Layer and serve Physical Layer control tasks). The format for Symbol encoding depends on whether RS-FEC is on or off.

4.3.1.2.1 Symbol Encoding of Transport Layer Bytes

Transport Layer bytes are grouped into Symbols. When RS-FEC is off, Transport Layer Packets are encoded using either 64b/66b encoding (for Gen 2 speed traffic) or 128b/132b encoding (for Gen 3 speed traffic).

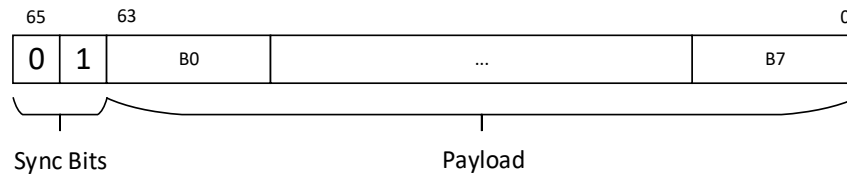
For 64b/66b encoding, a Data Symbol is made of 64 bits of Transport Layer bytes and 2 bits to identify the Symbol type (Transport Layer bytes vs. Ordered Set), called Sync Bits. Figure 4-22(a) depicts the encoding of a Data Symbol for 64b/66b.

For 128b/132b encoding, a Data Symbol is made of 128 bits of Transport Layer bytes and 4 bits to identify the Symbol type, called Sync Bits. Figure 4-22(b) depicts the encoding of a Data Symbol for 128b/132b.

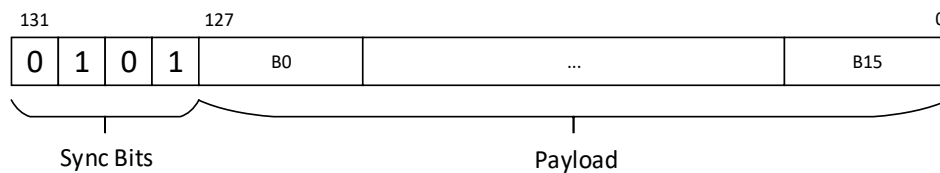
Symbol encoding is done on each Lane separately. A Symbol may contain either Transport Layer bytes or Ordered Set, but shall not contain both.

Note: The Transport Layer feeds the Logical Layer with a constant stream of bytes (referred to as “Transport Layer Bytes”). A Transport Layer sends Idle Packets when it does not have any other Transport Layer Packets to feed the Logical Layer, ensuring that there are always Transport Layer bytes to pack in to a Data Symbol.

Figure 4-22. Symbol Encoding of Data Symbols



(a) Data Symbol structure in 64b/66b encoding



(b) Data Symbol structure in 128b/132b encoding

Note: B0 in the Data Symbol Payload is the first from the Transport Layer

An invalid Sync bit value in a received Symbol generates an Alignment Lock Error (ALE) (see Section 4.4.2).

When RS-FEC is on, the basic transmission unit is a block. See Section 4.3.1.6 for details.

4.3.1.3 Ordered Sets

This section defines the structure of Ordered Sets with the exception of SLOS1, SLOS2, CL_WAKE1.X, and CL_WAKE2.X Ordered Sets.

Ordered Sets are used to perform Physical Layer control tasks. Ordered Sets may be transmitted in the middle of a Transport Layer Packet. An Ordered Set shall have the structure depicted in Table 4-54.

Table 4-54. Ordered Set Structure

Bits	Value	Description
63:10	Various	Ordered Set contents, specific to each Ordered Set
9:0	00 1111 0010b (Scrambled) or 11 0000 1101b (Not scrambled)	SCR – indicates whether the Ordered Set contents are scrambled.

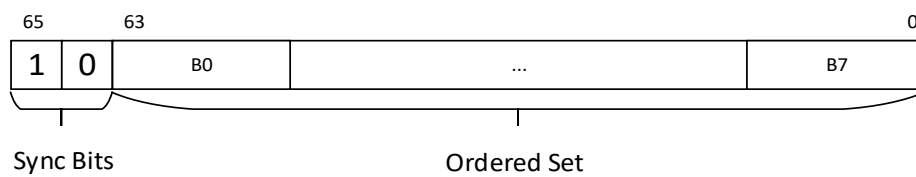
When RS-FEC is off, Ordered Sets are encoded using 64b/66b encoding in Gen 2 mode and 128b/132b encoding in Gen 3 mode.

For 64b/66b encoding, an Ordered Set Symbol shall contain a single copy of the Ordered Set and 2 Sync Bits. Figure 4-23(a) depicts the Symbol encoding of an Ordered Set Symbol for 64/66b encoding.

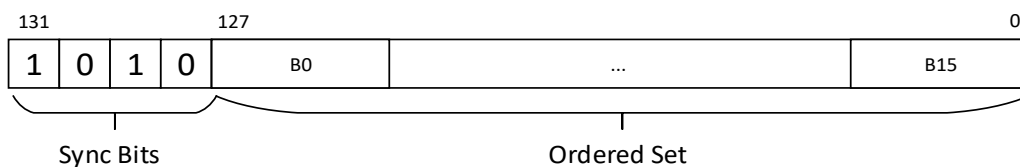
For 128b/132b encoding, an Ordered Set Symbol shall contain two copies of the Ordered Set (i.e. 64 bits followed by a second copy of the same 64 bits) and 4 Sync Bits. Figure 4-23(b) depicts the Symbol encoding of an Ordered Set Symbol for 128/132b encoding.

Note: Receiving two copies of an Ordered Set in an Ordered Set Symbol, is the equivalent of receiving two identical Ordered Sets.

Figure 4-23. Symbol Encoding of Ordered Set Symbols



(a) Ordered Set Symbol structure in 64b/66b encoding



(b) Ordered Set Symbol structure in 128b/132b encoding



IMPLEMENTATION NOTE

When operating with 128b/132b encoding, a receiver can identify an Ordered Set by either the first copy of the Ordered Set, the second copy of the Ordered Set, or both.

For RS-FEC encoding, see Section 4.3.1.6 for the structure of Ordered Sets.

Table 4-55 lists the Gen 2/3 Ordered Sets and reference for more details.

Table 4-55. Gen 2/3 Ordered Sets

Ordered Set	Reference
SLOS1, SLOS2	4.2.1.3.4.1
TS1, TS2	4.2.1.3.4.2
CL_WAKE1.X, CL_WAKE2.X	4.2.1.6.1.1.1
TSNOS	4.3.1.3.1
DESKEW	4.4.4
CL1_REQ, CL2_REQ, CL0s_ACK, CL1_ACK, CL2_ACK, CL_NACK, CL_OFF	4.2.1.6.1.1

4.3.1.3.1 Time Sync Notification Ordered Set (TSNOS)

When a Router receives a Time Sync Notification Ordered Set (TSNOS), it shall generate a time stamp as described in Section 7.2. The Time Sync Notification Ordered Set shall have the structure in Table 4-56.

Table 4-56-55. TSN Ordered Set

Bits	Value	Description
63:10	11 1001 0011 1001 0011 1001 0011 1001 0011 1001 0011 1001 0001 1100b	Contents, specific to the Ordered Set.
9:0	11 0000 1101b	SCR – Shall be set to this value to indicate that the Ordered Set contents are not scrambled.

4.3.1.4 Bit Swap

Bit Swap is the process by which bits from the Transport Layer and the Logical Layer are rearranged into the order in which they are transmitted on the wire.

Bit Swap of Transport Layer bytes and of Ordered Sets shall be performed prior to scrambling so that bytes and bits are delivered to the scrambler in the order that they are transmitted on the wire.

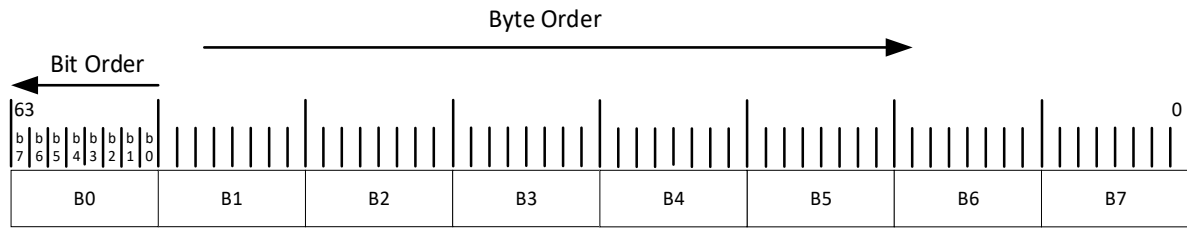
4.3.1.4.1 Sync Bits

If RS-FEC is off, all Symbols shall be transmitted Sync Bits first. Sync Bits shall be sent in the order of most significant bit (i.e. bit 65 for 64b/66b encoding or bit 131 for 128b/132b encoding) to least significant bit (i.e. bit 64 for 64b/66b encoding or bit 128 for 128b/132b encoding). Transport Layer bytes or Ordered Sets shall be transmitted after the Sync Bits.

If RS-FEC is on, the order of transmission of Sync Bits is defined in Section 4.3.1.6.

4.3.1.4.2 Data Symbol Payload

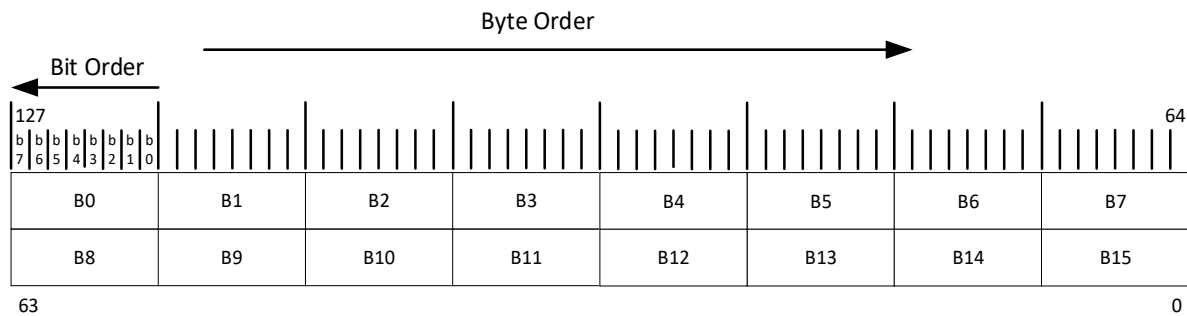
The payload within a Data Symbol shall be transmitted from left to right as depicted in Figure 4-24. Within each byte of payload, individual bits shall be transmitted from bit 0 to bit 7.

Figure 4-24. Bit and Byte Ordering on the Wire – Data Symbol Payload

Bytes are sent from B0 (first) to B7 (last)

Bits within each Byte are sent b0 (first) to b7 (last)

For example, the order of transmission is: bit 56, bit 57, ..., bit 63, bit 48, bit 49, ..., bit 55, ...

(a) Data Symbol Payload transmission order (Gen 2)

Bytes are sent from B0 (first) to B15 (last)

Bits within each Byte are sent b0 (first) to b7 (last)

For example, the order of transmission is: bit 120, bit 121, ..., bit 127, bit 112, bit 113, ..., bit 119, ...

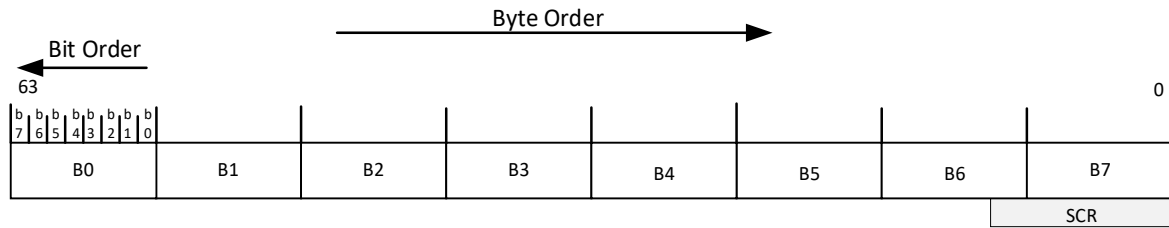
(b) Data Symbol Payload transmission order (Gen 3)

4.3.1.4.3 Ordered Set Symbol Payload

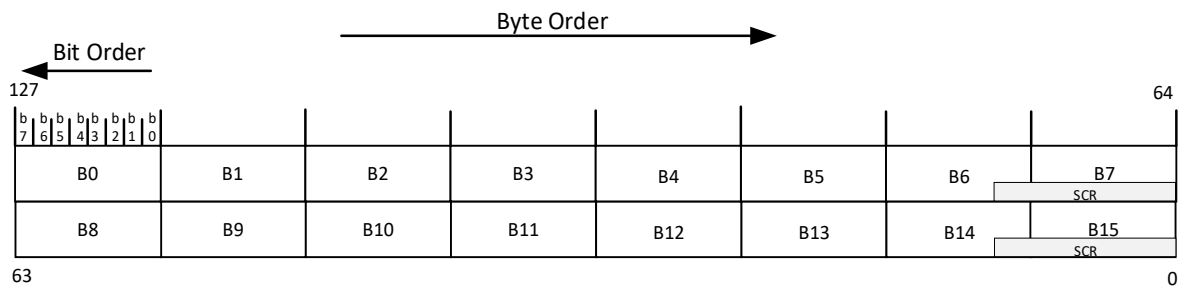
When an Ordered Set is 64 bits long, it is transmitted in one Ordered Set Symbol payload.

When an Ordered Set is longer than 64 bits (i.e. SLOS, CL_WAKE1.X, CL_WAKE2.X), it cannot fit into the payload of one Symbol, and shall be divided into multiple Symbol payloads. The Ordered Set shall be transmitted in increasing Symbols, starting with Symbol 0.

Within a Symbol payload, the bytes in an Ordered Set shall be transmitted from left to right as depicted in Figure 4-25. Within each byte, individual bits shall be transmitted from bit 0 to bit 7.

Figure 4-25. Bit and Byte Ordering on the Wire – Ordered Set Symbol Payload

Bytes are sent from B0 (first) to B7 (last)
Bits within each Byte are sent b0 (first) to b7 (last)

(a) Ordered Set Symbol payload transmission order (Gen 2)

Bytes are sent from B0 (first) to B15 (last)
Bits within each Byte are sent b0 (first) to b7 (last)

(b) Ordered Set Symbol payload transmission order (Gen 3)

4.3.1.5 Scrambling

The Logical Layer performs scrambling of transmit traffic and de-scrambling of receive traffic. Scrambling shall be performed according to the rules in Table 4-57.

Table 4-57 4-56. Scrambling Rules

	Scramble?	Advanced LFSR?
Data Symbols		
Sync Bits	No	No
Transport Layer bytes	Yes	Yes
Ordered Set Symbols		
Sync Bits	No	No
Contents	Determined by SCR value	When scrambled
SCR	No	When contents are scrambled

The following scrambling and de-scrambling rules shall be followed for all transmitted and received traffic:

- Scrambling and de-scrambling are performed by passing the encoded bits through an Additive LFSR with a polynomial of $G(X) = X^{23} + X^{21} + X^{16} + X^8 + X^5 + X^2 + 1$.
- The most significant output bit of the LFSR is XORed with the data stream on a per-bit basis. The data stream is scrambled in the order that it is sent on wire.

- The scrambler shall load a new seed on the following transitions:
 1. Transition from LOCK2 sub-state to TS1 sub-state in the Training state.
 - Initial value is 1F EEDDh.
 2. On exit from CL0s state, before the Adapter initiating exit transmits the first TS2 Ordered Set in the direction exiting electrical idle.
 - Initial value is 1F EEDDh.
 3. On transition from any state to CL0 when going to a Symmetric Link.
 - When exiting CL0s state, a new seed shall be loaded only in the direction exiting electrical idle.
 - Initial value on the Lane 0 is 1D BFBCCh.
 - Initial value on Lane 1 is 06 07BBh.
 - The per-Lane seeds are used, starting with the first byte after the last de-skew Ordered Set.
- Any single-bit errors in the *SCR* field shall be corrected. If the *SCR* field contains an uncorrectable error, the Logical Layer reports an OSE error as defined in Section 4.4.2.

The following pseudocode example produces N bits of LFSR output, starting with a seed value as defined above.

```
poly = 21 0124h
lfsr = seed
output = 0
for (i=1 to N) {
    msb = lfsr[22]
    lfsr = lfsr << 1
    lfsr[23] = 0
    if (msb == 1) then lfsr = (lfsr XOR poly)
    lfsr = lfsr + msb
    output = (output << 1) + msb
}
```



IMPLEMENTATION NOTE

During Training state or during exit from CL0s state, a receiver can identify the exact time to load a new scrambler seed by detecting an Ordered Set with the SCR (bits [9:0]) equal to 00 1111 0010b (scrambled).

See Appendix A.4 for examples of scrambling Data Symbols and Ordered Set Symbols.

4.3.1.6 RS-FEC

The Logical Layer employs a Reed-Solomon forward error-correction code (RS-FEC). An Adapter shall support RS-FEC at all speeds. An RS(198,194) code over GF(2⁸) is used:

- The primitive polynomial over GF(2⁸) is $p(x) = X^8 + X^4 + X^3 + X^2 + 1$
- The generating polynomial is $g(x) = X^4 + 15X^3 + 54X^2 + 120X + 64$

Each block of 194 bytes shall be generated in the following manner (see Figure 4-26):

- Transport Layer bytes and Ordered Sets are grouped into 16-byte (128 bit) Symbol payloads. Each Symbol payload may contain either one or more Ordered Set or Transport Layer bytes, but shall not contain both.

- When operating at Gen 2 speed, the 16-byte Ordered Set Symbol payload shall contain:
 - For a SLOS Ordered Set or a CL_WAKE2.X Ordered Set, 128 bits of the Ordered Set.
 - For all other Ordered Sets, two 64-bit Ordered Sets. When only one Ordered Set needs to be sent, the second Ordered Set shall be a SKIP Ordered Set. When a DESKEW Ordered Set is placed first in a 16-byte payload, the second Ordered Set shall be SKIP. See Section 4.4.3 for the structure of a SKIP Ordered Set.

Note: CL_WAKE1.X Ordered Sets are not RS-FEC encoded. See Section 4.2.1.6.1.1 for more information.

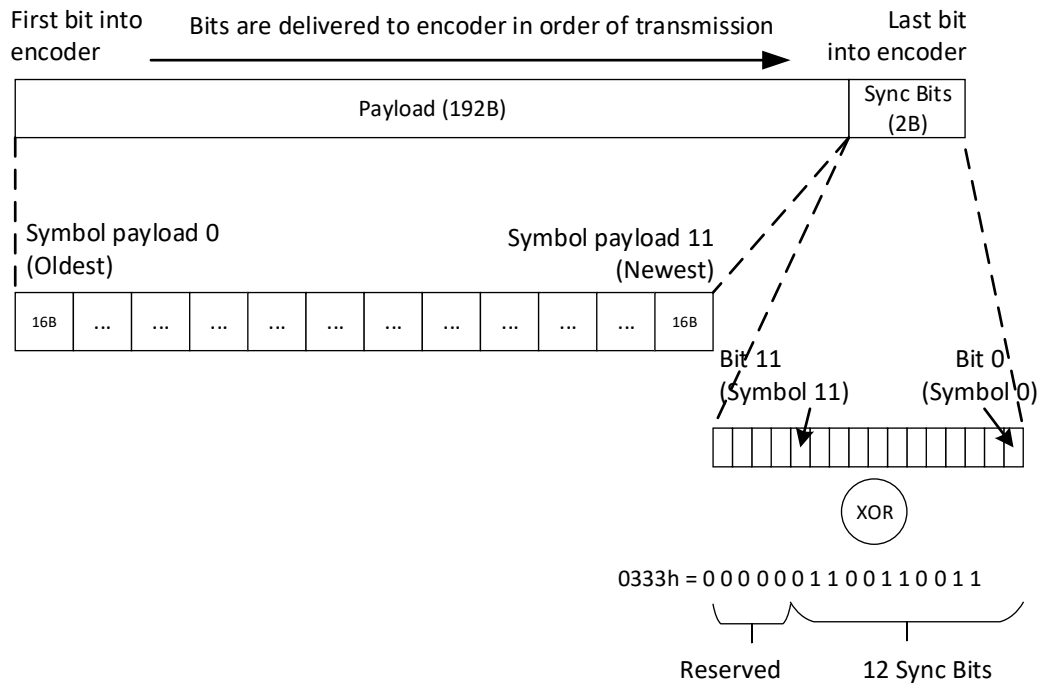
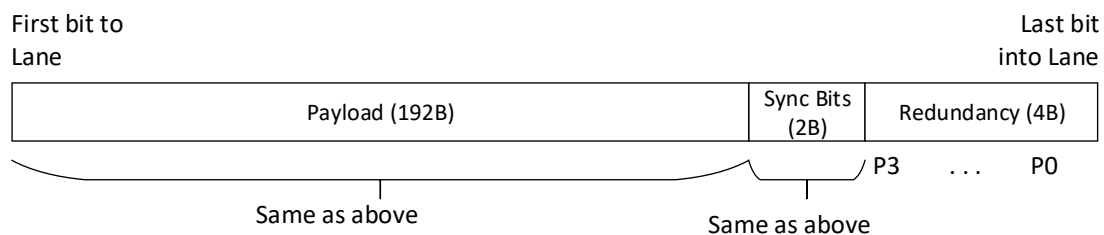
- When operating at Gen 3 speed, the 16-byte Ordered Set Symbol payload shall contain:
 - For a SLOS Ordered Set or a CL_WAKE2.X Ordered Set, 128 bits of the Ordered Set.
 - For all other Ordered Sets, two copies of the Ordered Set (i.e. 64 bits followed by a second copy of the same 64 bits).

Note: CL_WAKE1.X Ordered Sets are not RS-FEC encoded. See Section 4.2.1.6.1.1 for more information.

- The RS-FEC encoder is fed with twelve 16-byte Symbol payloads plus 2 bytes of Sync Bits. Each Symbol is allocated a single Sync Bit, indicating whether it contains Transport Layer bytes (Sync Bit = 0b) or Ordered Set (Sync Bit = 1b).
 - The 2 bytes of Sync Bits contain 12 active bits (one per 16-byte Symbol) and 4 reserved bits.
 - Sync Bits shall be delivered to the encoder in order that they are sent to the wire, from bit 15 to bit 0. The active Sync Bits reside in bits[11:0] of the Word. The Sync Bit corresponding to the oldest 16-byte Symbol (Symbol payload 0 in Figure 4-26) resides in bit 0 of the Sync Bits.
 - The 12 active bits are XORed with 333h before being fed to the RS-FEC encoder. The XORed value is the value seen on the wire.
- The RS-FEC encoder generates 4 bytes of redundancy bits (P3 to P0). P3 is the first byte to be sent on the wire and P0 is the last. Within each byte, bits are sent in descending order where bit 7 is sent first and bit 0 is sent last.

The RS-FEC decoder shall correct a received block with up to two 1-byte errors anywhere in the block.

An error in a received block that is detectable and uncorrectable shall cause an RDE error (see Section 4.4.2).

Figure 4-26. RS-FEC Data Structures**(a) Structure of RS-FEC input block****(b) Structure of RS-FEC output block**

Appendix A contains examples of RS-FEC blocks as these appear on the wire.

4.3.1.6.1 RS-FEC Activation and Deactivation

If RS-FEC is enabled during Phase 3 of Lane Initialization, then an Adapter shall activate RS-FEC encoding in the following cases:

- In Training state (see Section 4.2.1.3), immediately following the last transmitted SLOS2 and before sending the first TS1 Ordered Set.
- During exit from CL0s state (see Section 4.2.1.6.4), immediately before sending the first TS2 Ordered Set.

A START_RS_FEC bit sequence shall be sent prior to activating RS-FEC encoding on the Lane.

- The bit sequence is per Table 4-58.
- The bit sequence shall not be scrambled and shall not advance the scrambler LFSR.
- The START_RS_FEC bit sequence shall be sent with bit[31] first on the wire.

- During exit from CL0s state, the START_RS_FEC bit sequence shall only be sent in the direction exiting electrical idle.
- The bit following the START_RS_FEC bit sequence shall be the first bit to be RS-FEC encoded.

Table 4-584-57. START_RS_FEC Bit Sequence

Bits	Value	Description
31:0	0F0F 0F0Fh	Unique sequence indicating start of RS-FEC

If RS-FEC encoding is activated, a USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases:

- When transitioning to Training.LOCK1 sub-state, after transmitting n SLOS1 Symbols in LOCK1 sub-state with RS-FEC on, where $32 \leq n \leq 64$ in Gen 2 and $16 \leq n \leq 32$ in Gen 3.
- Entry to Training.LOCK2 sub-state.
- Entry to Disabled state.
- Entry to CLd state.
- Entry to CL0s state, in the direction entering Low Power state.
- Entry to CL2 or CL1 states.

Note: RS-FEC decoding of received bits may be turned off on entry to Training state.

4.3.1.6.2 Pre-Coding

If Pre-Coding is on, then before each bit is sent on the wire, it shall be XOR'ed with the bit sent before it, using the value of the bit after it was coded. The first bit is XOR'ed with 0b.

For example, if the bit sequence to be sent starts with 1,0,1,1,0,... then the sequence after Pre-Coding is 1,1,0,1,1,...

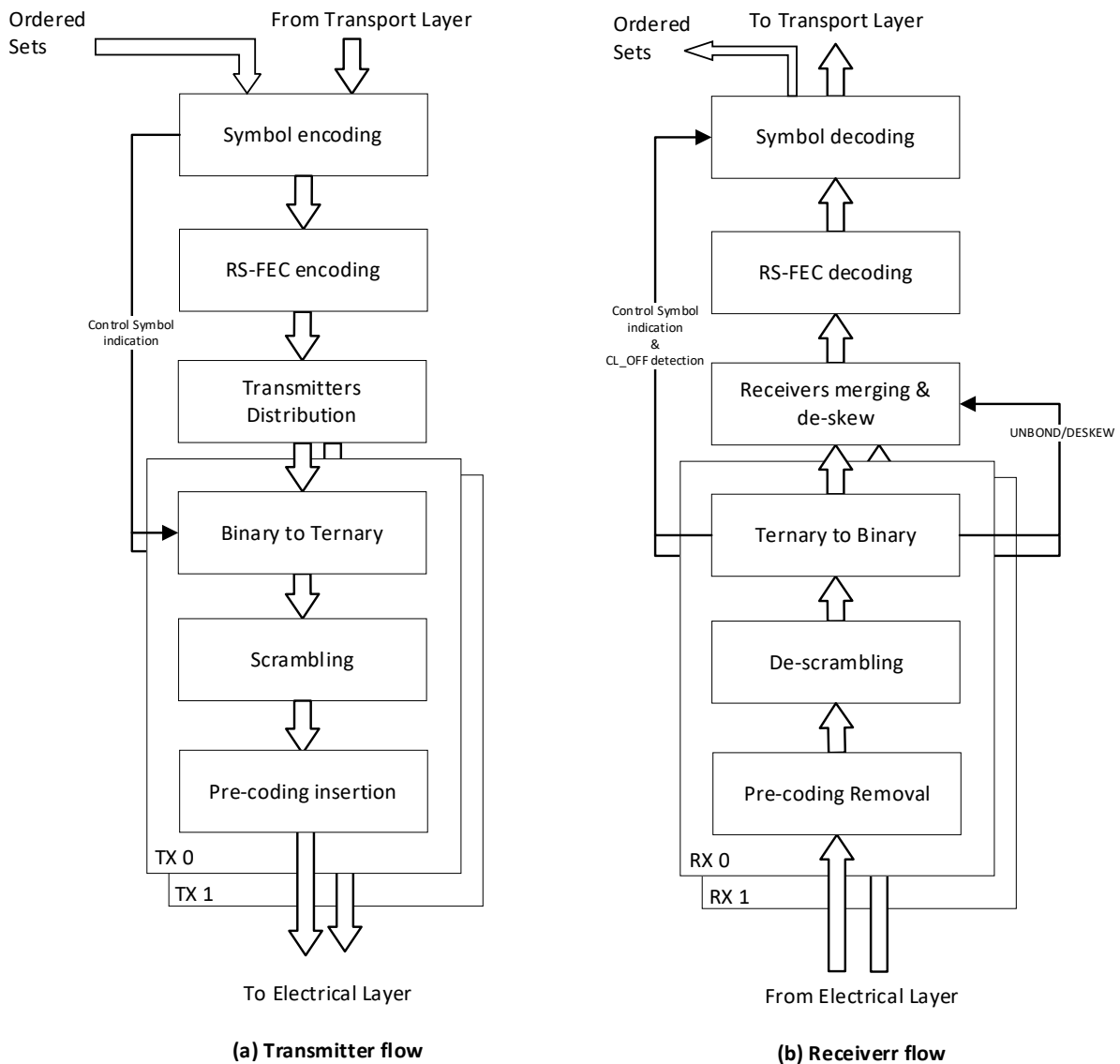
Pre-Coding shall be turned on with the first bit that is RS_FEC encoded.

Pre-Coding shall be turned off with the first bit that is not RS_FEC encoded.

4.3.2 Gen 4 Link Encoding

Figure 4-27 illustrates the logical flow of Transport Layer Packets (received from the Transport Layer) and Ordered Sets (generated by the Logical Layer) through the Logical Layer for a Symmetric Gen 4 Link. Actual implementations may differ as long as the logical order is maintained.

Note: The interface between the Transport Layer and the Logical Layer is a bit streaming interface. The Logical Layer is not aware of Tunneled Packets.

Figure 4-27. Data Flow in the Logical Layer for a Gen 4 Symmetric Link

The following steps are taken in the transmitter:

1. **Ordered Sets** – Gen 4 Ordered Sets are inserted into the data flow, used for Logical Layer control purposes. See Section 4.3.2.1 for more details.
2. **Symbol Encoding** – The bit stream from the Transport Layer is divided to 11 bits Symbols. Control Symbols are marked with a special indication to be translated differently to Ternary. See Section 4.3.2.2 for more details.
3. **RS-FEC Encoding** – Reed-Solomon encoding is performed per Section 4.3.2.3.
4. **Transmitters Distribution** – In a Link with more than one transmitter, RS-FEC block Symbols are distributed among the transmitters. See Section 4.3.2.4 for more details.
5. **Binary to Ternary** – Converting the Binary Symbols to Ternary Symbols. See Section 4.3.2.5 for more details.
6. **Scrambling** – The stream of symbols is scrambled as defined in Section 4.3.2.7.
7. **Pre-Coding** – Performed per Section 4.3.2.8.

The following steps are taken at the receiver:

1. **Pre-Coding Removal** – Performed per Section 4.3.2.8.
2. **De-scrambling** – The stream of symbols is de-scrambled as defined in Section 4.3.2.7.
3. **Ternary to Binary** – Converting the Ternary Symbols to Binary Symbols and detecting Control Symbols as defined in Section 4.3.2.5.
4. **Lane Merging and De-skew** – If a USB4 Link consists of more than one receiver, then the streams from the different receivers are de-skewed and combined into a single stream per Section 4.3.2.4.
5. **RS-FEC** – Reed-Solomon decoding is performed per Section 4.3.2.3.
6. **Symbol Decoding** – Symbols are converted back into Transport Layer bits and Ordered Sets.



IMPLEMENTATION NOTE

Due to the high BER in PAM3, the receiver may receive up to 12 error Symbols in an RS-FEC block. A receiver should be able to decode correctly the received Control or Data Symbols. Control Symbols and Ordered Sets should not be forwarded to the Transport Layer.

4.3.2.1 Gen 4 Ordered Sets in the Binary Space

Gen 4 Ordered Sets are inserted to the bit stream in the Binary space since they are part of the RS-FEC block. This section defines the structure of Gen 4 Ordered Sets in the binary space except for Gen 4 TSNOS. The Gen 4 TSNOS is defined in Section 4.3.2.6.5.

Gen 4 Ordered Sets may be transmitted in the middle of a Transport Layer Packet. Gen 4 Ordered Sets shall be transmitted as the first Symbols in an RS-FEC block, the number of Ordered Sets depends on the Ordered Set being sent. A Gen 4 Ordered Set shall have the structure depicted in Figure 4-28.

Figure 4-28. Structure of Gen 4 Ordered Set

Control Symbol	Control Symbol	Control Symbol	Control Symbol
----------------	----------------	----------------	----------------

4.3.2.2 Symbol Encoding

The Logical Layer carries two types of payload traffic: Transport Layer Packets (which are received as a bit stream from the Transport Layer), and Gen 4 Ordered Sets (which are added by the Logical Layer and serve Physical Layer control tasks).

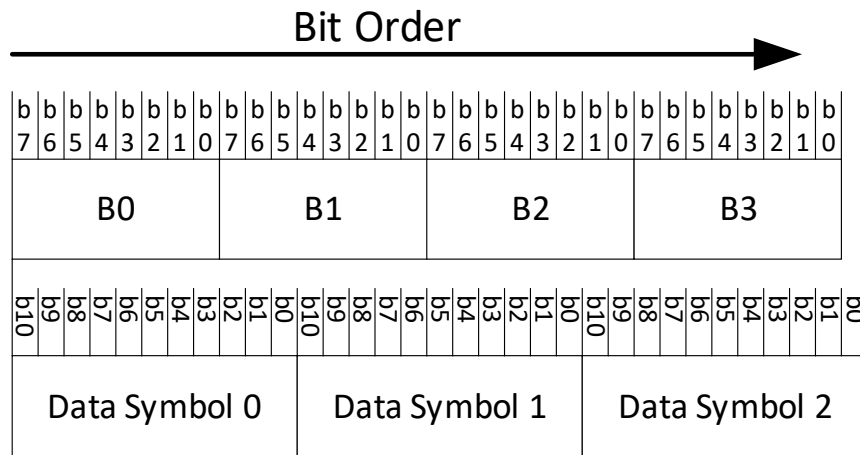
4.3.2.2.1 Symbol Encoding of Transport Layer Bits

Transport Layer bits shall be grouped into Binary Data Symbols. Each Data Symbol consist of 11 bits. Each consecutive four Data Symbols construct a Data Set. A Data Set contains only Data Symbols.

Note: When the transmitters are in CL0, the Transport Layer feeds the Logical Layer with a constant stream of bits (referred to as “Transport Layer Bits”). A Transport Layer sends Idle Packets when it does not have any other Transport Layer Packets to feed the Logical Layer, ensuring that there are always Transport Layer bits to pack into a Data Symbol.

Figure 4-29 shows an example of grouping 4 Bytes from the Transport Layer into Data Symbols in the Logical Layer. In this example, bit 7 from Byte 0 is mapped to bit 10 in Symbol 0 and bit 5 from Byte 1 is mapped to bit 0 in Symbol 0. The Byte ordering in a Transport Layer Packet is the same as for Gen 2 and Gen 3 (see Figure 4-20).

Figure 4-29. Example of Transport Layer Bit Stream Symbol Encoding



4.3.2.2.2 Symbol Encoding of Ordered Sets

When an Ordered Set is inserted by the Logical Layer, it stops the stream of Transport Layer bits to the Logical Layer on the RS-FEC block boundary. The Ordered Sets are constructed from 11-bit Binary Control Symbols. Appendix F describes the value for each Control Symbol in the Binary space. Each Control Symbol shall be marked as such. This is done so it can be translated to Ternary in a different method than Data Symbols (see Section 4.3.2.5, step 4). The method of marking the Control Symbols is implementation specific.

4.3.2.3 RS-FEC Encoding

Gen 4 Forward-Error-Correction (FEC) is based on Reed-Solomon RS(504,480) over GF(2¹¹), with 12 correctable errors per block. The code is applied before distribution to the transmitter and sent over all active transmitter to reduce latency.

The following GF parameters and encoder generator are used:

1. Primitive Polynomial:

$$p(x) = x^{11} + x^2 + 1 \text{ over } GF(2^{11})$$

2. The RS generator polynomial (t=12):

$$g(x) = \prod_{k=0}^{2t-1} (x - \alpha^k) = x^{2t} + g_{(2t-1)}x^{(2t-1)} + \dots + g_1x + g_0$$

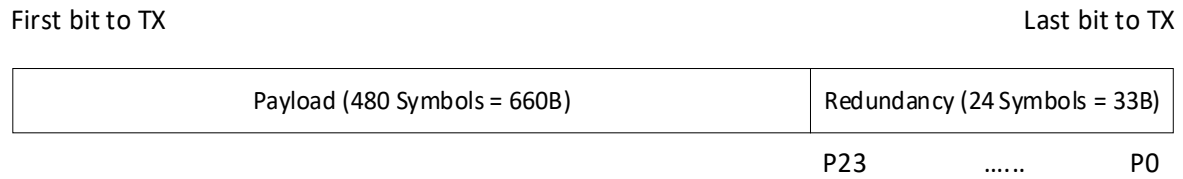
Where the polynomial coefficients are

$$\underline{g} = [1, 1984, 701, 1575, 1495, 996, 1879, 1362, 979, 1524, 640, 897, 645, 1812, 1605, 1096, 1173, 173, 1891, 286, 1498, 457, 1788, 722, 1455]$$

The RS-FEC encoder generates 24 Symbols of redundancy bits (P23 to P0). P23 is the first Symbol to be sent on the wire and P0 is the last.

The Redundancy Symbols are added as the last 24 Symbols in each RS-FEC block as described in Figure 4-30. Each four consecutive Redundancy Symbols define a Redundancy Set.

Figure 4-30. Structure of Gen 4 RS-FEC Block



The RS-FEC decoder shall correct a received block with 12 error Symbols or less anywhere in the block.

An error in a received block that is detectable and uncorrectable shall cause an RDE error (see Section 4.4.2).

Appendix A contains examples of RS-FEC blocks.

4.3.2.3.1 RS-FEC Activation and Deactivation

A USB4 Port shall activate RS-FEC encoding when its Lane Adapters enter CL0 state, starting from the first bit of the De-skew Block. The USB4 Port shall deactivate RS-FEC encoding when either of the following occur:

- The Lane Adapters transition to Disabled or CLd state.
- When sending Gen 4 CL_OFF Ordered Sets during the transition to CL0s TX, CL1, or CL2 state (i.e. any state except CL0s RX) as described in Section 4.2.1.

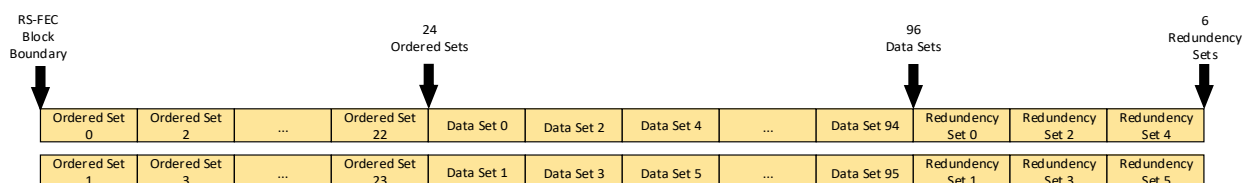
4.3.2.4 Transmitters Distribution

If there is more than 1 active transmitter, Data Symbols, Control Symbols, and Redundancy Symbols are distributed among the active transmitters as follows:

- Each transmitter sends one Set (four consecutive Symbols): a Data Set, Ordered Set or Redundancy Set.
- When Ordered Sets are transmitted, all active transmitters send the same Ordered Set unless specifically mentioned otherwise.
- Data Sets and Redundancy Sets shall be sent starting from the first active transmitter (TX0). Each additional Data/Redundancy Set shall be distributed to the next higher transmitter (modulo the number of active transmitters).
- All active transmitters shall send the same type of Symbols (Data Set/Ordered Set/Redundancy Set) at the same time.

Figure 4-31 shows an example with two transmitters that send 24 Ordered Sets at the beginning of an RS-FEC block and a Data Sets afterwards.

Figure 4-31. Example of Distribution with Two Transmitters



4.3.2.5 Binary to Ternary Conversion

Each Binary Symbol shall be converted to a Ternary Symbol using the following algorithm:

1. Divide the Binary Symbol to groups of bits using Table 4-59.
2. If $A \neq 11b$:
 - a. Convert A to A' using Table 4-60.
 - b. Convert B to B', C to C' and D to D' using Table 4-61.
 - c. Construct the Ternary Symbol using Table 4-62.
3. Else:
 - a. Convert C to C' and D to D' using Table 4-61.
 - b. Depending on the value of B, construct the Ternary Symbol using Table 4-63.
4. If the Symbol is a Control Symbol, replace trits 6:4 in the Ternary Symbol from 210t to 111t.

Table 4-594-58. Binary Symbol Groups

Group	Bits
A	10:9
B	8:6
C	5:3
D	2:0

Table 4-604-59. Conversion of 2 Bits to 1 Trit

Binary Representation	Ternary Representation
00	0
01	1
10	2

Table 4-614-60. Conversion of 3 Bits to 2 Trits

Binary Representation	Ternary Representation
000	00
001	01
010	02
011	10
100	12
101	20
110	21
111	22

Table 4-624-61. Ternary Symbol Groups

Trits	Group
6	A'
5:4	B'
3:2	C'
1:0	D'

Table 4-634-62. Constructing Ternary Symbol when A=11b

B	000	001	010	011	100	101	110	111
6	0t	1t	2t	0t	1t	2t	0t	2t
5:4	C'	C'	C'	C'	C'	C'	11t	11t
3:2	D'	D'	D'	11t	11t	11t	C'	C'
1:0	11t	11t	11t	D'	D'	D'	D'	D'

A receiver shall convert from Ternary to Binary using the same tables. When the receiver detects 111t in trits 6:4 of a Symbol, it shall replace trits 6:4 with 210t.

**IMPLEMENTATION NOTE**

Due to the fact that a Control Symbol is indistinguishable from a Data Symbol after the ternary to binary conversion, the receiver needs to use an implementation specific method to distinguish between Control Symbols and Data Symbols after ternary to binary conversion (e.g. the receiver may mark Control Symbols in the ternary domain and carry that marking alongside the ternary to binary conversion).

Note: When describing binary bits, the digits 0 and 1 are used to describe low and high voltages respectively. When describing ternary trits, the digits 0, 1 and 2 are used to describe low, middle, and high voltages respectively.

**IMPLEMENTATION NOTE**

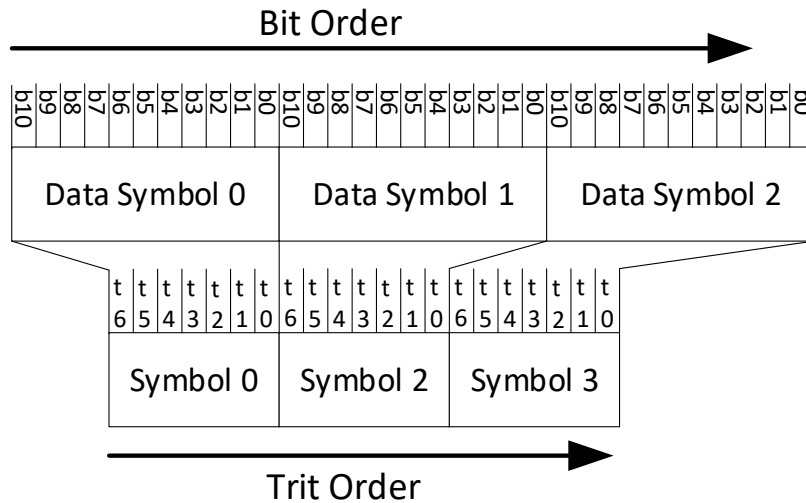
A receiver can use the information from the RS-FEC decoder to decide whether a Symbol is a Control or Data. Control Symbols are either in the first 24 Ordered Sets of an RS-FEC block or they fill the entire RS-FEC block. A receiver can use a majority rule to identify an Ordered Set in a beginning of a RS-FEC block.

The following examples use the tables in this section to convert a binary Symbol to a ternary Symbol and vice versa:

- An 11-bit binary Symbol (10101110110b) is divided into A=10b, B=101b, C=110b and D=110b. Since A≠11b, Table 4-60 is used to convert A to A' and Table 4-61 is used to convert B, C and D to B', C' and D'. A'=2t, B'=20t, C'=21t, D'=21t. The resulting ternary Symbol is 2202121t.
- When detecting a 7-trit ternary Symbol (2102011t), it is divided into A'=2t, B'=10t, C'=20t and D'=11t. Since D'=11t, Table 4-63 is used and, together with A'=2t, the third column is used. A=11b, B=010b, C is an inverse conversion of B', and D is an inverse conversion of C' using Table 4-61, so C=011b, D=101b. The resulting 11-bit binary Symbol is 11010011101b.

The Trits are transmitted on the wire from MST (first) to LST (last) as shown in Figure 4-32.

Figure 4-32. Trit Ordering After Conversion from Binary



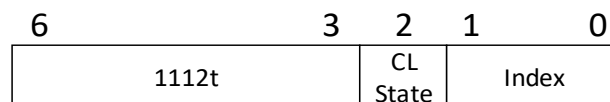
4.3.2.6 Gen 4 Ordered Sets in the Ternary Space

For each Control Symbol in the Gen 4 Ordered Set, the most significant trit shall be sent first on the wire. All Gen 4 Ordered Sets are scrambled. The Ordered Sets in the following sections are described in the Ternary space. The actual Binary Control Symbol values that are used to insert the Ordered Sets are a result of the reverse conversion described in Section 4.3.2.5. Examples are given in Appendix F.

4.3.2.6.1 Gen 4 CL_OFF Ordered Set

A Gen 4 CL_OFF Ordered Set shall consist of four Control Symbols with the structure depicted in Figure 4-33.

Figure 4-33. Structure of Gen 4 CL_OFF Control Symbol



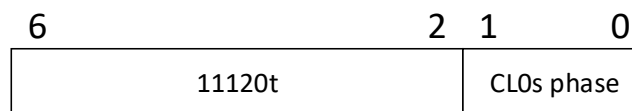
The *CLx State* field shall be set to 1t when entering CL0s with the option to enter CL1. The *CLx State* field shall be set to 2t when entering CL0s with option to enter CL2. A value of 0t in the *CLx State* field is reserved and shall not be used.

The *Index* field indicate which component on the Link (Router/Re-timer) is the target of this Ordered Set in Ternary base.

4.3.2.6.2 Gen 4 CLOs_EXIT Ordered Set

A Gen 4 CL0s_EXIT Ordered Set shall consist of four Control Symbols with the structure depicted in Figure 4-34.

Figure 4-34. Structure of Gen 4 CL0s_EXIT Control Symbol



The *CL0s Phase* field shall be set according to Table 4-64.

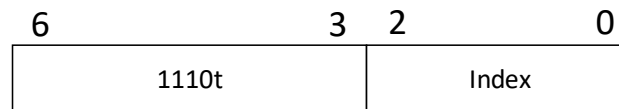
Table 4-64-63. CL0s Phase Coding

Value	Name	Description
00t	<i>AckLFPS</i>	Shall be set when Router detects LFPS and its transmitter is active (CL0s RX).
01t	<i>StartP3</i>	Shall be set when the receiver detects TS1 with Indication 2 in CL0s exit flow.
02t	<i>StartClkSw</i>	Shall be set when the receiver detects TS2 with Indication 4 in CL0s exit flow.
10t	<i>ClkSwAck</i>	Shall be set when the receiver detects TS3 with Indication 5 in CL0s exit flow.
Other	<i>Reserved</i>	Shall not be used by the transmitter and shall be ignored by the receiver.

4.3.2.6.3 Gen 4 DESKEW.X Ordered Set

A Gen 4 DESKEW.X Ordered Set shall consist of four Control Symbols with the structure depicted in Figure 4-35.

Figure 4-35. Structure of Gen 4 DESKEW.X Control Symbol

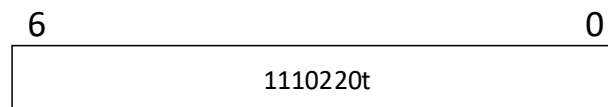


The *Index* field shall be set according to the rules of the De-skew Block described in Section 4.4.4. The X shall be equal to the *Index* field.

4.3.2.6.4 Gen 4 UNBOND Ordered Set

A Gen 4 UNBOND Ordered Set shall consist of four Control Symbols with the structure depicted in Figure 4-36.

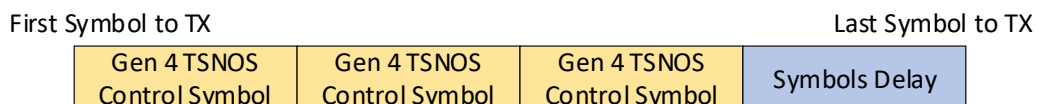
Figure 4-36. Structure of Gen 4 UNBOND Control Symbol



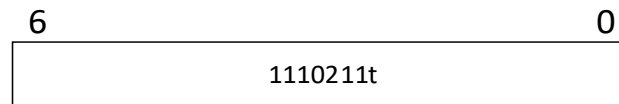
4.3.2.6.5 Gen 4 TSNOS Ordered Set

A Gen 4 Time Synchronization Notification Ordered Set (Gen 4 TSNOS) shall consist of three Control Symbols followed by a *Symbols Delay* Data Symbol as depicted in Figure 4-37.

Figure 4-37. Structure of Gen 4 TSNOS Ordered Set



The Gen 4 TSNOS Control Symbols shall have the structure depicted in Figure 4-38.

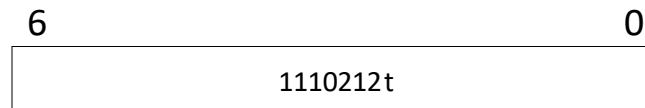
Figure 4-38. Structure of Gen 4 TSNOS Control Symbol

The *Symbols Delay* Data Symbol in the Gen 4 TSNOS shall indicate the Symbol Time that has passed from the Time Stamp Point to the beginning of the RS-FEC block on which the Gen 4 TSNOS is being sent as described in Section 7.2.2.

Note: The Symbols Delay value is added in binary and converted to ternary using Data Symbol method as described in section 4.3.2.5.

4.3.2.6.6 Gen 4 IGNORE Ordered Set

A Gen 4 IGNORE Ordered Set shall consist of four Control Symbols with the structure depicted in Figure 4-39.

Figure 4-39. Structure of Gen 4 IGNORE Control Symbol

A USB4 Port transmits 24 Gen 4 Ordered Sets at the beginning of an RS-FEC block, the rest of the RS-FEC block is undefined.

When a receiver detects a Gen 4 IGNORE Ordered Set, the entire RS-FEC block shall be ignored as follows:

- RS-FEC decoding errors in the RS-FEC block shall not cause the RDE bit to be set to 1b, shall not increase the FEC Errors Statistics Counters, and shall not cause a Notification Packet to be sent.
- The entire RS-FEC block shall be dropped and shall not be forwarded to the Transport Layer.

4.3.2.7 Scrambling

The Logical Layer performs scrambling of transmitted traffic. Scrambling is activated on the first trit after Gen 4 TS4 with *Counter* field set to Fh has finished (see Section 4.4.1.2). Each trit shall be sent to the scrambler in the order it is transmitted on the wire (MST to LST). Scrambling shall be performed by adding (module 3) a pseudo-random ternary sequence to the output of the Binary-to-Ternary conversion. The pseudo-random sequence shall be generated by applying function *F* to the output of a ternary LFSR with 19 taps and a binary LFSR with 11 taps. The *F* operation in the ternary finite field shall keep the PRTS19 ternary symbol unchanged if the corresponding PRBS11 bit is equal to 1b. It shall switch a ternary value of 2t with a ternary value of 0t (and vice-versa) if the corresponding PRBS11 bit is 0b. Table 4-65 describes the behavior of the *F* function. The initial seeds for PRBS11 and PRTS19 for each transmitter are defined in Table 4-66. The seeds are loaded on the transition to CL0 as described in Section 4.2.1.

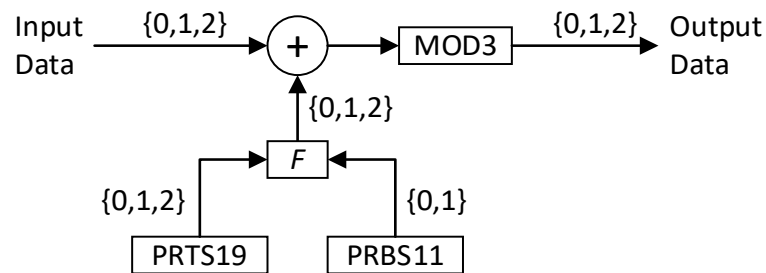
Table 4-654-64. Function F

PRTS19 Value	PRBS11 Value	
	0b	1b
0t	2t	0t

1t	1t	1t
2t	0t	2t

Figure 4-40 describes the operation of the Scrambler.

Figure 4-40. Scrambler Operation



The PRBS11 pattern generator shall be implemented as described in Table 4-66 and Figure 4-41. The PRTS19 pattern generator shall be implemented as described in Table 4-66 and Figure 4-42. Examples for PRBS11 and PRTS19 can be found in Appendix C.

Figure 4-41. PRBS11 Pattern Generator

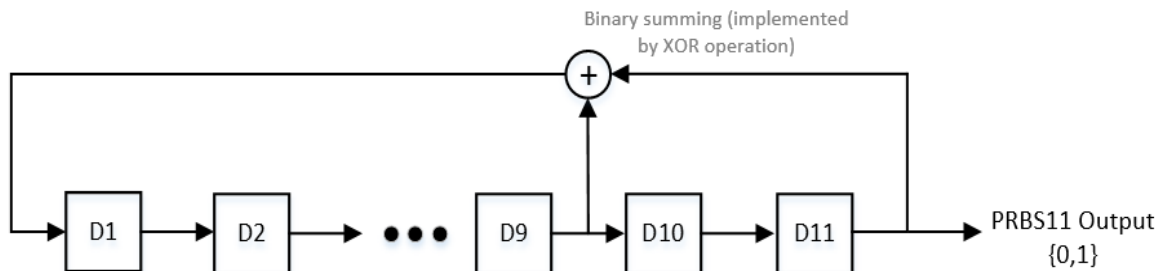
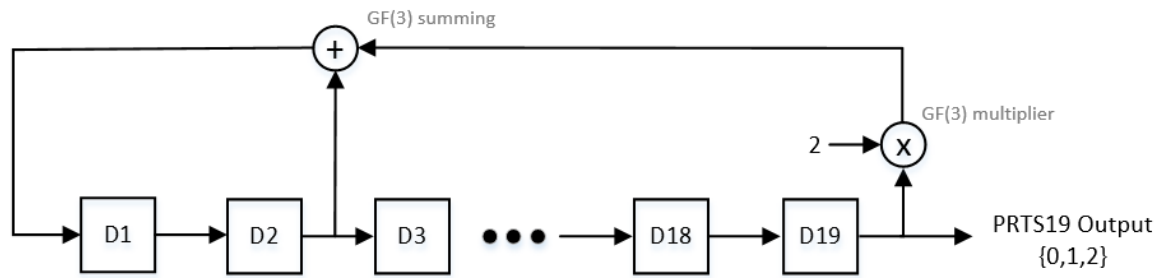


Figure 4-42. PRTS19 Pattern Generator

GF(3) Arithmetics:

+	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

x	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

Table 4-664-65. Seeds for Various Pseudo-Random Sequences

Name	Description	Comments
PRBS11	Pseudo-Random Binary sequence generated with the polynomial: $G(x)=1+x^9+x^{11}$ over $GF(2)$	Initial seed: TX0: {11111111111b} TX1: {11101110000b} TX2: {11011110000b}
PRTS7	Pseudo-Random Ternary sequence generated with the polynomial: $G(x)=1+x^2+2x^7$ over $GF(3)$	Initial seed: TX0: {1111111t} TX1: {0120210t} TX2: {1210212t}
PRTS19	Pseudo-Random Ternary sequence generated with the polynomial: $G(x)=1+x^2+2x^{19}$ over $GF(3)$	Initial seed: TX0: {111111111111111111t} TX1: {1210120212021012101t} TX2: {1210121020102120212t}

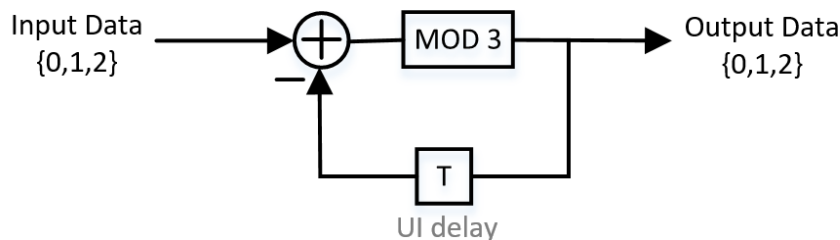
4.3.2.8 Pre-coding

Pre-coding is implemented to minimize the impact of error bursts. Pre-coding shall be turned on with the first bit that is RS-FEC encoded. The pre-coder output shall be calculated by subtracting the previous output from the input as follows:

$$Out[n] = MOD(In[n] - Out[n - 1], 3)$$

When Pre-Coding is turned on, output data = 0 is subtracted from the first trit of input data.

Figure 4-43 describes the operation of the Pre-coding.

Figure 4-43. Description of Pre-coding Operation

4.4 USB4 Link Operation

4.5 Sleep and Wake

This section describes how a Router participates in a system transition to sleep state and how wake events may bring the Router back from sleep.

4.5.1 Entry to Sleep

A Router shall enter sleep state when the *Enter Sleep* bit is set to 1b and one of the following sleep events occur:

- Host Router
 - The Router receives an implementation-specific signal indicating entry to sleep state.
- Device Router
 - The Router tunnels PCIe traffic and receives a PERST Active Tunneled Packet on the Upstream Facing Port.
 - The Router receives an LT_LRoff Transaction on the Sideband Channel of an Upstream Facing Port.

A Router shall not enter sleep state unless the *Enter Sleep* bit is set to 1b before a sleep event occurs.



CONNECTION MANAGER NOTE

If a Connection Manager initiates Transactions on the Sideband Channel, then the Connection Manager shall not set the Enter Sleep bit to 1b until all such Transactions are complete. A Connection Manager shall not initiate a Transaction on the Sideband Channel after the Enter Sleep bit is set to 1b.

After setting the Enter Sleep bit to 1b, a Connection Manager shall not write to a USB4 Port is Configured bit or USB4 Port is Inter-Domain bit.

After the *Enter Sleep* bit is set to 1b, the Router shall complete any pending Transactions on the Sideband Channel. When the Router is ready for the sleep event it shall set the *Sleep Ready* bit to 1b. After setting the *Sleep Ready* bit and before the Sleep event, the Router shall not initiate any Sideband transaction except LT_LRoff. A Router shall set the *Sleep Ready* bit to 1b within tSetSR time after the *Enter Sleep* bit is set to 1b, unless the Router is waiting for a Notification Acknowledgment Packet as described in Section 11.1.4.2. A Router shall also send the Connection Manager a Notification Packet with Event Code = ROP_CMPLT and the *Event Info* field set to 03h.

After a sleep event occurs, the Router shall do the following for each USB4 Port:

- If the *USB4 Port is Inter-Domain* bit is 0b and the *USB4 Port is Configured* bit is 0b, perform a disconnect by driving its SBTX line low for tDisconnectTx. If the *Enable Wake on Connect* bit of the USB4 Port is 1b, the USB4 Port shall drive its SBTX line high after tDisconnectTx.
- If the *USB4 Port is Inter-Domain* bit is 1b and the *Enable Wake on Inter-Domain* bit is set to 0b, perform a disconnect by driving its SBTX line low for tDisconnectTx.
- Else:
 - If the Router supports PCIe Tunneling, send at least 3 PERST Active Tunneled Packets on all Downstream PCIe Adapters that have the *Path Enable* bit set to 1b.
 - Send an LT_LRoff Transaction on the Sideband Channel within tLRoffResponse after detecting the sleep event.
 - If the *USB4 Port is Inter-Domain* bit is 0b and the *USB4 Port is Configured* bit is 1b, wait for an LT_LRoff Transaction on the Sideband Channel, unless an LT_LRoff Transaction was already received from the time the *Enter Sleep* bit was set to 1b.
 - If the Downstream Facing Port is expecting an LT_LRoff Transaction and doesn't receive it within 30 ms, it is recommended that the USB4 Port initiate a disconnect by driving its SBTX line low for tDisconnectTx.
 - Transition the Adapters to CLd state.

If a Downstream Facing Port drives its SBTX line low after a sleep event, it is recommended that it keep it low for the duration of the sleep. This will prevent the attached Router from issuing any Transactions on the Sideband Channel and allow it to enter a lower power state.



CONNECTION MANAGER NOTE

The following is an example of how a Connection Manager should transition its Domain into system sleep:

1. *The Connection Manager sets the Enter Sleep bit to 1b in each Router.*
2. *The Connection Manager reads the Sleep Ready bit in each Router.*

3. When all Routers have the Sleep Ready bit set to 1b, the host system initiates a Sleep Event, which causes the Routers to transition to sleep state.
4. The Host system goes into system sleep.



IMPLEMENTATION NOTE

It is expected that an LT_LRoff Transaction is received within 30 ms from sending the LT_LRoff Transaction.

If the LT_LRoff Transaction is sent over an Inter-Domain Link, the Link Partner outside the Domain goes through disconnect as defined in Section 4.4.5.2.2.

4.5.2 Behavior in Sleep State

On entry to sleep state, a Router shall restore all Configuration Spaces to their default values.

If the *Enter Sleep* bit is set to 1b, a Router shall retain a copy of the state information listed in Table 4-71 separate from Configuration Space.

Table 4-714-70. Router State Retained During Sleep

Field Copied	Configuration Space / Capability	Value
Upstream Adapter	Router Configuration Space	<i>Upstream Adapter</i> field prior to sleep entry.
USB4 Port is Configured	USB4 Port Capability	<i>USB4 Port is Configured</i> bit prior to sleep entry.
USB4 Port is Inter-Domain	USB4 Port Capability	<i>USB4 Port is Inter-Domain</i> bit prior to sleep entry.
Enable Wake on Connect	USB4 Port Capability	<i>Enable Wake on Connect</i> bit prior to sleep entry.
Enable Wake on Disconnect	USB4 Port Capability	<i>Enable Wake on Disconnect</i> bit prior to sleep entry.
Enable Wake on Inter-Domain	USB4 Port Capability	<i>Enable Wake on Inter-Domain</i> bit prior to sleep entry.
Enable Wake on USB4	USB4 Port Capability	<i>Enable Wake on USB4</i> bit prior to sleep entry.
Enable Wake on PCIe	Router Configuration Space	<i>Enable Wake on PCIe</i> bit prior to sleep entry.
Enable Wake on USB3	Router Configuration Space	<i>Enable Wake on USB3</i> bit prior to sleep entry.
Enable Wake on DP	Router Configuration Space	<i>Enable Wake on DP</i> bit prior to sleep entry.
Far-end receiver termination	--	Indicator value of USB far-end receiver termination for USB3 Gen X. See Section 9.1.1.1.2.
Path Established	--	Indicator value if Path is established for USB3 Gen T. See Section 9.1.5.
DP Resource Allocation	--	Which DP Resources were allocated to which DP IN Adapters prior to sleep entry.
Target Asymmetric Link	Lane Adapter Configuration	<i>Target Asymmetric Link</i> field prior to sleep entry.
Target Link Speed	Lane Adapter Configuration	<i>Target Link Speed</i> field prior to sleep entry.
Enable Scrambler Re-Sync (ESRS) Gen 2 or Gen 3	Sideband Register Space	Value of ESRS for Gen 2 or Gen 3 prior to sleep entry.
Enable Scrambler Re-Sync (ESRS) Gen 4	Sideband Register Space	Value of ESRS for Gen 4 prior to sleep entry.

If a USB4 Port has the *USB4 Port is Inter-Domain* state set to 1b, then the USB4 Port shall ignore any Transactions received on the Sideband Channel while in sleep state.

4.5.3 Wake Events

A Router shall support the wake events defined in Table 4-72.

Table 4-724-71. Wake Events

Type	Description
Wake on Connect	A Router shall issue a Wake on Connect if the <i>Enable Wake on Connect</i> bit of a USB4 Port is set to 1b, the <i>USB4 Port is Configured</i> bit is 0b, the USB4 Port is Inter-Domain bit is set to 0b, and it detects either of the following after the <i>Enter Sleep</i> bit is set to 1b: <ul style="list-style-type: none"> A connection on the USB Type-C connector attached to the USB4 Port. SBRX is at logic high on the USB4 Port for tConnectRx.
Wake on Disconnect	A Router shall issue a Wake on Disconnect if the <i>Enable Wake on Disconnect</i> bit of a USB4 Port is set to 1b, the <i>USB4 Port is Inter-Domain</i> bit is set to 0b, the <i>USB4 Port is Configured</i> bit is set to 1b, and the Router detects either of the following after the <i>Enter Sleep</i> bit is set to 1b: <ul style="list-style-type: none"> A disconnect on the USB Type-C connector attached to the USB4 Port. SBRX is at logic low on the USB4 Port for tDisconnectRx.
Wake on Inter-Domain	A Router shall issue a Wake on Inter-Domain event if the <i>Enable Wake on Inter-Domain</i> bit is set to 1b, the <i>USB4 Port is Inter-Domain</i> bit is set to 1b, and the Router detects either of the following after the <i>Enter Sleep</i> bit is set to 1b: <ul style="list-style-type: none"> A disconnect on the USB Type-C connector attached to the USB4 Port. SBRX is at logic low on the USB4 Port for tDisconnectRx.
Wake on PCIe	A Router shall issue a Wake on PCIe event if the <i>Enable Wake on PCIe</i> bit is set to 1b, and it detects a PCIe Wake event from any connected PCIe Endpoint or Switch after a Sleep Event occurs.
Wake on USB3	A Router shall issue a Wake on USB3 event if the <i>Enable Wake on USB3</i> bit is set to 1b, and it detects a USB3 Wake event from any connected USB device after a Sleep Event occurs.
Wake on USB4	A Router shall issue a Wake on USB4 event if the <i>USB4 Port is Inter-Domain</i> bit is set to 0b, the <i>USB4 Port is Configured</i> bit is set to 1b, the <i>Enable Wake on USB4 Wake</i> is set to 1b, and the Router detects at least one transition of SBRX to logical low for tWake time after a Sleep Event occurs.
Wake on DP	A Router shall issue a Wake on DP event if the <i>Enable Wake on DP</i> bit is set to 1b, and it detects an HPD Plug Event or reception of an HPD IRQ after a Sleep Event occurs.
Wake by Host System	A Host Router shall issue a Wake by Host System when it detects an implementation-specific wake indication from the host system.

4.5.4 Exit from Sleep

A Router exits sleep state when one of the following occurs:

- An Upstream Facing Port Disconnect (see Section 4.5.4.1)
- Detection of a Wake on USB4 event (see Section 4.5.4.2)

4.5.4.1 Upstream Facing Port Disconnect

When a Router detects a disconnect on the Upstream Facing Port, it shall exit sleep state. See Section 4.4.5.1 for how a Router detects and handles an Upstream Facing Port disconnect.

4.5.4.2 Wake on USB4 Event

A Wake on USB4 event is used to propagate a wake event throughout a USB4 Fabric. A Router shall assert SBTX to logical low for tWake time to indicate a Wake on USB4 event.

After detecting one of the wake events listed in Table 4-72, a Router shall:

- Issue a Wake on USB4 event on all connected USB4 Ports by asserting SBTX to logical low for tWake time.
 - If the detected wake event is a Wake on USB4 event, the Router may issue a Wake on USB4 event to the USB4 Port where the Wake on USB4 event arrived, but is not required to do so.

2. Begin Lane Initialization on all connected USB4 Ports.
 - A USB4 Port may ignore any Transactions received before it is ready for Lane Initialization. The transmitting USB4 Port shall retry the Transactions as defined in Section 4.1.1.2.6.
3. For every Adapter that reaches CL0 state, the Router sends a Hot Plug Event Packet to the Connection Manager with the *UPG* bit set to 0b.

4.6 Timing Parameters

Table 4-73 lists the timing parameters for the Logical Layer.



IMPLEMENTATION NOTE

When both a Min and a Max value are listed in the table below, an implementation can choose to implement that parameter with any value in the given range. Furthermore, an implementation cannot assume that its Link Partner will use the Max value and needs to be prepared for Link Partners that use any value between Min and Max (inclusive).

Table 4-73~~4-72~~. Logical Layer Timing Parameters

Parameter	Description	Min	Max	Units
tDisconnectTx	The time that SBTX is driven to logical low to identify a disconnect.	50	--	ms
tDisconnectRx	The time that SBRX is detected in logical low to identify a disconnect.	14	1000	μs
tConnectRx	The time that SBRX is detected in logical high to identify a new connection.	25	--	μs
tCmdResponse	The time between receiving an AT Command and sending an AT Response or between receiving an Addressed RT Command and sending an RT Response.	--	50	ms
tATTimeout	The amount of time the originator of an AT Command waits before optionally timing out the AT Command.	100	--	ms
tRTTimeout	The amount of time the originator of an Addressed RT Command waits before optionally timing out the Addressed RT Command.	100	--	ms
tLTPhase4	The amount of time that Broadcast RT Transactions are sent after completion of Lane Initialization Phase 2.	25	--	ms
tTxFFEResponse	The time between the last bit of the write to a Gen 4 TxFFE register that sets the New Request bit to 1b and the first bit of the write to a Gen 4 TxFFE register that sets the Request Done bit to 1b.	--	2	ms
tWake	The time that SBRX is in logic low to initiate exit from sleep state.	1	9	Bit time
tDisabled	The minimal time an Adapter stays in a Disabled State after entering the state.	10	--	ms

Parameter	Description	Min	Max	Units
tTrainingError	The time an Adapter has to transition to CL0 state before a Timeout Error is generated. The time is measured from when the Adapter either sends the first SLOS1 in Training state (for Gen 2/3) or starts the exit from CLx (for Gen 4) to when it transitions to CL0 state (see Sections 4.2.1.6.5.1.2 and 4.2.1.6.5.4).	480	700	µs
tTrainingAbort1	The amount of time in Training state or Asymmetric transition following Lane Initialization.	1	--	sec
tTrainingAbort2	<ol style="list-style-type: none"> 1. The amount of time in Training state following any transition to Training state other than from CLd state. 2. The time to send LFPS when exiting CL1 or CL2 or exiting CL0s for Gen 4. 3. The time to send SLOS1 in CL0s exit. 3-4. <u>The amount of time in CLx Exit from LFPS transmission to either detecting LFPS or reaching Training.LOCK1 sub-state for Gen2/3.</u> 	100	--	ms
tLaneParams	The time interval between transmissions of Broadcast RT Transactions.	Lane Initialization - 1 Recovery Flow - 0	5	ms
tPollTXFFE	The rate of polling during the TxFFE flows.	1	5	ms
tGen4TS1	The time to transition to the TS2 sub-state from the TS1 sub-state for a Gen 4 Link.	--	400	ms
tGen4TS2	The time to transition to the TS3 sub-state from the TS2 sub-state for a Gen 4 Link.	--	200	ms
tBonding	The time to transition to CL0 state from transmitting the first TS1 Ordered Set before failure to bond is determined.	40	100	µs
tCLxIdleRx	The time for a receiver to wait after the last LFPS cycle received before starting calibration.	130	--	ns
tCLxRetry	The time that a requester waits after receiving the last bit of a CL_NACK Ordered Set before sending the first bit of another CL2_REQ Ordered Set or CL1_REQ Ordered Set.	1.5	--	µs
tCLxRequest	Time from receiving the last bit of a Request Ordered Set to sending the first bit of a CL2_ACK, CL1_ACK, or CL0s_ACK Ordered Set.	--	14 (Host Router) 2 (Device Router)	µs

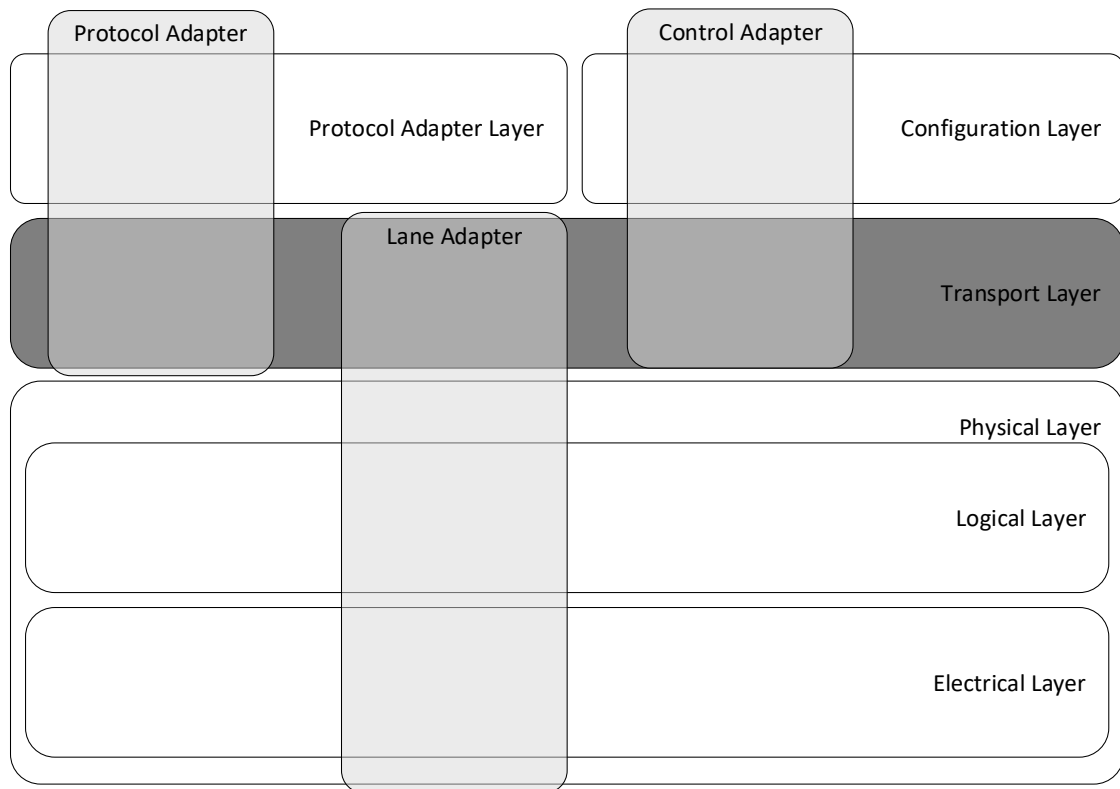
Parameter	Description	Min	Max	Units
tCLxResponse	Time from detection of a CL2_ACK, CL1_ACK, or CL0s_ACK Ordered Set to sending the first CL_OFF Ordered Set. Also, the time from detection of a Link error to sending the first SLOS.	--	800	ns
tCLxSetup	The time required for a Responding Port to meet tCL0sEntry and tCL0sExit timing, after sending CL_NACK.	--	200	μs
tCLxAccept	The duration in which the Responding Port is required to meet tCL0sEntry and tCL0sExit timing.	500	--	μs
tTxOff	Time between sending the last CL_OFF Ordered Set and shutting off the transmitters of a requesting USB4 Port when entering a CLx state or as part of Gen 4 Asymmetric Link Transitions.	--	100 (Gen 2/3) 150 (Gen 4)	ns
tEnterLFPS1	For a Gen 2 or Gen 3 Link, time between shutting off the transmitters of a requesting USB4 Port and enabling transmission and detection of LFPS in CL1 or CL2 states. For a Gen 4 Link, time between shutting down Tx0 to enable LFPS transmission.	400	500	ns
tEnterLFPS2	Time to activate LFPS detection when entering CLx (see section 4.2.1.6 for more details).	2500 (Gen 2/3) 400 (Gen 4)	5000 (Gen 2/3) 500 (Gen 4)	ns
<u>tEnterLFPS3</u>	<u>Time between shutting down the transmitter to the last LFPS sent on CL1/2 exit flow.</u>	<u>18</u>	<u>25</u>	
tEnterLFPS4	Time between shutting off the transmitters of a requesting USB4 Port and enabling transmission of LFPS in CL0s state.	1700	2000	ns
tEnterLFPS5	Time between shutting off the receivers of the responding USB4 Port after reception a CL_OFF Ordered Set and enabling detection of LFPS in CL0s states.	2500	3000	ns
tTimeInCL0	The time a Lane Adapter stays in CL0 after exiting CLx when the Link is Gen 4 speed.	500	--	ns
tLFPSDuration	Time between transmitting the first LFPS cycle and transmitting the last LFPS cycle upon CL0s exit and after detecting LFPS upon CL1/2 exit.	--	2560	ns
tStopLFPS1	Time between when the conditions to stop LFPS are met and the last LFPS cycle in the Lane Initialization and Asymmetric transition flow.	--	150	μs
tStopLFPS2	Time between when the conditions to stop LFPS are met and the last LFPS cycle in a CLx exit flow.	--	2	μs

Parameter	Description	Min	Max	Units
tCL0sSwitch	Time to abort normal CL0s exit flow if a CL_WAKE1.(X+1) Ordered Set Symbol does not arrive after CL_WAKE1.X Ordered Set Symbols.	500	--	μs
tWarmUpCL0s	When exiting CL0s state, time between receiving the first LFPS cycle and achieving the first Symbol lock.	--	50	μs
tWarmUpCL1	When exiting CL1 state, time between receiving the first LFPS cycle and sending the first LFPS.	--	2110	μs
tWarmUpCL2	When exiting CL2 state, time between receiving the first LFPS cycle and sending the first LFPS.	--	100250	μs
tRxLock	Time to achieve the first Symbol lock during exit from CLx states.	--	50 (Gen 2/3) 30 (Gen 4)	μs
tWakeResponse	Time between receiving the last bit of a CL_WAKE1/2.X Ordered Set Symbol and sending the first bit of the relevant response (CL_WAKE2.X or SLOS).	--	7 (Host Router) 1 (Device Router)	μs
tTrainingTransition	Time to transition Training Sub-State where no errors on the receive signal	--	7 (Host Router) 1 (Device Router)	μs
tActivateSSC	Time between transmitting the first trit of the first TS4 and activating SSC.	--	1000 (Transition to Training from CLd) 10 (Otherwise)	μs
tSSCActivated	Time after activating SSC that the transmitter sends TS4 with <i>Counter</i> field set to 0h.	2	1000 (Transition to Training from CLd) 5 (Otherwise)	μs
tSymbolLock	Time to achieve Symbol alignment lock in CL0s/1/2 exit flow.	--	1	μs
tLROffResponse	Time between a sleep event and sending an LT_LROff Transaction.	--	20	ms
tTS2Timeout	While exiting CL0s state, the time to transition to Training state after sending TS2 Ordered Sets and not receiving TS2 Ordered Sets.	9	--	μs
tActivateNewTx	Timer from sending the LT_SwitchAck Transaction to transmitting LFPS on a new transmitter in Asymmetric transition.	1	--	ms
tSetSR ¹	Time from when the <i>Enter Sleep</i> bit is set to 1b to when the <i>Sleep Ready</i> bit is set to 1b.	--	50	ms
tLocalSBAccess	Time to complete a read or write to the local SB Register Space in a Router.	--	50	ms
tRemoteSBAccess	Time to complete a read or write to SB Register Space in a Re-timer.	--	150	ms
tSwitchAck	Time to respond with an LT_SwitchAck Transaction after receiving an LT_SwitchRx2Tx Transaction.	1	10	ms

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Parameter	Description	Min	Max	Units
tRecoveryAbort	Time to enter CL0 after sending an ELT_Recovery Transaction.	--	10	ms
tRecoveryResponse	Time to send the first bit of an ELT_Recovery response after receiving the last bit of an ELT_Recovery Transaction after the Sideband transmitter is in idle.	--	200	μs
tRecoveryTxOff	Time between receiving the last bit of an ELT_Recovery Transaction and shutting off the Lane Adapter transmitter.	--	150	μs
tRecoveryRxOff	Recommended time between shutting off the Lane Adapter receivers and sending the last bit of the ELT_Recovery Transaction.	--	50	μs
<u>tRecoveryRxErr</u>	<u>Time from detecting a link error to sending the last bit of ELT Recovery.</u>	<u>--</u>	<u>150</u>	<u>μs</u>
tScramblerSampleRate	The time between scrambler state sampling occasions.	2	10	ms
tScramblerReSyncMessage	The time between scrambler state sampling time and the first bit of the write command to the debug register containing the sampled data and LFSR states.	--	0.5	ms
tSBInterSymbolGap	The time between the stop bit of a Symbol to the start bit of the following Symbol on the same transaction.	--	1	ms
<u>tTxSLOS</u>	<u>Time to send SLOS after detecting the conditions to send next Ordered Sets.</u>	<u>200 (Gen2)</u> <u>100 (Gen 3)</u>	<u>--</u>	<u>ns</u>
<u>tGen4TS2Lock</u>	<u>Time to lock on Gen 4 TS2 on CLx exit.</u>	<u>--</u>	<u>30</u>	<u>μs</u>
Notes:				
1. If any of the Router's Sideband Channels operate in TBT3-compatible mode, then the maximum value of tSetSR is 80 ms.				

5 Transport Layer



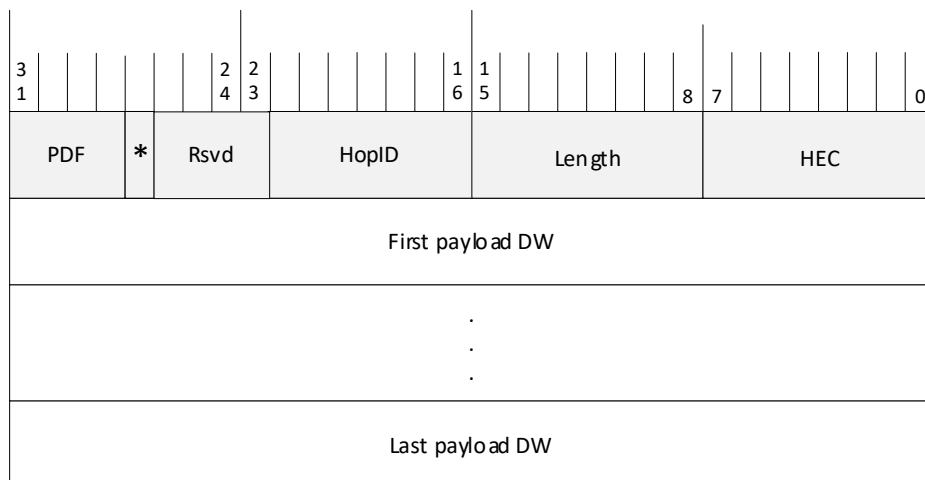
5.1 Transport Layer Packets

5.1.1 Conventions

5.1.1.1 Bit/Byte Conventions

The packet formats defined in this chapter are shown with the Doubleword layout in Figure 5-1, where the least-significant bit is on the right. Fields within each Doubleword are also shown using this convention.

Figure 5-1. Convention for Transport Layer Diagrams



* SuppID

5.1.1.2 Reserved Values and Fields

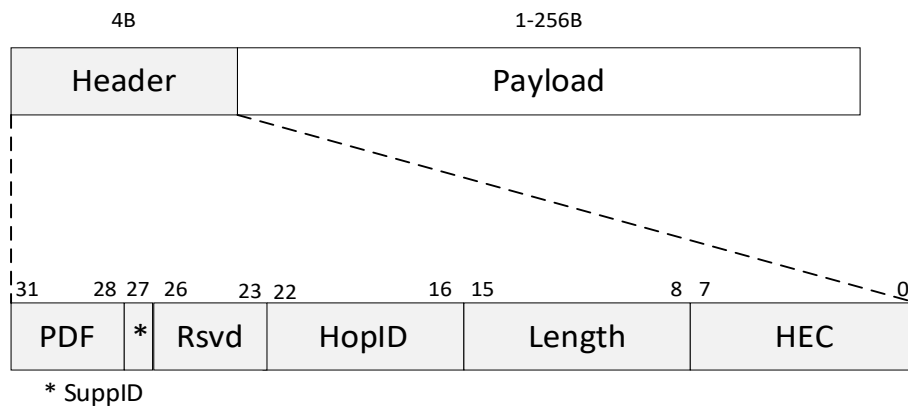
Unless otherwise specified, fields and values marked “Reserved” shall be handled as described in Table 5-1.

Table 5-1 Reserved Value and Field Handling

Type	Handling
Reserved value	<p>The originator of a Packet shall not use a value that is marked as “Rsvd”.</p> <p>A Router that forwards a Packet shall ignore any field containing a reserved value and shall forward the Packet to its target. The forwarding Router shall not modify the contents of the field. However, if the field containing a reserved value is required for the Routers operation, then the Router shall drop the Packet and proceed as if the Packet was never received</p> <p>The target of a Packet shall ignore a Packet that has any of its defined fields set to an Rsvd value and proceed as if the packet was never received.</p>
Reserved field	<p>The originator of a Packet shall set a field that is marked “Rsvd” to zero.</p> <p>A Router that forwards a Packet shall ignore any fields that are marked “Rsvd” and shall forward the Packet to its target. The forwarding Router shall not modify the contents of the field.</p> <p>A receiver shall ignore any fields that are marked “Rsvd”.</p>

5.1.2 Format

All Transport Layer Packets shall start with the 4-byte header described in Section 5.1.2.1. All Transport Layer Packets except Idle Packets shall carry between 1 and 256 bytes (inclusive) of payload. Section 5.1.3.3.1 describes Idle Packets. Figure 5-2 shows the format of a Transport Layer Packet with payload.

Figure 5-2. Transport Layer Packet Format**5.1.2.1 Header****Table 5-2. Transport Layer Packet Header Format**

Bits	Field	Description
7:0	<i>HEC</i>	Header Error Control – See Section 5.1.2.1.1.
15:8	<i>Length</i>	Length – Shall contain the payload size in bytes excluding the padding size. A value of 00h is used to indicate a payload size of 256 bytes.
22:16	<i>HopID</i>	HopID – Uniquely identifies a Path in the context of a Link. See Section 5.2.2.
26:23	<i>Rsvd</i>	Reserved

Bits	Field	Description
27	<i>SuppID</i>	Supplemental ID – Used to distinguish certain types of Link Management Packets that need additional distinction. Shall be set to 0b in a Tunneled Packet.
31:28	<i>PDF</i>	Protocol Defined Field – Contents depend on packet type. Tunneled Packets: defined by the Protocol Adapter Layer. Link Management and Control Packets: together with the <i>SuppID</i> and <i>HopID</i> fields, identifies the Link Management or Control Packet type.

5.1.2.1.1 Header Error Control (HEC)

The *HEC* field in a Transport Layer Packet Header shall cover bits[31:8] of the Transport Layer Packet Header. It shall not cover any payload. The *HEC* field consists of 8 redundancy bits, which shall be calculated from bit 31 to bit 8 as follows:

- Width: 8
- Poly: 07h
- Init: 00h
- RefIn: False
- RefOut: False
- XorOut: 55h

See Appendix A for examples of HEC calculations.

When a Router receives a Transport Layer Packet, it shall verify the *HEC* field value in the packet. The Router shall correct any single-bit errors in the Transport Layer Packet Header. After correcting an error, a Router shall continue on as if the error had never occurred.

When an Ingress Adapter that is a Lane Adapter detects an uncorrectable HEC error, it shall:

- Drop the packet with the error.
- Set the *HEC Error* bit in the Adapter Configuration Space to 1b.
- Increment the *HEC Errors* field in Adapter Configuration Space.

If the Ingress Adapter that detected the uncorrectable HEC error is a part of a Downstream Facing Port:

1. The Ingress Adapter shall send a Notification Packet upstream if the *HEC Error Enable* bit in the Adapter Configuration Space is set to 1b. The Notification Packet shall contain Event Code = ERR_HEC (see Section 6.5).
2. The Lane Adapters in the USB4® Port with the Ingress Adapter shall:
 - a. If the Link is Gen 2 or Gen 3, enter the Training state.
 - b. If the Link is Gen 4, initiate Gen 4 Link Recovery.

If the Ingress Adapter that detected the uncorrectable HEC error is a Lane Adapter that is a part of an Upstream Facing Port:

1. The Lane Adapter(s) in the USB4 Port with the Ingress Adapter shall:
 - a. If the Link is Gen 2 or Gen 3, enter the Training state.
 - b. If the Link is Gen 4, initiate Gen 4 Link Recovery.
2. When the Lane Adapter enters CL0 state, it shall send a Notification Packet upstream if the *HEC Error Enable* bit in the Adapter Configuration Space is set to 1b. The Notification Packet shall contain Event Code = ERR_HEC (see Section 6.5).

5.1.2.2 Payload Padding

The size of a Transport Layer Packet is always a multiple of 4 bytes. The Protocol Adapter Layer of a Source Adapter shall add between 0 and 3 bytes of padding to the payload of a Tunneled Packet to ensure that the Tunneled Packet is of a size that is a multiple of 4 bytes. The Protocol Adapter Layer of the Destination Adapter shall remove any bytes of padding.

The content of the padding bytes is implementation-specific and cannot be assumed to have any specific values. However, it is recommended that zero-byte padding be used.

5.1.2.3 Error Correction Code (ECC)

When a Transport Layer Packet contains an *ECC* field, the ECC shall be calculated as described in this section.

The *ECC* field is calculated over a portion of the payload within a Transport Layer Packet. The *ECC* field consists of 8 redundancy bits, which shall be calculated from most significant bit to least significant bit as follows:

- Width: 8
- Poly: 07h
- Init: 00h
- RefIn: False
- RefOut: False
- XorOut: 00h

See Appendix A for examples of ECC calculations.

5.1.3 Transport Layer Packet Types

Transport Layer Packets are either Tunneled Packets from a Protocol Adapter Layer, Control Packets from the Configuration Layer, or Link Management Packets generated within the Transport Layer.

The format and types of Link Management Packets (except for Time Sync Packets) are defined in this section. Time Sync Packets are defined in Section 7.3.3. Unless specified otherwise, a transmitter shall set a field that is marked “Rsvd” to zero. A receiver shall ignore any fields that are marked “Rsvd”.

5.1.3.1 Tunneled Packets

Tunneled Packets are generated by the Protocol Adapter Layer of a Source Adapter and handed off to the Transport Layer. A Tunneled Packet shall have the header defined for Transport Layer Packets in Table 5-2. The Protocol Adapter Layer of a Source Adapter shall fragment Tunneled Protocol traffic larger than 256 bytes into multiple Tunneled Packets. Re-assembly of Tunneled Protocol traffic from Tunneled Packets shall be performed by the Protocol Adapter Layer of the Destination Adapter.

A Transport Layer may modify the *HopID* and *HEC* fields of a Tunneled Packet. It shall not modify any other fields in a Tunneled Packet Header and it shall not modify the payload.

5.1.3.1.1 Power Management (PM) Packet

Power Management (PM) Packets are used to ensure that a Lane Adapter only allows entry to a Low Power state if none of the Paths that traverse the Adapter assert any objections.

An Ingress Adapter uses its Routing Table to determine the Egress Adapter and Egress HopID values for a received PM Packet.

A PM Packet shall consist of the header described in Table 5-3 followed by 1 DW of payload as described in Table 5-4. See also Figure 5-3 for the structure of a PM Packet for the CL1 and CL2 Low Power states.

Table 5-3. Power Management Packet Header

Bits	Field	Description
7:0	<i>HEC</i>	See Section 5.1.2.1.1
15:8	<i>Length</i>	04h
22:16	<i>HopID</i>	HopID corresponding to the target Path
26:23	<i>Rsvd</i>	Reserved
27	<i>SupplD</i>	0b
31:28	<i>PDF</i>	Eh

Table 5-4. Power Management Packet Payload

Bits	Field	Description
1:0	<i>CLx State</i>	CLx State – Indicates which Low Power states are possible in the Lane Adapters that this packet traverses. 00b – indicates that no CLx states are possible. 01b – indicates that CL1 state is possible. 11b – indicates that CL1 and CL2 states are possible. All other values are reserved.
31:2	<i>Reserved</i>	Reserved

Figure 5-3. PM Packet for CL1 and CL2 States

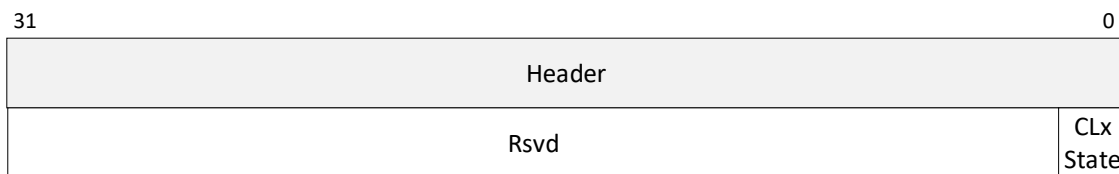
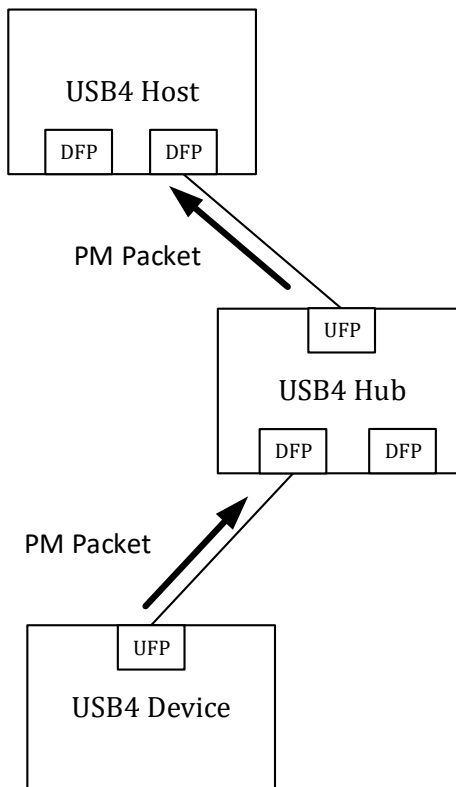


Figure 5-4 shows an example of how a PM Packet traverses a topology with a Host Router, Hub Router, and Device Router. The Device Router transmits a PM Packet with the option to enter CL1 from a Protocol Adapter. The PM Packet targets a Protocol Adapter in the Host Router. When the PM Packet is forwarded from the Downstream Facing Port to the Upstream Facing Port of the Hub Router, the Upstream Facing Port of the Hub Router removes its objection to CL1.

Figure 5-4. Example of a PM Packet**5.1.3.2 Control Packets**

Control Packets are defined in Section 6.4.2.

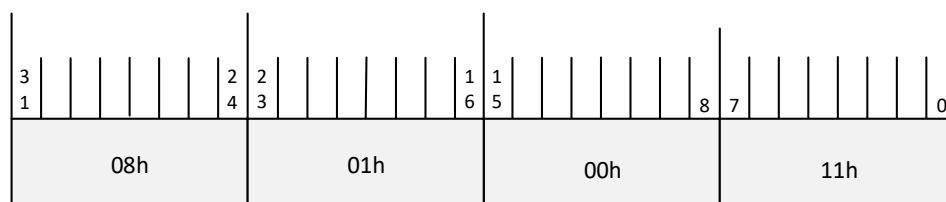
5.1.3.3 Link Management Packets

Link Management Packets are confined to a Link. They originate from the Transport Layer at one side of a Link and terminate at the Transport Layer at the other side of the Link.

5.1.3.3.1 Idle Packets

Idle Packets ensure that the Transport Layer feeds the Logical Layer with a continuous byte stream. When an Adapter is in CL0 state, the Transport Layer shall insert Idle Packets at the transmitting end of a USB4 Link if there are no other Transport Layer Packets to be transmitted. A Transport Layer shall remove Idle Packets at the receiving end of the USB4 Link.

An Idle Packet consists of a Transport Layer Packet Header with no payload. An Idle Packet shall have the format shown in Figure 5-5.

Figure 5-5. Idle Packet Contents

5.1.3.3.2 Credit Grant Packet

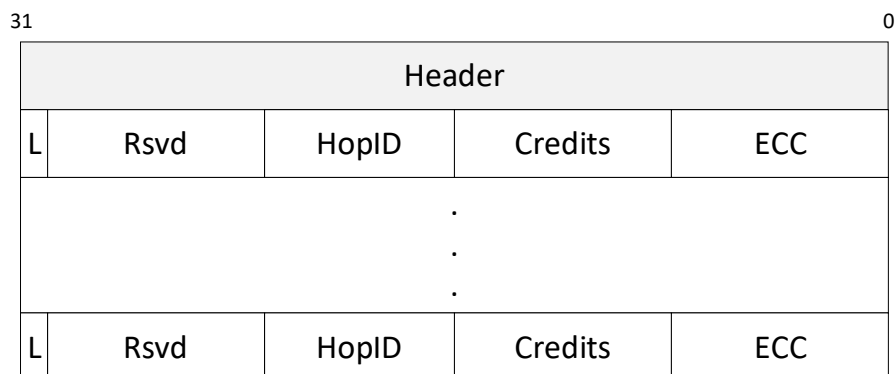
This packet is used to transmit credit information from an Ingress Adapter to an Egress Adapter. A Credit Grant Packet shall include the header in Table 5-5 followed by one or more of the Credit Grant Records defined in Table 5-6. A Credit Grant Packet shall not contain more than 64 Credit Grant Records. When more than one Credit Grant Record is sent in the same Credit Grant Packet, they shall be processed in the order received.

Table 5-5. Credit Grant Packet Header

Bits	Field	Description
7:0	<i>HEC</i>	See Section 5.1.2.1.1
15:8	<i>Length</i>	Number of Credit Grant Records * 4 or 00h if packet is carrying 64 Credit Grant Records (256 bytes)
22:16	<i>HopID</i>	01h
26:23	<i>Rsvd</i>	Reserved
27	<i>SuppID</i>	0b
31:28	<i>PDF</i>	1h

Table 5-6. Credit Grant Record Format

Bits	Field	Description
7:0	<i>ECC</i>	Error Correction – Calculated over bits [31:8] of the Credit Grant Record. See Section 5.1.2.3 for calculation.
15:8	<i>Credits</i>	Flow Control Credits – Indicates the total number (modulo 256) of flow control credits granted to the Egress Adapter for the specified Path or Shared Buffer since initialization. For a Path, it carries the value of the PCA state variable (see Section 5.3.2.1.2). For a Shared Buffer, it carries the value of the SCA state variable (see Section 5.3.2.1.2).
22:16	<i>CreditHopID</i>	HopID – Indicates the HopID of the Path for which the credit grant shall be applied. This field shall only be valid if L Flag= 0b.
30:23	<i>Rsvd</i>	Reserved
31	<i>L</i>	L Flag – Identifies whether the Credit Grant Record applies to a Path or a Shared Buffer. Shall be set to 0b for a Path or 1b for a Shared Buffer.

Figure 5-6. Credit Grant Packet Format

5.1.3.3.3 Path Credit Sync Packet

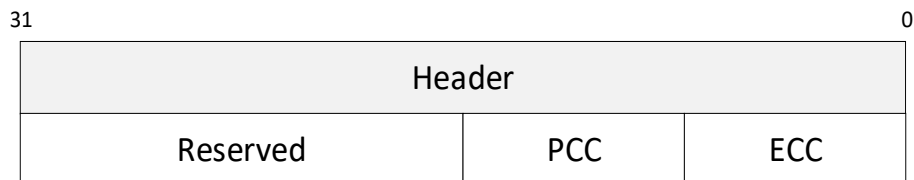
This packet is used by an Egress Adapter to maintain credit count synchronization for a given Path with an Ingress Adapter. A Path Credit Sync Packet shall consist of the header in Table 5-7 followed by the payload defined in Table 5-8. See also Figure 5-7.

Table 5-7. Path Credit Sync Packet Header

Bits	Field	Description
7:0	<i>HEC</i>	See Section 5.1.2.1.1
15:8	<i>Length</i>	04h
22:16	<i>HopID</i>	HopID corresponding to the target Path
26:23	<i>Rsvd</i>	Reserved
27	<i>SupplD</i>	1b
31:28	<i>PDF</i>	0h

Table 5-8. Path Credit Sync Packet Payload

Bits	Field	Description
7:0	<i>ECC</i>	Error Correction – Calculated over bits [31:8] of the Path Credit Sync Packet payload. See Section 5.1.2.3 for calculation.
15:8	<i>PCC</i>	Path Credits Consumed – Represents the number (modulo 256) of credits consumed by the Egress Adapter for the Path identified by the <i>HopID</i> field up to (and including) the last packet transmitted on the Path prior to this Path Credit Sync Packet.
31:16	<i>Rsvd</i>	Reserved.

Figure 5-7. Path Credit Sync Packet Format**5.1.3.3.4 Shared Buffers Credit Sync Packet**

This packet is used by an Egress Adapter to maintain credit count synchronization with an Ingress Adapter for the Shared Buffer. A Shared Buffers Credit Sync Packet shall consist of the header in Table 5-9 followed by the payload defined in Table 5-10. See also Figure 5-8.

Table 5-9. Shared Buffers Credit Sync Packet Header

Bits	Field	Description
7:0	<i>HEC</i>	See Section 5.1.2.1.1
15:8	<i>Length</i>	04h
22:16	<i>HopID</i>	01h
26:23	<i>Rsvd</i>	Reserved
27	<i>SupplD</i>	0b
31:28	<i>PDF</i>	2h

Table 5-10. Shared Buffers Credit Sync Packet Payload

Bits	Field	Description
7:0	<i>ECC</i>	Error Correction – Calculated over bits [31:8] of the Shared Buffers Credit Sync Packet payload. See Section 5.1.2.3 for calculation.
15:8	<i>SCC</i>	Shared Credits Consumed – Represents the number (modulo 256) of Shared Buffer credits consumed by the Egress Adapter up to (and including) the last packet transmitted prior to this Shared Buffers Credit Sync Packet.
31:16	<i>Rsvd</i>	Reserved.

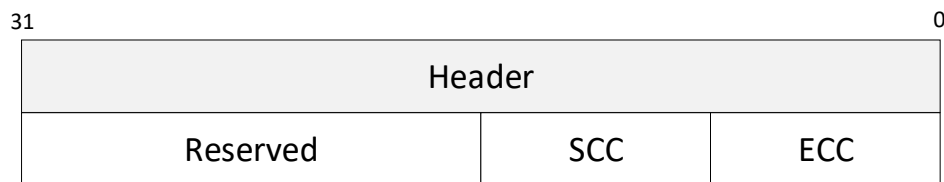
Figure 5-8. Shared Buffers Credit Sync Packet Format**5.1.4 Effect of Link State on Transport Layer Packets**

Table 5-11 describes how the Logical Layer Link states defined in Section 4.2.3 affect Transport Layer behavior with regards to Transport Layer Packet transport.

Table 5-11. Transport Layer Behavior per Link State

Link State	Tunneled Packets and Control Packets	Credit Grant Packets	Credit Sync Packets	Time Sync Packets
Inactive	Shall not be sent to or received from the Logical Layer. Packets may be dropped by the transmitting Transport Layer.	Shall not be sent to or received from the Logical Layer.	Shall not be sent to or received from the Logical Layer.	Shall not be sent to or received from the Logical Layer.
Active	May be sent to Logical Layer and received from Logical Layer.	May be sent to Logical Layer and received from Logical Layer.	May be sent to Logical Layer and received from Logical Layer.	May be sent to Logical Layer and received from Logical Layer.
Low Power	Shall trigger transition to Active state.	Credit Grant Packets shall only be sent as a result of a the following: <ul style="list-style-type: none"> Increment on a packet dequeue. Update on a Credit Sync due to packet loss. Initial credits allocation to a Path. Sending a Credit Grant Packet shall trigger transition to Active state.	Shall not be sent.	Shall trigger transition to Active state in time to send the Time Sync Packet.
<i>Note: CLOs is a Low Power state. Transition to the Active Link state can only be initiated by the USB4 Port that has its Transmitter shut down.</i>				

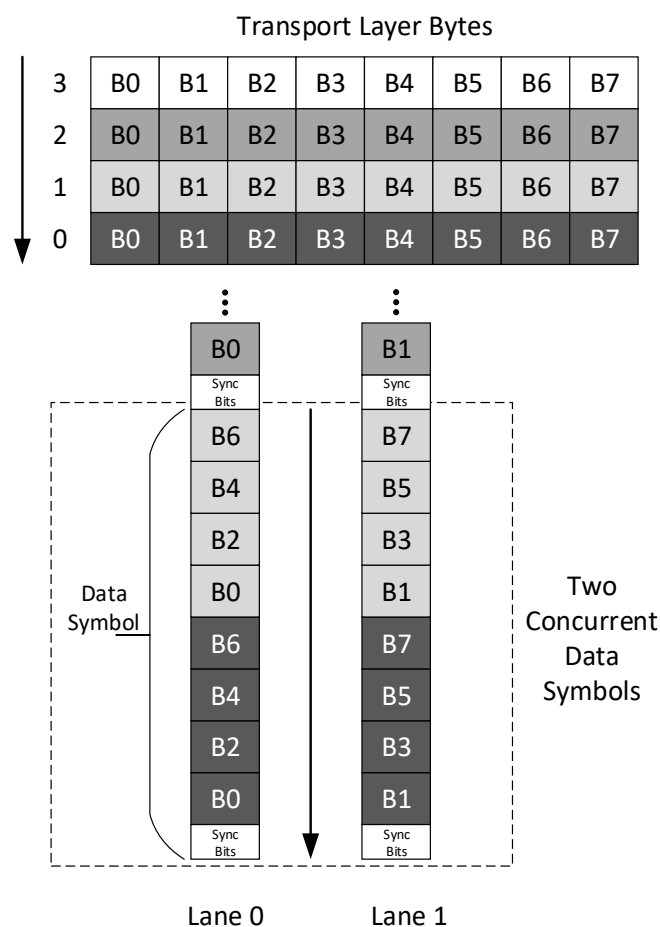
5.1.5 Minimum Headers Gap

For a Gen 2 or Gen 3 Link, a Router needs to maintain a minimum gap between two non-Idle Transport Layer Packet Headers. The size of the gap depends on the Link configuration. A Router shall insert Idle Packets to meet the requirements defined in Table 5-12. Figure 5-9 shows an example of two 64-bit Data Symbols sent concurrently with RS-FEC off.

There is no minimum gap between two non-Idle Transport Layer Packet Headers for a Gen 4 Link.

Table 5-12. Minimum Transport Layer Packet Header Gap Requirements

Link Configuration	Requirement
Gen 2, Single-Lane	A Router shall send no more than one non-Idle Transport Layer Packet Header in a 64-bit Data Symbol. <i>Note: This requirement is always satisfied, as the minimal length of a non-Idle Transport Layer Packet is 64 bits.</i>
Gen 2, Symmetric	A Router shall send no more than one non-Idle Transport Layer Packet Header in the two 64-bit Data Symbols that are sent concurrently on the two Lanes of a Symmetric Link.
Gen 3, Single-Lane	A Router shall send no more than one non-Idle Transport Layer Packet Header in a 128-bit Data Symbol.
Gen 3, Symmetric	A Router shall send no more than one non-Idle Transport Layer Packet Header in the two 128-bit Data Symbols that are sent concurrently on the two Lanes of a Symmetric Link.

Figure 5-9. Two Concurrent Data Symbols Example



IMPLEMENTATION NOTE

If a Router receives two or more Transport Layer Packet Headers that violate the rules defined in Table 5-12, it may drop any of the Transport Layer Packets.

5.2 Routing

The Path assigned to a Transport Layer Packet determines how that packet is routed through the USB4 Fabric. This section describes how Transport Layer Packets traverse a Path as forwarded by the Routers along that Path.

5.2.1 Adapter Numbering Rules

A Router can support up to 64 Adapters (including the Control Adapter). The following rules describe how the Adapters within a Router are numbered:

- Each Adapter shall be assigned a different 6-bit Adapter Number.
- The Control Adapter shall be assigned Adapter Number 0.
- For a Device Router, the Lane 0 Adapter in the Upstream Facing Port shall be assigned the lowest Adapter Number among all Lane Adapters.
- A USB4 Port shall have two Lane Adapters. The Lane Adapter Numbers within a USB4 Port shall be consecutive. The Lane 0 Adapter shall have a lower number than the Lane 1 Adapter.
- If a Router does not use an Adapter Number that is less than or equal to the *Max Adapter* field in the Router Configuration Space, the Router shall use one of the following methods to indicate that the Adapter is unused:
 - Assign a value of “Unsupported Adapter” to the *Adapter Type* field in the Adapter Configuration Space of the unused Adapter Number. In this case, the Adapter needs to implement the Basic Configuration Registers in its Adapter Configuration Space. It is recommended that a Router use this method.
 - Respond to a Read Request or Write Request that targets the Adapter Configuration Space of the unused Adapter with a Notification Packet with Event Code = ERR_ADDR. In this case, the unused Adapter is not required to implement an Adapter Configuration Space.

Note: A USB4 Product may contain additional unused Adapter Numbers as defined in the USB4 DROM Specification. In that case, the Router does not need to respond as defined above for an Unused Adapter Number.

- If a Device Router tunnels PCIe traffic, then the Upstream PCIe Adapter shall be assigned the lowest Adapter Number among all PCIe Adapters.
- If a Device Router tunnels USB3 traffic, then the Upstream USB3 Adapter shall be assigned the lowest Adapter Number among all USB3 Adapters.

5.2.2 HopID Rules

HopIDs are used by Routers to direct packets between Links on a Path. HopIDs are configured by the Connection Manager.



CONNECTION MANAGER NOTE

When setting up a Path, a Connection Manager sets the Output HopID field in the Path Configuration Space of the Ingress Adapter to allocate a HopID for that Path. The Output HopID in an Egress Adapter becomes the Input HopID of the next Ingress Adapter on the Path.

A Connection Manager shall follow the rules below when allocating HopID values in a Router:

- An Input HopID can only be used once per Ingress Adapter.
- A HopID can only be used once per Egress Adapter.
- An Output HopID can be used more than once in an Ingress Adapter as long as the Output HopID targets a different Egress Adapter.

For example, a Connection Manager can configure an Ingress Port with multiple Path entries that use Output HopID = 8, provided that the Output Adapter field for the Paths are different.

- The HopIDs for a Path can be different in each Router that the Path traverses.
- If the Egress Adapter is not a Host Interface Adapter:
 - Output HopID cannot be less than 8.
 - Output HopID cannot exceed the Max Output HopID field in the Adapter Configuration Space of the Egress Adapter.
 - If the Egress Adapter is a Lane Adapter, the Output HopID cannot exceed the Max Input HopID field in the Adapter Configuration Space of the next Ingress Adapter (i.e. the Adapter that will be receiving the packet from the Egress Adapter).
- If the Egress Adapter is a Host Interface Adapter:
 - Output HopID cannot be less than 1.
 - Output HopID cannot exceed the Max Input HopID field in the Adapter Configuration Space of the Host Interface Adapter.

5.2.3 Routing Tables

An Ingress Adapter uses a Routing Table to determine the Egress Adapter and Egress HopID values for a received Transport Layer Packet. The Routing Table contains an entry for each Ingress HopID that the Ingress Adapter supports. A Routing Table entry contains the Egress Adapter Number and the Egress HopID that correspond to the Ingress HopID. Figure 5-10 depicts a schematic structure of a Routing Table.

Figure 5-10. Routing Table

HopID = n*	Egress Adapter	Egress HopID
Ingress HopID →	.	.
	.	.
	.	.
HopID = Max Input HopID	Egress Adapter	Egress HopID

* The first HopID in the table is 1 for Host Interface Adapters and 8 otherwise

A Routing Table is populated according to the Path Configuration Space of the Ingress Adapter. For each Ingress HopID, the Path Configuration Space entry at offset (2 * Ingress HopID) is used as follows:

- The Egress Adapter in the Routing Table entry shall equal the *Output Adapter* field in the Path Configuration Space entry.
- The Egress HopID in the Routing Table entry shall equal the *Output HopID* field in the Path Configuration Space entry.

A Host Interface Adapter shall contain Routing Table entries for Ingress HopIDs 1 through *Max Input HopID*. All other Adapters shall contain Routing Table entries for Ingress HopIDs 8 through *Max Input HopID*.

5.2.4 Routing Rules

Each Ingress Adapter shall have its own Routing Table. For a Single-Lane Link, the Routing Table of the Ingress Adapter that a Transport Layer Packet arrives on shall be used to route the packet. For an Aggregated Link, the Routing Table of the Lane 0 Adapter of the Ingress Port that a Transport Layer Packet arrives on shall be used to route the packet.

5.2.4.1 Control Packets

Control Packets use HopID 0. A Lane Adapter and a Host Interface Adapter shall forward a Transport Layer Packet with a HopID value of 0 to the Control Adapter. The Control Adapter shall forward the packet to an Egress Adapter as defined in Section 6.4.3.2.

USB3 Adapters, PCIe Adapters, and DP Adapters do not send or receive Control Packets.

5.2.4.2 Link Management Packets

Link Management Packets use HopIDs 1 through 7 (inclusive). If the *SupplD* bit is set to 1b, Link Management Packets also use HopIDs greater than 7. Only Lane Adapters route Link Management Packets—a Protocol Adapter does not send or receive Link Management Packets.

The following rules determine how a Lane Adapter routes a Link Management Packet:

- A Transport Layer Packet with a HopID value of 1 shall be forwarded to the Transport Layer for credit management processing. It shall not be forwarded to an Egress Adapter.
- A Transport Layer Packet with a HopID value of 2 shall be dropped and no further action shall be taken on its behalf.
- A Transport Layer Packet with a HopID value of 3 shall be forwarded to the TMU. It shall not be forwarded to an Egress Adapter.
- A Transport Layer Packet with a HopID value of 4 through 7 (inclusive) shall be dropped and no further action shall be taken on its behalf.
- A Transport Layer Packet with a HopID value greater than 7 and the *SupplD* bit set to 1b shall be forwarded to the Transport Layer for credit management processing. It shall not be forwarded to an Egress Adapter.

5.2.4.3 Tunneled Packets

Tunneled Packets use HopIDs 8 through Max Input HopID (inclusive). For a Host Interface Adapter only, Tunneled Packets can also use HopIDs 1 through 7 (inclusive).

The following rules determine how an Ingress Adapter routes a Tunneled Packet:

- If the *Valid* bit in the Path Configuration Space for the Path of the packet is 0b, the packet shall be dropped and no further action shall be taken on its behalf.

- If the Transport Layer Packet has an Ingress HopID that is greater than the Max Input HopID of the Ingress Adapter, the packet shall be dropped and no further action shall be taken on its behalf.
- If the Routing Table entry corresponding to the Ingress HopID of the Transport Layer Packet contains an Egress HopID greater than the *Max Output HopID* of the Egress Adapter, the packet shall be dropped by the Router and no further action shall be taken on its behalf.
- If the Routing Table entry corresponding to the Ingress HopID of the Transport Layer Packet contains an Egress Adapter that is greater than the *Max Adapter* field in Router Configuration Space, the packet shall be dropped and no further action shall be taken on its behalf.
- Else, the Ingress Adapter shall:
 1. Replace the Ingress HopID value in the Tunneled Packet with the Egress HopID in the Routing Table entry that corresponds to the Ingress HopID.
 2. Update the *HEC* field in the Tunneled Packet.
 3. Forward the Tunneled Packet to the Egress Adapter in the Routing Table entry that corresponds to the Ingress HopID of the Tunneled Packet.

Unless specified otherwise, the Ingress Adapter shall not modify any additional fields (including Reserved fields).



CONNECTION MANAGER NOTE

The Routing Table entries for HopIDs greater than 7 are populated by the Connection Manager during Path setup by programming the Path Configuration Space of the Ingress Adapter.

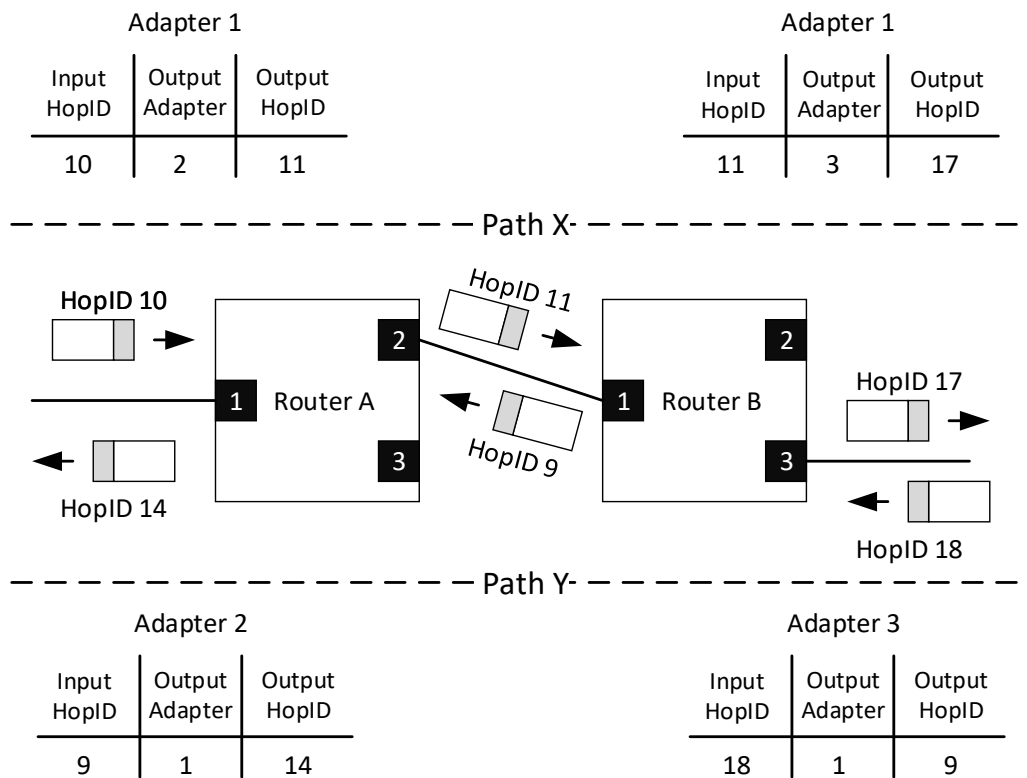
When configuring a Routing Table to direct outgoing traffic to an Aggregated Link, a Connection Manager shall use the Adapter Number of the Lane 0 Adapter associated with the Aggregated Link.

5.2.4.4 Routing Example

Figure 5-11 shows an example of how Routing Tables are used to route Transport Layer Packets along a Path. In the example, there are two Paths (one in each direction). The two Paths are independent of each other.

For Path X, a Router (not shown) injects a Transport Layer Packet onto Path X with a HopID of 10. The packet is received on Adapter 1 (Ingress Adapter) of Router A. Adapter 1 remaps the HopID to 11 and forwards the packet to Adapter 2 (Egress Adapter). The packet is then received on Adapter 1 (Ingress Adapter) of Router B. Adapter 1 remaps the HopID to 17 and forwards the packet to Adapter 3 (Egress Adapter).

For Path Y, a Router (not shown) injects a Transport Layer Packet onto Path Y with a HopID of 18. The packet is received on Adapter 3 (Ingress Adapter) of Router B. Adapter 3 remaps the HopID to 9 and forwards the packet to Adapter 1. The packet is then received on Adapter 2 (Ingress Adapter) of Router A. Adapter 2 remaps the HopID to 14 and forwards the packet to Adapter 1.

Figure 5-11. Routing Example

5.2.5 Connectivity Rules

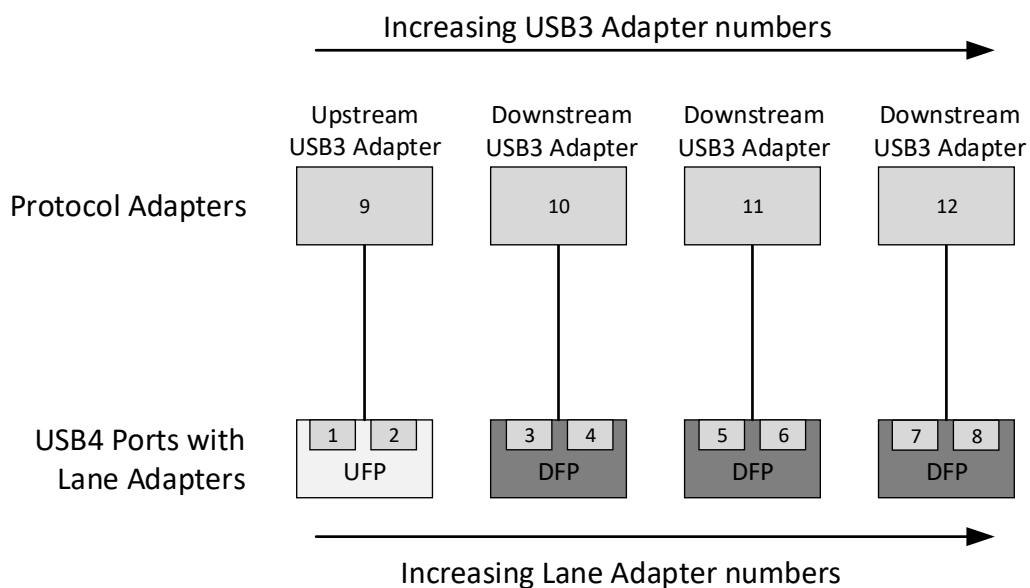
A Router shall be capable of forwarding packets as follows:

- A Router shall be able to forward a Control Packet received on any Lane 0 Adapter to the Control Adapter.
- A Router shall be able to forward a Control Packet from the Control Adapter to any Lane 0 Adapter.
- A Router shall be able to forward a Transport Layer Packet received on the Lane 0 Adapter of one USB4 Port to the Lane 0 Adapter of any other USB4 Port.
- A Host Router shall be able to forward a packet received on the Host Interface Adapter to the Control Adapter and to any Lane 0 Adapter.
- A Host Router shall be able to forward a packet received on any Lane 0 Adapter to the Host Interface Adapter.
- A Host Router shall be able to forward a packet from the Control Adapter to the Host Interface Adapter.
- A Router shall be able to forward a packet received on a DP IN Adapter to any Lane 0 Adapter.
- A Router shall be able to forward a packet received on a DP OUT Adapter to any Lane 0 Adapter.
- A Router shall be able to forward a packet received on a Lane 0 Adapter to any DP IN Adapter or any DP OUT Adapter.
- A Device Router shall be able to forward a packet received on the DP OUT AUX Adapter to the Upstream Adapter.

- A Device Router shall be able to forward a packet received on the Upstream Adapter to the DP OUT AUX Adapter.
- A Router shall be able to forward a packet received on an Upstream PCIe Adapter to the Upstream Adapter.
- A Router shall be able to forward a packet received on the Upstream Adapter to the Upstream PCIe Adapter.
- USB4 Ports and PCIe Adapters are paired in order of increasing Adapter Numbers. A Router shall be able to forward a packet received on the Lane 0 Adapter of a USB4 Port to the paired PCIe Adapter. A Router shall be able to forward a packet received on a PCIe Adapter to the Lane 0 Adapter of the paired USB4 Port.
- A Router shall be able to forward a packet received on an Upstream USB3 Adapter to the Upstream Adapter.
- A Router shall be able to forward a packet received on the Upstream Adapter to the Upstream USB3 Adapter.
- USB4 Ports and USB3 Gen X Adapters are paired in order of increasing Adapter Numbers. A Router shall be able to forward a packet received on the Lane 0 Adapter of a USB4 Port to the paired USB3 Gen X Adapter. A Router shall be able to forward a packet received on a USB3 Gen X Adapter to the Lane 0 Adapter of the paired USB4 Port.
- If the *Gen T Full Connectivity Support* bit in the Router Configuration space is set to 0b
 - USB4 Ports and USB3 Gen T Adapters are paired in order of increasing Adapter Numbers. A Router shall be able to forward a packet received on the Lane 0 Adapter of a USB4 Port to the paired USB3 Gen T Adapter. A Router shall be able to forward a packet received on a USB3 Gen T Adapter to the Lane 0 Adapter of the paired USB4 Port.
- Else
 - A Router shall be able to forward a packet received on the Lane 0 Adapter of a USB4 Port to any USB3 Gen T Adapter. A Router shall be able to forward a packet received on a USB3 Gen T Adapter to the Lane 0 Adapter of any USB4 Port.

Figure 5-12 depicts an example of a USB3 Adapter connectivity scheme in a Router with three Downstream Facing Ports. Connectivity for PCIe Adapters follows the same scheme.

Figure 5-12. Example of Connectivity for USB3 Adapters



Note: This section defines the minimum connectivity rules for a Router. A Router implementation may or may not offer additional connectivity. Router behavior is undefined if a Connection Manager configures a Path that assumes connectivity beyond what is defined in this specification.

5.3 Quality of Service (QOS)

5.3.1 Packet Ordering

A Router shall transmit Transport Layer Packets for a Path in the same order that they are received. The ordering of packets on a single Path is guaranteed. However, ordering of packets transmitted on multiple Paths is not guaranteed.

The ordering of Transport Layer Packets on one Path shall not affect the ordering of packets on any other Path.

5.3.2 Flow Control

The Transport Layer employs a per-Link, credit-based flow control mechanism to prevent overflowing the receive buffers due to congestion. Each enabled Path has its own flow control scheme. There are four flow control schemes defined in this specification:

- Flow Control Disabled – Transport Layer Packets are not flow controlled. An Ingress Adapter drops packets if there is insufficient space in the receive buffer.
- Dedicated Flow Control – The Ingress Adapter has buffer space allocated for the Path. The Egress Adapter can only send a Transport Layer Packet when the Ingress Adapter has space in the Path buffer.
- Shared Flow Control – The Ingress Adapter has a Shared Buffer for all Paths that use shared flow control. The Egress Adapter can only send a Transport Layer Packet when there is space in the Shared Buffer.
- Restricted Shared Flow Control – The Ingress Adapter uses the Shared Buffer (same as used for Shared Flow Control), but the Path can only use a limited amount of space in the Shared Buffer. The Egress Adapter can only send a Transport Layer Packet when there is space in the Shared Buffer and it has not exceeded its space in the Shared Buffer.

Flow control is managed individually for each Link. Flow control is managed by both the Ingress Adapter and the Egress Adapter at either end of a Link. Section 5.3.2.1 defines flow control management for an Ingress Adapter and Section 5.3.2.2 defines flow control management for an Egress Adapter.

Credits are used to track the number of Transport Layer Packets that an Ingress Adapter can receive. One credit corresponds to one Transport Layer Packet of up to the maximum size. For example, if an Ingress Adapter advertises three credits, it has buffer space to accept three maximum-sized Transport Layer Packets (even though the actual Transport Layer Packets it receives may be less than the maximum size).

Link Management Packets are not subject to flow control and shall not be stored in any of the Flow Control Buffers defined in this section.

**CONNECTION MANAGER NOTE**

For each enabled Path, the Connection Manager shall configure both ends of a Link to have the same flow control scheme.

A Connection Manager shall only use the Flow Control Disabled scheme for a DisplayPort Main-Link Path.

5.3.2.1 Ingress Adapter

The *IFC Flag* and *ISE Flag* fields in the Path Configuration Space determine which flow control scheme is used for a Path. Table 5-13 defines the flow control schemes that are used for each set of *IFC Flag* and *ISE Flag* values.

Table 5-13. Ingress Adapter Flow Control Schemes

Scheme	IFC Flag	ISE Flag
Flow Control Disabled	0b	0b
Dedicated Flow Control	1b	0b
Shared Flow Control	0b	1b
Restricted Shared Flow Control	1b	1b

An Ingress Adapter shall always use the Dedicated Flow Control scheme for a Path that corresponds to HopID 0 (i.e. for Control Packets).

All other Paths shall be configurable during Path Setup. A configurable Path shall use the flow control scheme as determined by the *IFC Flag* and *ISE Flag* fields.

5.3.2.1.1 Buffer Allocation

An Ingress Lane Adapter shall have a buffer space that is used exclusively for incoming packets. A Connection Manager can divide the buffer space into three types of buffers:

- A Flow Control Disabled Buffer that is used for Paths with Flow Control Disabled.
- A set of Dedicated Buffers for Paths that use the Dedicated Flow Control scheme. There shall be one Dedicated Buffer for each Path that uses the Dedicated Flow Control scheme.
- A Shared Buffer that is used for all Paths that use either the Shared Flow Control scheme or the Restricted Shared Flow Control scheme.

For a Single-Lane Link, the *Total Buffers* field in the Adapter Configuration Space of the Lane 0 Adapter contains the total size of the buffer space available to the Lane 0 Adapter. For an Aggregated Link, the *Total Buffers* field in the Adapter Configuration Space of the Lane 0 Adapter contains the total size of the buffer space for both Lane Adapters in the USB4 Port. When a USB4 Link transitions between an Symmetric Link and an Asymmetric Link, the *Total Buffers* field shall not change.

**CONNECTION MANAGER NOTE**

A Connection Manager uses the parameters provided by the Buffer Allocation Request Operation (defined in Section 8.3.1.3.4) to allocate Buffers for each Path. A Connection Manager can allocate buffer space up to what it reads from the Total Buffers field.

If a Connection Manager enables the Buffer Allocation per USB4 Port capability, it shall use the Buffer Allocation Request Router Operation to query the Lane 0 Adapter of a USB4 Port before setting up a Path through the Port.

A Router may implement a different number of buffers and a different buffer allocation scheme for each of its Ingress Lane Adapters. If a Router implements different buffer allocation schemes for its Ingress Adapters, it shall advertise its support for the *Buffer Allocation Per USB4 Port* capability (see Section 8.3.1.3.2).

Note: A Connection Manager that does not enable the Buffer Allocation Per USB4 Port feature issues a single Buffer Allocation Request Router Operation, which will be used as the allocation for all USB4 Ports.

Table 5-14 defines the buffer allocation parameters a Router reports through the Buffer Allocation Request Operation. See Appendix E for example buffer space calculations.

Table 5-14. Buffer Allocation Parameters

Name	Description	Egress Adapter	Requirements
baMaxUSB3GenX	The buffer allocation requested for a USB3 Gen X Path to achieve the maximum target bandwidth.	USB3 Gen X	Shall be present if Router has a USB3 Gen X Adapter.
baMinDPaux	The minimum buffer allocation requested for each Egress Adapter.	Lane or DP	Shall be present if Router has a DP Adapter or multiple USB4 Ports.
baMinDPmain	The minimum buffer allocation requested for each DP Main-Link Path.	Lane or DP OUT	Shall be present if Router has a DP OUT Adapter or multiple USB4 Ports.
baMaxPCle	The buffer allocation requested for a PCle Path to achieve the maximum target bandwidth.	PCle	Shall be present if Router has a PCle Adapter.
baMaxHI	The buffer allocation requested for the sum of all Host Interface Paths to achieve the maximum target bandwidth.	HI	Shall be present if Router is a Host Router.
baMaxUSB3GenT	The buffer allocation requested, for the sum of all USB3 Gen T Paths through a USB4 Port, to achieve the maximum target bandwidth.	USB3 Gen T	Shall be present if Router has a USB3 Gen T Adapter.



CONNECTION MANAGER NOTE

A Connection Manager shall not set up a DP Path if it cannot allocate at least baMinDPmain buffers for the DP Main-Link Path and at least baMinDPaux buffers for the DP AUX Path.

It is recommended that a Connection Manager allocate the maximum available number of buffers for a Gen X Path, not exceeding baMaxUSB3GenX. However, the Connection Manager may setup a USB3 Gen X Path with less buffers as long as the number of buffers supports a minimal bandwidth of 1.5 Gbps.

It is recommended that a Connection Manager allocate the maximum available number of buffers for the Gen T Paths, not exceeding baMaxUSB3GenT. However, the Connection Manager may setup the USB3 Gen T Paths with less buffers as long as the number of buffers supports a minimal bandwidth of 1.5 Gbps for each supported Gen T Path.

The Connection Manager may set up PCle and HI Paths with less than the maximum requested buffers.

5.3.2.1.1.1 Flow Control Disabled Buffer

An Ingress Adapter shall store Transport Layer Packets arriving on Paths that use the Flow Control Disabled scheme in the Flow Control Disabled Buffer.

The Flow Control Disabled Buffer shall be the size set in the *Non Flow Controlled Buffers* field in Adapter Configuration Space.

5.3.2.1.1.2 Dedicated Flow Control Buffer

If a Path is defined with the Dedicated Flow Control Buffer scheme, an Ingress Adapter shall store any Transport Layer Packets arriving on that Path in the Dedicated Buffer for that Path.

A Dedicated Buffer shall be the size set in the *Path Credits Allocated* field in the Path Configuration Space.

5.3.2.1.1.3 Shared Flow Control Buffer

If a Path is defined with the Shared Flow Control Buffer scheme, an Ingress Adapter shall store any Transport Layer Packets arriving on that Path in the Shared Buffer.

The size of the Shared Buffer shall be the size set in the *Link Credits Allocated* field in Adapter Configuration Space.

5.3.2.1.1.4 Restricted Shared Flow Control Buffer

If a Path is defined with the Restricted Shared Flow Control Buffer scheme, an Ingress Adapter shall store any packets arriving on that Path in the Shared Buffer. The Path shall not use more space in the Shared Buffer than is set forth in the *Path Credits Allocated* field in the Path Configuration Space.

5.3.2.1.2 Credit Tracking

The following Rules apply for an Ingress Adapter tracking credits:

- If the *IFC Flag* field is set to 0b, credits shall not be tracked for the Path.
- If the *IFC Flag* field is set to 1b, credits shall be tracked for the Path.
- If the *ISE Flag* field is set to 0b, credits shall not be tracked for the Path in the Shared Buffer.
- If the *ISE Flag* field is set to 1b, credits shall be tracked for the Path in the Shared Buffers.
- For each Path with the *IFC Flag* field set to 1b, the Ingress Adapter shall initially allocate the number of credits specified in the *Path Credits Allocated* field in the Path Configuration Space.
 - The Path corresponding to HopID 0 shall be provisioned with at least 2 initial credits.
- For the Shared Buffer, if the *Shared Buffering Capable* bit is set to 1b, the Ingress Adapter shall initially allocate the number of credits in the *Link Credits Allocated* field in the Adapter Configuration Space.

If an Ingress Adapter receives a packet on a flow controlled Path and the appropriate buffer (Dedicated or Shared) has no space for the packet, then the packet shall be discarded, the *Flow Control Error* bit in Adapter Configuration Space shall be set to 1b, and the flow control state shall not be affected. If the *Flow Control Error Enable* bit in the Adapter Configuration Space is 1b, then a Notification Packet with Event Code = ERR_FC shall be sent upstream (see Section 6.5 for more information).

- Each Ingress Adapter shall track credits individually for its Shared Buffer and all of its Dedicated Buffers.
- When an Ingress Adapter drops a packet (e.g. due to a HEC error), it shall not account for the dropped packet in its credit tracking counters.

- Link Management Packets shall not cause credit counts to increment or decrement when received.

It is recommended that the following state variables be used to track credits for Paths with the *IFC Flag* field set to 1b. Credits are tracked individually for each Path. Other implementations are possible as long as credit tracking and synchronization are maintained.

- Path Credits Received (PCR)
 - Contains the total number (modulo 256) of Transport Layer Packets received on the Path since initialization.
 - Set to 0 upon Path setup.

Note: Path 0 is set up upon exit from CLd state.

- Incremented when a Transport Layer Packet is received on the Path: $PCR = (PCR + 1) \bmod 256$.
 - When a Path Credit Sync Packet is consumed, and after the PCA counter is updated (see below), the PCR counter is updated as follows: PCR = PCC value from the Path Credit Sync Packet.

- Path Credits Allocated (PCA)
 - Contains the total number (modulo 256) of credits allocated to Path since initialization.
 - Upon Path setup, set to the value in the *Path Credits Allocated* field in the Path Configuration Space.

Note: Path 0 is set up upon exit from CLd state.

- Included in the *Credits* field of a Credit Grant Record for the Path each time a Credit Grant Packet is sent.
 - Incremented when a Transport Layer Packet is dequeued from the Adapter buffers: $PCA = (PCA + 1) \bmod 256$.
 - Each time a Path Credit Sync Packet is consumed, the PCA counter is updated as follows:
 - $PCA = (PCA + (PCC \text{ value from the Path Credit Sync Packet} - PCR + 256)) \bmod 256$.

It is recommended that the following state variables be used to track credits for Paths with the *ISE Flag* field set to 1b. Credits are shared between Paths and tracked per Adapter. Other implementations are possible as long as credit tracking and synchronization are maintained.

- Shared Credits Received (SCR)
 - Contains the total number (modulo 256) of Transport Layer Packets received on all Paths with the *ISE Flag* field set to 1b.
 - Set to 0 when the first shared Path is set up.
 - Only valid when the *Shared Buffering Capable* bit is set to 1b.
 - Incremented when a Transport Layer Packet is received on a Path with *ISE Flag* field set to 1b: $SCR = (SCR + 1) \bmod 256$.
 - When a Shared Credits Sync Packet is consumed, and after the SCA counter is updated (see below), the SCR counter is updated as follows: SCR = SCC value from the Shared Credit Sync Packet.
- Shared Credits Allocated (SCA)
 - Contains the total number (modulo 256) of credits allocated to the Shared Buffers since initialization.

- Only valid when the *Shared Buffering Capable* bit is set to 1b.
- Set to the value in the *Link Credits Allocated* field when either of the following occur:
 - The value in the *Link Credits Allocated* field changes.
 - The first Path that uses shared flow control is set up.
- Included in the *Credits* field of a Credit Grant Record for the Shared Buffer when a Credit Grant Packet is sent.
- Incremented when a Transport Layer Packet is dequeued from the Shared Buffer and the *ISE Flag* field for the Path is set: $SCA = (SCA + 1) \bmod 256$.
- When a Shared Credits Sync Packet is consumed, the SCA counter is updated as follows:
 - $SCA = (SCA + (SCC \text{ value from the Shared Credit Sync Packet} - SCR + 256)) \bmod 256$.



CONNECTION MANAGER NOTE

A Connection Manager shall not change the Link Credits Allocated field in Adapter Configuration Space if there is an enabled Path with the ISE Flag field set to 1b.

5.3.2.1.3 Credit Grant Packets

Credit information is transferred from an Ingress Adapter to an Egress Adapter using Credit Grant Packets. An Ingress Adapter shall send Credit Grant Packets according to the following rules:

- If the *IFC Flag* field in the Path Configuration Space is set to 0b, Credit Grant Packets shall not be sent for the Path.
- If the *IFC Flag* field in the Path Configuration Space is set to 1b for a Path, an Ingress Adapter shall send Credit Grant Packets for that Path after Transport Layer Packets are dequeued. The policy for how frequently to send Credit Grant Packets after Transport Layer Packets are dequeued is implementation specific.
- If the *IFC Flag* field in the Path Configuration Space is set to 1b, an Ingress Adapter shall send a Credit Grant Packet with a Credit Grant Record for the Path when the Path is first enabled.
- If the *ISE Flag* field in the Path Configuration Space is set to 0b, the Path shall not affect Credit Grant Packets sent for the Shared Flow Control Buffer.
- If an Ingress Adapter has a Path with the *ISE Flag* field in the Path Configuration Space set to 1b, the Ingress Adapter shall send Credit Grant Packets for its Shared Flow Control Buffer after Transport Layer Packets are dequeued. The policy for how frequently to send Credit Grant Packets after Transport Layer Packets are dequeued is implementation specific.
- If the *ISE Flag* field in the Path Configuration Space is set to 1b, an Ingress Adapter shall send a Credit Grant Packet with a Credit Grant Record for the Shared Buffer when the Path is first enabled.
- When the Link is in the Active state, an Ingress Adapter sends Credit Grant Packets for its Shared Buffer and all of its Dedicated Buffers. Credit Grant Packets shall be sent at least every tCredits.
- When the Link is in a Low Power state, an Ingress Adapter sends Credit Grant Packets as defined in Table 5-11.

Note: Sending a Credit Grant Packet causes the Link to transition to the Active State

- When a Link first becomes Active, an Ingress Adapter that is a Lane 0 Adapter shall send a Credit Grant Packet with a Credit Grant Record for HopID 0.



IMPLEMENTATION NOTE

If a Router does not send a Credit Grant Packet immediately after a Transport Layer Packet is dequeued, it is recommended that the Ingress Adapter buffers be sized to compensate for the delay.

An Egress Adapter shall process Credit Grant Packets in the order that they are received. Each Credit Grant packet shall be processed as follows:

- The Egress Adapter shall verify the *ECC* field value in the Credit Grant Record:
 - The Egress Adapter shall correct any single-bit errors. After correcting an error, the Egress Adapter shall continue on as if the error had never occurred.
 - If an uncorrectable error is detected, the Credit Grant Record shall be dropped, and the *ECC Error* field in the Adapter Configuration Registers shall be incremented.
- If the HopID in a Credit Grant Record does not match an enabled Path in the Egress Adapter, the Credit Grant Record shall be dropped and no further actions shall be taken.
- Section 5.3.2.2.1 describes how the information in a Credit Grant Record is used.

In order to assure minimum bandwidth, the round trip delay between sending a Credit Grant Packet to getting the next Tunneled Packet needs to be bounded. If an Egress Adapter is not transmitting Tunneled Packets due to a lack of credits, a Router shall send a Tunneled Packet for a Path when the Egress Adapter receives a Credit Grant Record for the Path and the Credit Grant Record contains an advanced PCA. Unless another packet or Ordered Set is transmitted in the interim or the USB4 Link is in the middle of a Link Transition, the Tunneled Packet shall be sent within tCGtoPkt_Gen3 (for a Gen 3 Link) or tCGtoPkt_Gen4 (for a Gen 4 Link) time after receiving the Credit Grant Packet. The time is measured on the USB Type-C connector from the first received bit of the Credit Grant Record to the first transmitted bit of the Tunnel Packet.

5.3.2.2 Egress Adapter

Table 5-15 defines the flow control schemes for an Egress Adapter. The *EFC Flag* and *ESE Flag* fields in the Path Configuration Space determine which flow control scheme is used for a Path.

Table 5-15. Egress Adapter Flow Control Schemes

Scheme	EFC Flag	ESE Flag
Flow Control Disabled	0b	0b
Dedicated Flow Control	1b	0b
Shared Flow Control	0b	1b
Restricted Shared Flow Control	1b	1b

The Path corresponding to HopID 0 shall always use the Dedicated Flow Control scheme. For an Adapter that is not a Host Interface Adapter, the Paths that correspond to Paths 1 through 7 shall always use the Flow Control Disabled scheme. All other Paths are configurable and shall use the flow control scheme that corresponds to the *EFC Flag* and *ESE Flag* fields in the Path Configuration Space.

5.3.2.2.1 Credit Tracking

It is recommended that the following state variables be used to track credits for a Path with the *EFC Flag* field set to 1b. Credits are tracked individually for each Path. Other implementations are possible as long as credit tracking and synchronization are maintained.

- Path Credits Consumed (PCC)
 - Contains a count (modulo 256) of the total number of credits consumed by Transport Layer Packet transmissions on the Path since the Path was initialized.
 - Set to 0 upon Path setup.

Note: Path 0 is set up upon exit from CLd state.

- Incremented each time a Transport Layer Packet is transmitted over the Path:
 $PCC = (PCC + 1) \bmod 256$.
- Path Credit Limit (PCL)
 - Contains the most recent number of credits advertised by the Ingress Adapter for the Path.
 - Set to 0 upon Path setup.

Note: Path 0 is set up upon exit from CLd state.

- Updated each time a Credit Grant Record is received for the Path by overwriting with the value contained in the *Credits* field.

It is recommended that the following state variables be used to track credits for Paths with the *ESE Flag* field set to 1b. Credits are shared between Paths and tracked per Adapter. Other implementations are possible as long as credit tracking and synchronization are maintained.

- Shared Credits Consumed (SCC)
 - Contains a count (modulo 256) of the total number of credits consumed by Transport Layer Packet transmissions on Paths with the *ESE Flag* field enabled.
 - Set to 0 when the first shared Path is set up.
 - Incremented each time a Transport Layer Packet is transmitted over a Path that has the *ESE Flag* field enabled: $SCC = (SCC + 1) \bmod 256$.
- Shared Credit Limit (SCL)
 - Contains the most recent number of credits advertised by the Ingress Adapter for the Shared Buffers.
 - Set to 0 when the first shared Path is set up.
 - Updated each time a Credit Grant Record is received with a record for the Shared Buffer by overwriting with the value contained in the *Credits* field.

5.3.2.2.2 Transmission Rules

If a Path uses the Flow Control Disabled scheme (*EFC* = 0b and *ESE* = 0b), then the Egress Adapter shall not require any credits to transmit a Transport Layer Packet on that Path.

If a Path uses the Dedicated Flow Control scheme (*EFC* = 1b and *ESE* = 0b), then the Egress Adapter shall require the following condition to be true before transmitting a Transport Layer packet on the Path:

- $[(PCL - PCC > 0) \text{ and } (PCL - PCC < 128)] \text{ or } [(PCL - PCC < 0) \text{ and } (PCC - PCL > 128)]$.

If a Path uses the Shared Flow Control scheme (*EFC* = 0b and *ESE* = 1b), then the Egress Adapter shall require the following condition to be true before transmitting a Transport Layer packet on the Path:

- $[(SCL-SCC > 0) \text{ and } (SCL-SCC < 128)] \text{ or } [(SCL-SCC < 0) \text{ and } (SCC-SCL > 128)]$.

If a Path uses the Restricted Shared Flow Control scheme ($EFC = 1b$ and $ESE = 1b$), then the Egress Adapter shall require both of the following conditions be true before transmitting a Transport Layer packet on the Path:

- $[(PCL-PCC > 0) \text{ and } (PCL-PCC < 128)] \text{ or } [(PCL-PCC < 0) \text{ and } (PCC-PCL > 128)]$.
- $[(SCL-SCC > 0) \text{ and } (SCL-SCC < 128)] \text{ or } [(SCL-SCC < 0) \text{ and } (SCC-SCL > 128)]$.

5.3.2.3 Credit Counter Synchronization

If a flow controlled Transport Layer Packet is dropped or otherwise lost for any reason, the Egress Adapter credit counters lose synchronization with the Ingress Adapter. In order to re-establish synchronization, an Egress Adapter sends Credit Sync Packets periodically to the Ingress Adapter.

There are two types of Credit Sync Packets: Path Credit Sync Packets, which are defined in Section 5.1.3.3.3, and Shared Buffers Credit Sync Packets, which are defined in Section 5.1.3.3.4.

An Egress Adapter shall send Credit Sync Packets according to the following rules:

- An Egress Adapter shall send a Path Credit Sync Packet every $tSync$ for a Path with the *Egress Flow Control (EFC) Flag* field set to 1b and the *Valid* bit set to 1b.
- If the *Egress Shared Buffering Enable (ESE) Flag* field in the Path Configuration Space is set to 1b for at least one enabled Path, an Egress Adapter shall send a Shared Buffers Credit Sync Packet every $tSync$.
- The credit count in the *PCC* field of a Path Credit Sync Packet shall be based on the number of flow controlled Transport Layer Packets sent on the Path prior to the Path Credit Sync Packet and shall not include flow controlled Transport Layer Packets which have not yet been sent.
- The credit count in the *SCC* field of a Shared Credit Sync Packet shall be based on the number of Transport Layer Packets sent on all Paths that use the Shared Buffer prior to the Shared Credit Sync Packet and shall not include Transport Layer Packets which have not yet been sent.
- An Egress Adapter shall not send Path Credit Sync Packets for a Path that uses the Flow Control Disable scheme.
- An Egress Adapter shall not send a Credit Sync Packet while in a Low Power state.

Note: When an Egress Adapter transitions back to the CL0 state after recovering from an error, it is recommended that the Egress Adapter send a Credit Sync Packet for each enabled Path that uses flow control.



IMPLEMENTATION NOTE

Restart the $tSync$ counter by the Egress Adapter after every CLx exit may lead to undesired behavior in which a Path Credit Sync Packet will not be sent for a long duration.

When an Ingress Adapter receives a Credit Sync Packet, it shall verify the *ECC* field value in the Credit Sync Packet payload as follows:

- The Ingress Adapter shall correct any single-bit errors. After correcting an error, the Ingress Adapter shall continue on as if the error had never occurred.
- If an uncorrectable error is detected, the Credit Sync Packet shall be dropped, and the *ECC Error* field in the Adapter Configuration Registers shall be incremented.

5.3.3 Bandwidth Arbitration and Priority

Bandwidth arbitration and prioritization of traffic in a Domain is done in a distributed manner. Each Egress Adapter contains a configurable traffic manager that does bandwidth arbitration and prioritization for all Paths that traverse the Adapter. The traffic manager is configured during Path setup.

A Router shall enable bandwidth arbitration for a given Path when the *Valid* bit in the Path Configuration Space is set to 1b.



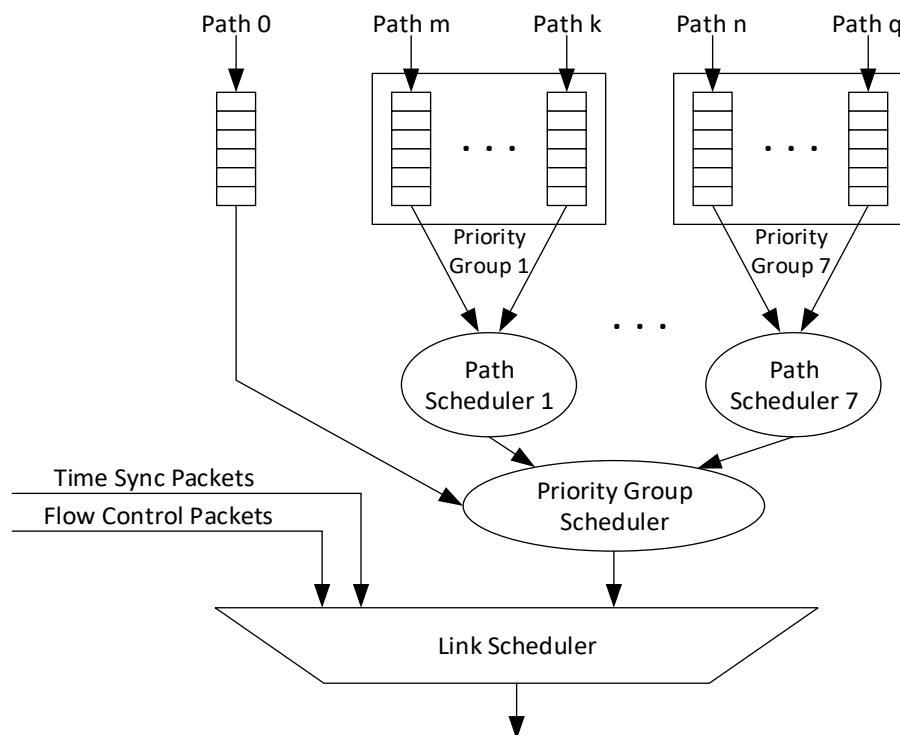
IMPLEMENTATION NOTE

The Priority field in a Path Configuration Space is global to a Router. It can be used to determine the priority between queues in an Ingress Adapter, between different Ingress Adapters, between different Egress Adapters, and within each Egress Adapter.

5.3.3.1 Scheduling

The traffic manager for an Egress Adapter shall use the 3-layer scheduling scheme described in this section to schedule outgoing packets. This scheme is summarized in Figure 5-13.

Figure 5-13. Egress Adapter Scheduler



5.3.3.1.1 Path Schedulers

The first layer of the traffic manager consists of several schedulers (called Path Schedulers) that prioritize traffic for a given Priority Group. A Priority Group is a set of Paths that share the same scheduling priority value. A Path is assigned a scheduling priority value by writing to the *Priority* field in the Path Configuration Space.

There shall be one Path Scheduler for each Priority Group. A Path Scheduler operates according to the following rules:

- A weighted round-robin (WRR) scheduling scheme shall be implemented among the Paths that share the same Priority Group.
- The weight assigned to a Path shall be determined by the *Weight* field in the Path Configuration Space.
- When the *Weight* field changes for an enabled Path, the Path Scheduler shall use the new weight.
- The Path Scheduler shall support weights in the range of 1-15.
- The Path Scheduler shall schedule packets such that the total number of packet header and payload bytes scheduled for each Path within the Priority Group is proportional to the weight assigned to that Path with 10% maximum deviation over a measurement period of 1 ms, assuming each Path in the Priority Group is either delivering packets throughout the 1 ms period or is idle throughout the 1 ms period, and that sufficient credits are available for each Path in the Priority Group.

A Path Scheduler in a Host Router that sets the *Gen T Bundle Weight Mode* bit to 1b operates with the following additional rules and changes for USB3 Gen T Paths:

- The shared weight assigned to all the USB3 Gen T Paths shall be determined by the *Bundle Weight* field in the USB4 Port Capability Fields.
- When the *Bundle Weight* field changes, the Path Scheduler shall use the new shared weight.
- The Path Scheduler shall support weights in the range of 1-255 for the shared weight of the USB3 Gen T Paths.
- The Path Scheduler shall schedule packets such that the total number of packet header and payload bytes scheduled for all the USB3 Gen T Paths together is proportional to the shared weight assigned in the *Bundle Weight* field with 10% maximum deviation over a measurement period of 1 ms.

Note: When the Gen T Bundle Weight Mode bit is set to 1b, the Path scheduling scheme between individual USB3 Gen T Paths is implementation specific.



IMPLEMENTATION NOTE

A common practice is to allocate a quota (in some multiplicity of bytes) to each Path in the Priority Group. The quota for each Path is proportional to the weight assigned to the Path in the Path Configuration Space. It is recommended that the Path Scheduler minimize the quota allocated to each Path within a Priority Group such that the ratio of quota between any two Paths is equal to the ratio of the weights between the Paths and the quota for each Path is enough to schedule at least one Packet of maximum length.

The method for interleaving packets from different Paths within a Priority Group is vendor defined. In order to reduce the latency incurred by arbitration on any specific Path, it is recommended that the scheduler minimizes the number of packets scheduled in a row from a single Path.

HopID 0 traffic shall be assigned to Priority Group 0. No other traffic shall be assigned to Priority Group 0.



CONNECTION MANAGER NOTE

When assigning weights to USB3 Paths and to PCIe Paths, a Ver. 2 Connection Manager shall allocate at least 1.5Gbps bandwidth to each of these Paths. Allocating a minimum bandwidth to a Path ensures that its latency does not exceed the maximum value defined by the implementation.

5.3.3.1.2 Priority Group Scheduler

The second layer of the traffic manager consists of a Priority Group Scheduler that prioritizes traffic from each of the Path Schedulers. The Priority Group Scheduler shall employ a strict priority scheme between the eight Priority Groups, where Priority Group 0 has the highest priority and Priority Group 7 has the lowest priority. A request for scheduling by a higher Priority Group always takes precedence over requests of lower Priority Groups.

5.3.3.1.3 Link Scheduler

The Third Layer of the traffic manager consists of a Link Scheduler that multiplexes traffic from the Priority Group Scheduler with other packets generated within the Transport Layer. The Link Scheduler shall schedule traffic according to a strict priority scheme where the following priorities (from highest to lowest) are observed:

- Flow Control Packets.
- Time Sync Packets.
- Packets from the Priority Group Scheduler.

5.3.4 Packet Forwarding Delay and Packet Forwarding Delay Jitter

When a Router routes a Tunneled Packet along a Path, from an Ingress Adapter to an Egress Adapter, it generates a Packet Forwarding Delay (PFD) and PFD Jitter. The PFD is the delay between the time when the last bit of a Tunneled Packet is received at the Ingress Adapter to the time when the first bit of the Tunneled Packet is sent by the Egress Adapter.

When operating at Gen 3 or Gen 4 speeds, for a Tunneled Packet that is forwarded directly from a Router's ingress USB4 Port to one of its egress USB4 Ports, the Packet Forwarding Delay in the Router shall not exceed t_{PktFwd} . t_{PktFwd} does not apply when the received Tunneled Packet is forwarded to a Protocol Adapter in the Router. The time is measured on the USB Type-C connector from the first received bit of the Tunnel Packet to the first transmitted bit of the Tunnel Packet.

The PFD Jitter is the difference between the maximum and the minimum PFD between two Adapters along a Path in a Router. The PFD Jitter in a Router shall be no more than $t_{TunneledPacketJitter}$.

Note: PFD Jitter and t_{PktFwd} do not include the additional delay due to another Transport Layer Packet or Ordered Set having priority in being transmitted. They also do not include the delay in transmission due to insufficient flow control credits.

5.4 Path Teardown

A Connection Manager tears down a Path starting from the Destination Adapter and ending with the Source Adapter. A Connection Manager initiates Path teardown by setting the *Valid* bit in Path Configuration Space to 0b. After the *Valid* bit in a Path Configuration Space changes from 1b to 0b, a Router shall respond to the Write Request that sets the *Valid* bit to 0b and then tear down the Path at its Egress Adapter and Ingress Adapter.

Section 5.4.1 describes the flow for tearing down a Path in the Egress Adapter. Section 5.4.2 describes the flow for tearing down a Path in the Ingress Adapter.

Note: The Ingress Adapter and the Egress Adapter mentioned in this section refer to Adapters in the same Router.

Note: The Path teardown flows described in this section are applicable for all type of Adapters. The rules that involve Credits are applicable for Lane Adapters only.

**IMPLEMENTATION NOTE**

When the Valid bit is set to 0b in a Path Configuration Space, the Path configuration registers become stale, as well as the Paths credit management state. Therefore, a Packet that has not been dequeued, or has been dequeued but did not consume a credit yet is dropped and not transmitted. A Packet that has been dequeued from the flow control buffers, and has already consumed a credit by the Egress arbiter, may be transmitted.

5.4.1 Egress Adapter

For the Egress Adapter of the Path being torn down, a Router shall perform the following steps in the order listed:

1. If the *ESE Flag* field in the Path Configuration Space is set to 1b for the Path and besides the Path being torn down there is additional enabled Path with its *ESE Flag* set to 1b, then the Router shall send a Shared Buffers Credit Sync Packet to the Link Partner.
2. While the *Valid* bit in the Path Configuration Space is 0b:
 - The Router shall not send any Path Credit Sync Packets for the Path.
 - The Router shall ignore any Path credit updates for the Path received on the Egress Adapter.
3. The Router may transmit packets on the Path when the *Pending Packets* bit in the Path Configuration Space is set to 1b and for tTeardown after the Router sets the *Pending Packets* bit to 0b.
4. After tTeardown time, the Router shall discard any remaining packets for the Path.
5. The Router shall block the transmission of any packets on the Path after tTeardown has elapsed since it set the *Pending Packets* bit to 0b and until the *Valid* bit in the Path Configuration Space is set again to 1b.

**CONNECTION MANAGER NOTE**

A Connection Manager shall wait at least tTeardown time after a Router sets the Pending Packets bit to 0b before setting the Valid bit for the Path to 1b again.

5.4.2 Ingress Adapter

For the Ingress Adapter of the Path being torn down, a Router shall perform the following steps in the order listed:

1. The Router shall drop any packets received on the Path after the *Valid* bit is set to 0b.
2. The Router shall dequeue all packets for the Path that are queued in the flow control buffers. The Router may transmit a dequeued packet as a whole on its designated Egress Adapter or it may discard the packet. A Router shall not transmit a partial packet.
 - If the *ISE Flag* field in the Path Configuration Space is set to 1b, the Ingress Adapter shall continue to increment the SCA state variable and send Credit Grant Packets. The SCA variable shall increment each time a packet is dequeued, regardless of whether the packet was discarded or transmitted.
3. While the *Valid* bit in the Path Configuration Space is 0b:
 - The Router shall discard any Path Credit Sync Packets received for the Path.
 - The Router shall stop sending Path credits updates for the Path.

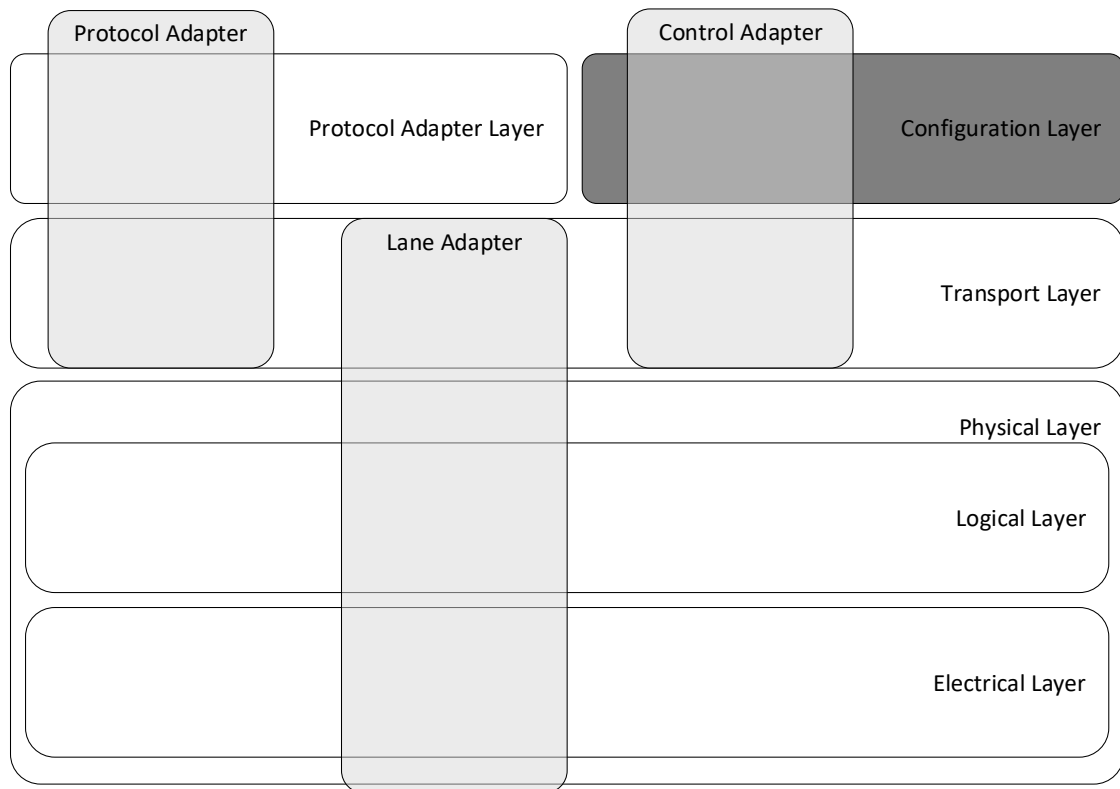
5.5 Timing Parameters

Table 5-16 lists the timing parameters for the Transport Layer.

Table 5-16. Transport Layer Timing Parameters

Parameter	Description	Min	Max	Units
tSync	The time interval at which Credit Sync Packets are periodically sent for a Path.	--	64	ms
tCredits	The time interval at which an Ingress Adapter sends Credit Grant Records for a Path.	--	200	μs
tTeardown	Duration during which packet transmission is permitted on a removed Path after the <i>Pending Packets</i> bit was set to 0b.	--	2	μs
tTunneledPacketJitter	The maximum PFD jitter of Tunneled Packets in a Router.	--	100	ns
tCGtoPkt_Gen3	The maximum time between receiving a Credit Grant Packet and sending a Tunneled Packet, assuming the Tunneled Packet is available and was originally not sent due to a lack of credits. This parameter only applies to a Gen 3 Link.	--	650	ns
tCGtoPkt_Gen4	The maximum time between receiving a Credit Grant Packet and sending a Tunneled Packet, assuming the Tunneled Packet is available and was originally not sent due to a lack of credits. This parameter only applies to a Gen 4 Link while the link is not in the middle of link transitions. Note: It is recommended for a Host Router not to exceed 550nSec	--	550 (Device Router) 700 (Host Router)	ns
tPktFwd	The maximum time for a Router to forward a Tunneled Packet from one USB4 Port to another USB4 Port. This parameter only applies to a USB4 Hub that is acting as a “pass through” for Tunneled Protocol traffic. It only applies when the Links are operating at Gen 3 or Gen 4 speeds.	--	550	ns

6 Configuration Layer



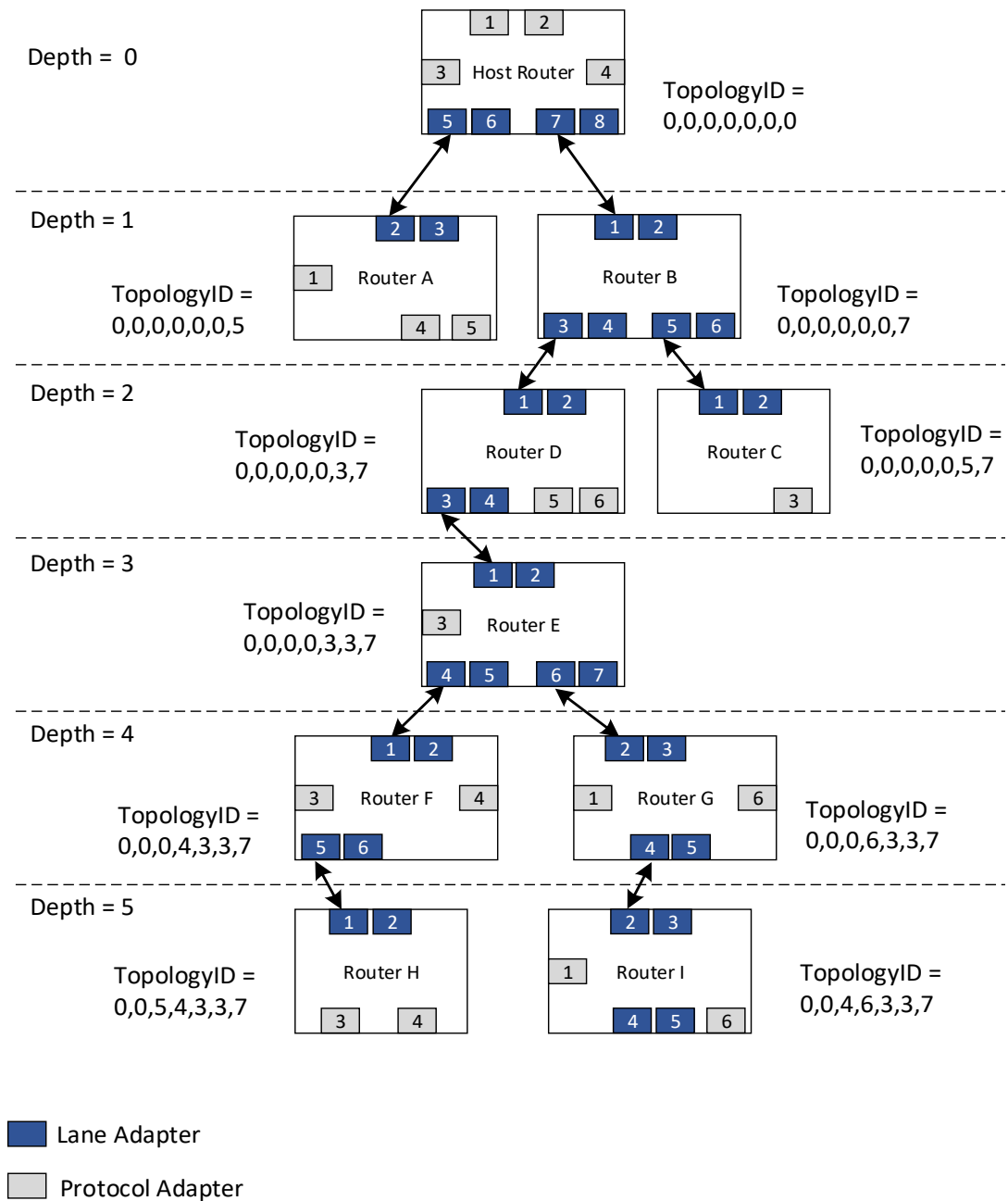
6.1 Domain Topology

A Spanning Tree contains up to six levels (depths 0 through 5). The Host Router is at the top of the Spanning Tree (depth = 0). Device Routers are connected at depths 1 through 5 (inclusive). A Connection Manager accesses a Domain through the Host Router of that Domain.

6.2 Router Addressing

A Connection Manager assigns each Router in its Domain a unique topological address called a TopologyID. The TopologyID represents the position of the Router within the Domain's Spanning Tree.

The TopologyID is a sequence of seven Adapter Numbers representing a Lane 0 Adapter in the Downstream Facing Ports at each level of the Spanning Tree between the Host Router and the Router. The TopologyID of a Host Router is always 0,0,0,0,0,0,0. The TopologyID for a Device Router at depth X (where X is from 1 to 5) is denoted as 0,...,0,P_{X-1},P_{X-2},...,P₀ where P_n is the Adapter Number of the Adapter in the Downstream Facing Port at level n. Figure 6-1 shows an example of a Spanning Tree along with the assignment of TopologyID values to each Router.

Figure 6-1. Example of TopologyID Assignment

6.3 Router States

Figure 6-2 describes a Host Router state machine.

Figure 6-2. Host Router State Machine

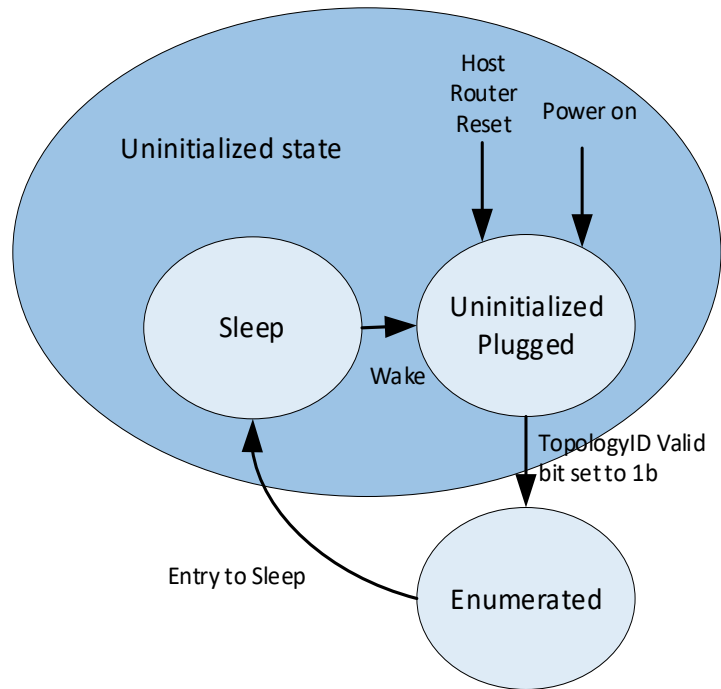
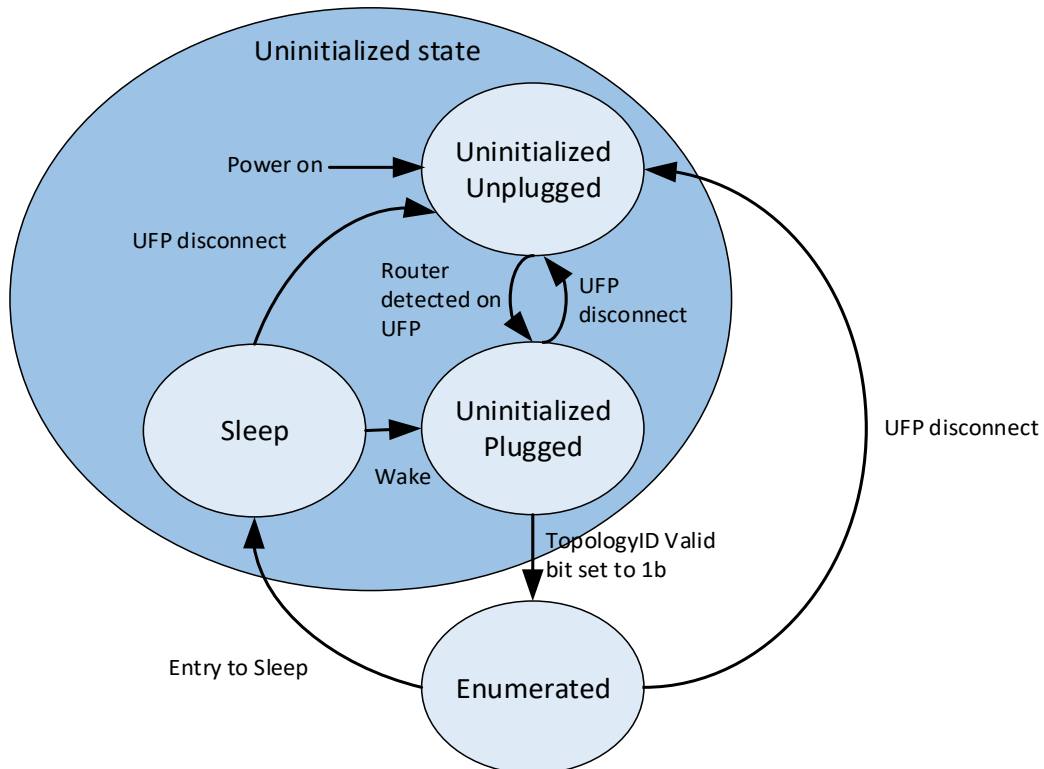


Figure 6-3 describes a Device Router state machine.

Figure 6-3. Device Router State Machine



6.3.1 Uninitialized Unplugged State

A Device Router enters this state upon completion of the following events:

- Power on.
- Upstream Facing Port is disconnected.

Upon entering this state, a Device Router does the following:

- Discards all Transport Layer Packets.
- Removes all Paths.
- Restores all Configuration Spaces to their default values.

Note: All Lane Adapters are in CLd state while a Router is in the Uninitialized Unplugged state.

A Device Router exits this state after detecting a Router on its Upstream Facing Port (see Section 4.1.2.2).

6.3.2 Uninitialized Plugged State

A Host Router enters this state:

- After Power On.
- From the sleep state, upon a wake event (see Section 4.4.7).
- After Host Router reset (See Section 6.10).

A Device Router enters this state:

- From the Uninitialized Unplugged state, when it detects a Router on its Upstream Facing Port (see Section 4.1.2.2).
- From the sleep state, upon a wake event (see Section 4.4.7).

While in this state, a Router performs Lane Initialization on all Connected Adapters.

A Host Router exits this state when the *TopologyID Valid* bit is set to 1b.

A Device Router exits this state upon the following events:

- *TopologyID Valid* bit is set to 1b.
- The Router is hot unplugged.

6.3.3 Sleep State

Section 4.5 defines how a Router enters and exits sleep and how it behaves while in sleep state.

6.3.4 Enumerated State

A Router enters this state from the Uninitialized Plugged state when its *TopologyID Valid* bit is set to 1b.

A Router in this state supports routing of Tunneled Protocols through the USB4 Fabric.

A Router exits this state when its Upstream Facing Port is disconnected. A Host Router also exits this state upon a Host Router reset (see Section 6.10).

See Section 6.7 for more information on Router enumeration.

6.4 Control Packet Protocol

6.4.1 Control Adapter

A Router shall support an internal Control Adapter that is used solely for transmitting and receiving Control Packets to and from the Transport Layer. Unlike the other Adapter types, the Control Adapter does not connect directly to a Link and therefore does not have a Physical Layer associated with it.

6.4.2 Control Packets

6.4.2.1 Bit/Byte Conventions

Control Packets are defined using the bit and byte conventions defined in Section 5.1.1.

6.4.2.2 Format

A Control Packet is a Transport Layer Packet. A Control Packet has the generic structure shown in Figure 6-4. The first DW is the Transport Layer Packet Header. The remaining DWs are payload and are defined in Table 6-1.

Figure 6-4 Control Packet Format

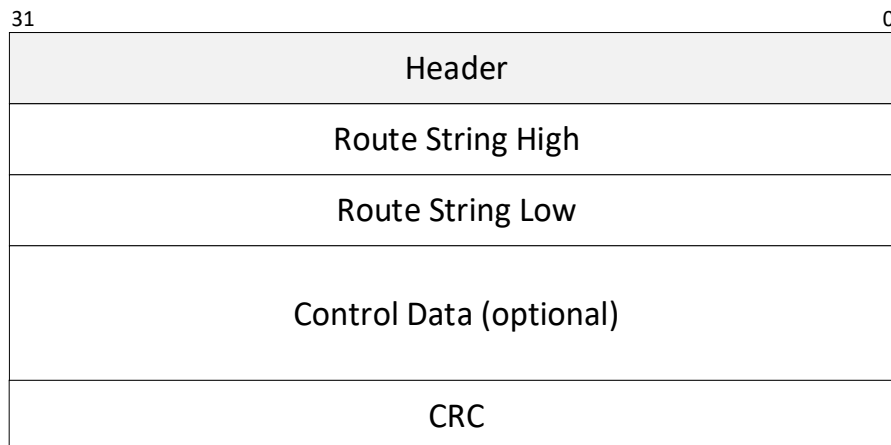
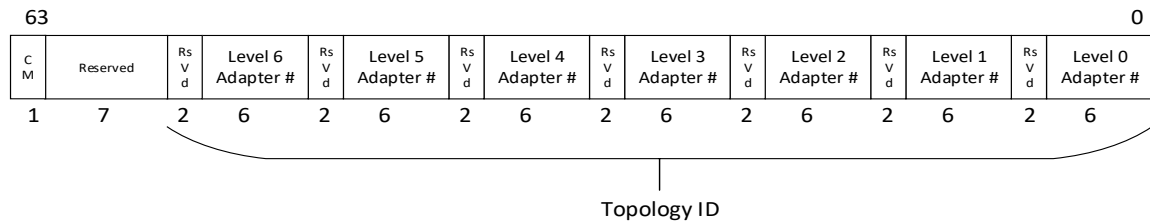


Table 6-1. Control Packet Payload

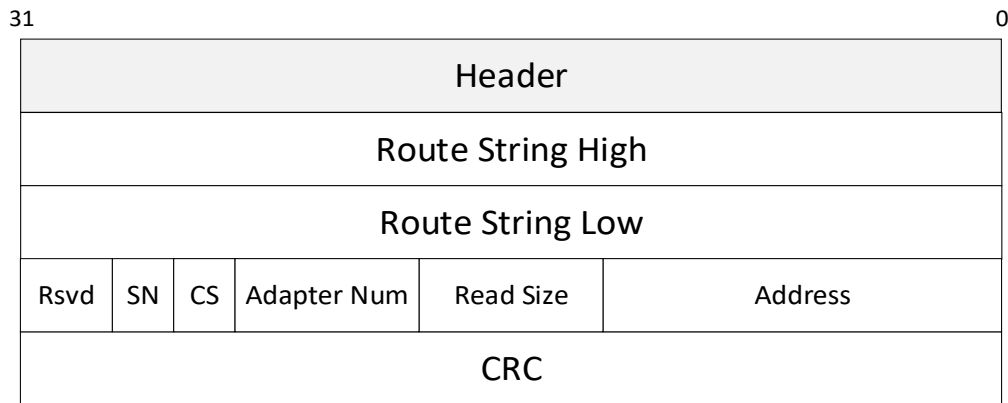
DW	Field	Description
1	<i>Route String High</i>	<p>Route String High – All Control Packets shall include a Route String. The format of the Route String is shown in Figure 6-5.</p> <p>For Control Packets that originate from the Connection Manager and target a Router:</p> <p>TopologyID [55:32] – Shall contain the high 24 bits of the TopologyID of the target Router.</p> <p>Rsvd [62:56] – Shall be set to 0.</p> <p>CM [63] – Shall be set to 0b.</p> <p>For Control Packets that originate from an Enumerated Router and target the Connection Manager:</p> <p>TopologyID [55:32] – Shall contain the high 24 bits of the TopologyID of the Router that originates the Control Packet.</p> <p>Rsvd [62:56] – Shall be set to 0.</p> <p>CM [63] – Shall be set to 1b.</p> <p>For Read Responses that originate from an Uninitialized Router and target the Connection Manager:</p> <p>TopologyID [55:32] – Shall be set to the high 24 bits of the TopologyID that was used to access the Router.</p> <p>Rsvd [62:56] – Shall be set to 0.</p> <p>CM [63] – Shall be set to 1b.</p> <p>For Notification Packets that originate from an Uninitialized Router and target the Connection Manager:</p> <p>TopologyID [55:32] – Shall be set to 0.</p> <p>Rsvd [62:56] – Shall be set to 0.</p> <p>CM [63] – Shall be set to 1b.</p>
2	<i>Route String Low</i>	<p>Route String Low – All Control Packets shall include a Route String. The format of the Route String is shown in Figure 6-5.</p> <p>For Control Packets that originate from the Connection Manager and target an Enumerated Router:</p> <p>TopologyID [31:0] – Shall contain the low 32 bits of the TopologyID of the target Router.</p> <p>For Control Packets that originate from a Router and target the Connection Manager:</p> <p>TopologyID [31:0] – Shall contain the low 32 bits of the TopologyID of the Router that originates the Control Packet.</p> <p>For Read Responses that originate from an Uninitialized Router and target the Connection Manager:</p> <p>TopologyID [31:0] – Shall be set to the low 32 bits of the TopologyID that was used to access the Router.</p> <p>For Notification Packets that originate from an Uninitialized Router and target the Connection Manager:</p> <p>TopologyID [31:0] – Shall be set to 0.</p>
(n+2):3 (if n>0)	<i>Control Data</i>	<p>Control Data – n DWs (where n >=0) carrying additional information specific to each type of Control Packet.</p>
n+3	<i>CRC</i>	<p>CRC – A 32-bit Cyclic Redundancy Code that protects the Route String and Control Data. The CRC does not cover the Control Packet Header. The CRC shall be calculated in increasing DW order, starting with the <i>Route String High</i> DW. Within each DW, CRC shall be calculated from bit[31] to bit[0]. The following CRC shall be used:</p> <ul style="list-style-type: none"> Width: 32 Poly: 1EDC6F41h Init: FFFFFFFFh RefIn: True RefOut: True XorOut: FFFFFFFFh <p>See Appendix A for examples of CRC calculations for several Control Packets.</p>

Figure 6-5. Route String Format**6.4.2.3 Read Request**

A Connection Manager uses Read Requests to read from a Configuration Space. A Read Request shall have the format shown in Figure 6-6. The fields in a Read Request shall be as defined in Table 6-2.

Table 6-2. Content of a Read Request

DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header HEC – See Section 5.1.2.1.1 Length – 10h HopID – 00h SuppID – 0b PDF – 1h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2.
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2.
3	12:0	<i>Address</i>	Address – DW address of the first configuration register to read.
	18:13	<i>Read Size</i>	Read Size – Number of Doublewords that shall be read starting from the <i>Address</i> field value. The <i>Read Size</i> field shall be greater than 0 and less than or equal to 60.
	24:19	<i>Adapter Num</i>	Adapter Num – Adapter Number of the Adapter whose Configuration Space is being read or 0 if Router Configuration Space is being read.
	26:25	<i>Configuration Space (CS)</i>	Configuration Space – Identifies the target Configuration Space. 00b – Path Configuration Space 01b – Adapter Configuration Space 10b – Router Configuration Space 11b – Counters Configuration Space
	28:27	<i>Sequence Number (SN)</i>	Sequence Number – Used to associate a Response Packet with a Request Packet. The sequence number is assigned by the Connection Manager and is returned in the Response Packet by the Destination Router.
	31:29	<i>Rsvd</i>	Reserved.
4	31:0	<i>CRC</i>	CRC – See Table 6-1.

Figure 6-6. Read Request**CONNECTION MANAGER NOTE**

A Connection Manager shall only have one outstanding Read Request or Write Request at a time. The Connection Manager shall wait for a response to the previous Read or Write Request before sending the next Read or Write Request.

A Connection Manager shall set the Adapter Num field in a Read Request to 0b when the Configuration Space field in the Read Request is 10b.

6.4.2.4 Read Response

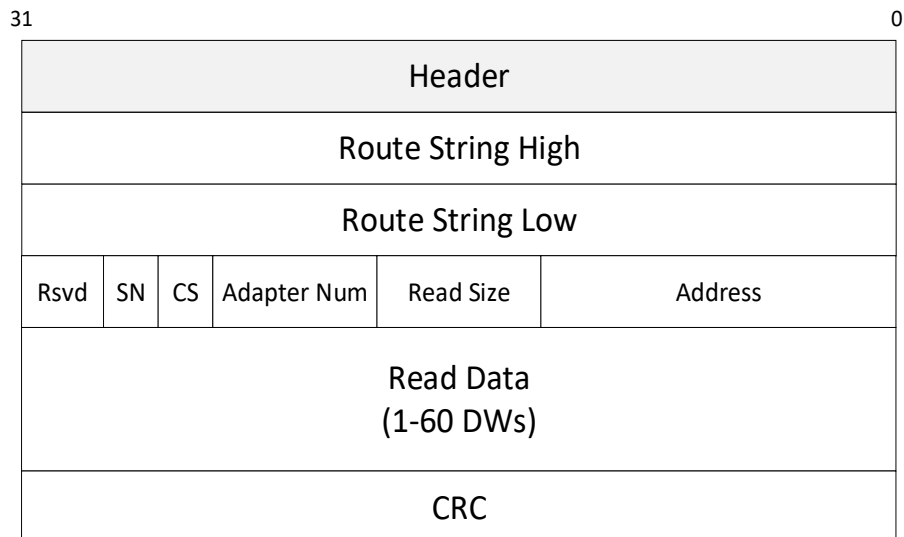
A Router uses a Read Response to respond to a Read Request. A Read Response shall have the format shown in Figure 6-7. The fields in a Read Response shall be as defined in Table 6-3.

Table 6-3. Content of a Read Response

DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header. HEC – See Section 5.1.2.1.1 Length – See Section 5.1.2 HopID – 00h SuppID – 0b PDF – 1h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2.
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2.
3	12:0	<i>Address</i>	Address – DW address of the first configuration register to be read. This field shall contain the same value as the associated Read Request.
	18:13	<i>Read Size</i>	Read Size – Number of Doublewords that were requested to be read. This field shall contain the same value as the associated Read Request.
	24:19	<i>Adapter Num</i>	Adapter Num – For a Response to a Request that targets Router Configuration Space, this field shall contain the Adapter Number on which the associated Read Request arrived. For a Response to a Request that targets other Configuration Spaces, this field shall contain the <i>Adapter Num</i> value in the associated Read Request.

DW	Bits	Field	Description
	26:25	<i>Configuration Space (CS)</i>	Configuration Space – Identifies the target Configuration Space. This field shall contain the same value as the associated Read Request.
	28:27	<i>Sequence Number (SN)</i>	Sequence Number – Used to associate a Response Packet with a Request Packet. This field shall contain the same value as the associated Read Request.
	31:29	<i>Rsvd</i>	Reserved.
(3+Read Size):4	31:0	<i>Read Data</i>	Read Data – Data read from the target Configuration Space. The size of this field shall match the number of DWs in the <i>Read Size</i> field. Data shall be structured in increasing address order with bit 0 of each DW containing bit 0 of the corresponding configuration register.
4+Read Size	31:0	<i>CRC</i>	CRC – See Table 6-1.

Figure 6-7. Read Response



6.4.2.5 Write Request

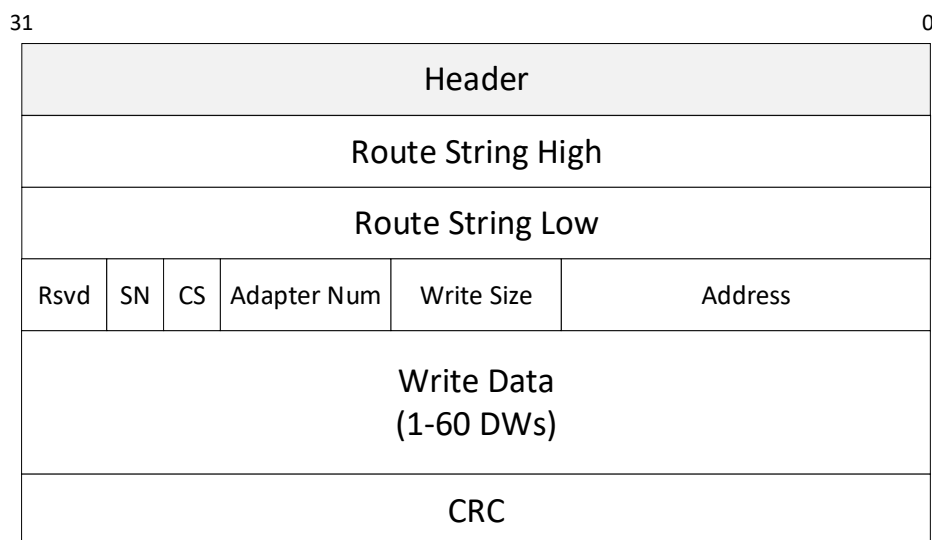
A Connection Manager uses Write Requests to write to a Configuration Space. A Write Request shall have the format shown in Figure 6-8. The fields in a Write Request shall be as defined in Table 6-4.

Table 6-4. Content of a Write Request

DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header. HEC – See Section 5.1.2.1.1 Length – See Section 5.1.2 HopID – 00h SupplID – 0b PDF – 2h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2.
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2.

DW	Bits	Field	Description
3	12:0	<i>Address</i>	Address – DW address of the first configuration register to be written.
	18:13	<i>Write Size</i>	Write Size – Number of Doublewords that were requested to be written. The <i>Write Size</i> field shall be greater than 0 and less than or equal to 60.
	24:19	<i>Adapter Num</i>	Adapter Num – Adapter Number of the Adapter whose Configuration Space is being written or 0 if Router Configuration Space is being written.
	26:25	<i>Configuration Space (CS)</i>	Configuration Space – Identifies the target Configuration Space. 00b – Path Configuration Space 01b – Adapter Configuration Space 10b – Router Configuration Space 11b – Counters Configuration Space
3	28:27	<i>Sequence Number (SN)</i>	Sequence Number – Used to associate a Response Packet with a Request Packet. The sequence number is assigned by the Connection Manager and is returned in the Response Packet by the destination Router.
	31:29	<i>Rsvd</i>	Reserved.
(3+Write Size):4	31:0	<i>Write Data</i>	Write Data – Data to be written to Configuration Space. The size of this field shall match the number of DWs in the <i>Write Size</i> field. Data shall be structured in increasing address order with bit 0 of each DW containing bit 0 of the corresponding configuration register.
4+Write Size	31:0	<i>CRC</i>	CRC – See Table 6-1.

Figure 6-8. Write Request

**CONNECTION MANAGER NOTE**

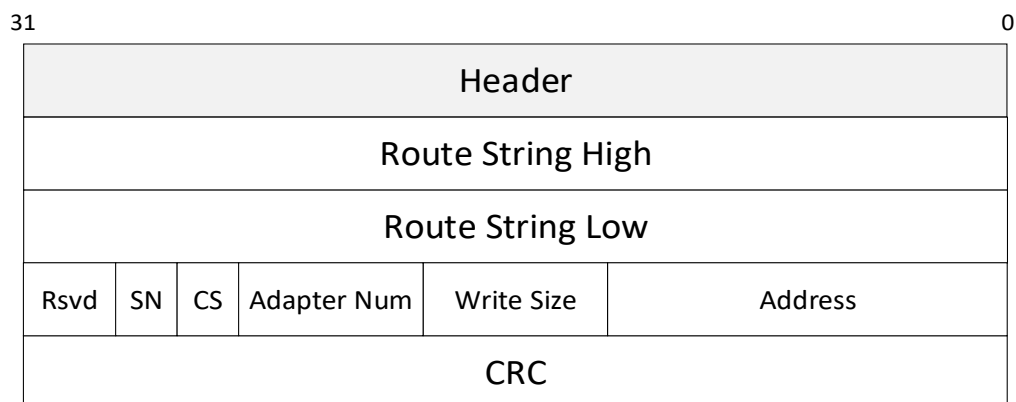
A Connection Manager shall set the *Adapter Num* field in a Write Request to 0b when the *Configuration Space* field in the Write Request is 10b.

6.4.2.6 Write Response

A Router uses a Write Response to respond to a Write Request. A Write Response shall have the format shown in Figure 6-9. The fields in a Write Response shall be as defined in Table 6-5.

Table 6-5. Content of a Write Response

DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header. HEC – See Section 5.1.2.1.1 Length – 10h HopID – 00h SupplD – 0b PDF – 2h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2.
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2.
3	12:0	<i>Address</i>	Address – DW address of the first configuration register the associated Request is targeting. This field shall contain the same value as the associated Write Request.
	18:13	<i>Write Size</i>	Write Size – Number of Doublewords that were requested starting from the Address field value. This field shall contain the same value as the associated Write Request.
	24:19	<i>Adapter Num</i>	Adapter Num – This field shall contain the Adapter Num value in the associated Write Request.
	26:25	<i>Configuration Space (CS)</i>	Configuration Space – Identifies the target Configuration Space. This field shall contain the same value as the associated Write Request.
	28:27	<i>Sequence Number (SN)</i>	Sequence Number – Used to associate a Response Packet with a Request Packet. This field shall contain the same value as the associated Write Request.
	31:29	<i>Rsvd</i>	Reserved.
4	31:0	<i>CRC</i>	CRC – See Table 6-1.

Figure 6-9. Write Response

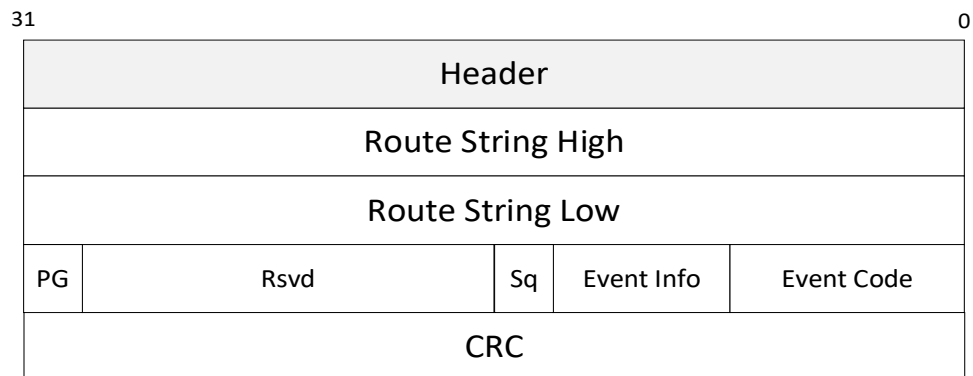
6.4.2.7 Notification Packet

A Notification Packet shall have the format shown in Figure 6-10 and the fields defined in Table 6-6.

A Notification Packet carrying a Hot Plug Acknowledgment (see Table 6-12) is called a Hot Plug Acknowledgment Packet.

Table 6-6. Content of a Notification Packet

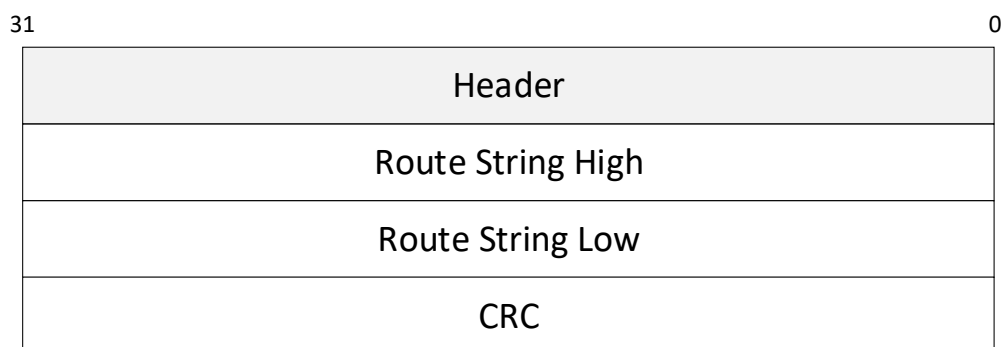
DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header. HEC – See Section 5.1.2.1.1 Length – 10h HopID – 00h SupplD – 0b PDF – 3h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2.
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2.
3	7:0	<i>Event Code</i>	Event Code – Identifies the type of event. See Table 6-12.
	13:8	<i>Event Info</i>	Event Info – Additional information relating to the notification event. See Table 6-12.
	14	<i>Sequence (Sq)</i>	Sequence – Used to associate a Notification Acknowledgement with a Notification Packet. The Sequence bit is assigned by the originating Router and is returned in the Enhanced Notification Acknowledgement Packet by the Connection Manager. This bit shall be set to 0b if any of the following are true: <ul style="list-style-type: none"> The Router does not support the Sequence bit in Notification Packet capability (see Section 8.3.1.3.2.2). The Router supports the Sequence bit in Notification Packet capability but the capability is not enabled by a Set Capabilities Operation. Else, the bit shall be flipped when sending a Notification Packet for a new event that requires a Notification Acknowledgment (see Section 6.6). The bit shall maintain its last value when sending a new Notification Packet that does not require a Notification Acknowledgment. The bit shall maintain its last value when retransmitting a Notification Packet (see Section 6.6). This bit shall be set to 0b following a transition to the Uninitialized Plugged state.
	29:15	<i>Rsvd</i>	Reserved.
	31:30	<i>PG</i>	PG – Differentiates Hot Plug and Hot Unplug Events in a Hot Plug Acknowledgment Packet. 00b – Notification Packet is not a Hot Plug Acknowledgment 01b – Rsvd 10b – Hot Plug Event 11b – Hot Unplug Event
4	31:0	<i>CRC</i>	CRC – See Table 6-1.

Figure 6-10. Notification Packet**6.4.2.8 Notification Acknowledgement Packet**

A Notification Acknowledgment Packet shall have the format shown in Figure 6-11 and the fields defined in Table 6-7.

Table 6-7. Content of a Notification Acknowledgement Packet

DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header. HEC – See Section 5.1.2.1.1 Length – 0Ch HopID – 00h SuppID – 0b PDF – 4h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2
3	31:0	<i>CRC</i>	CRC – See Table 6-1.

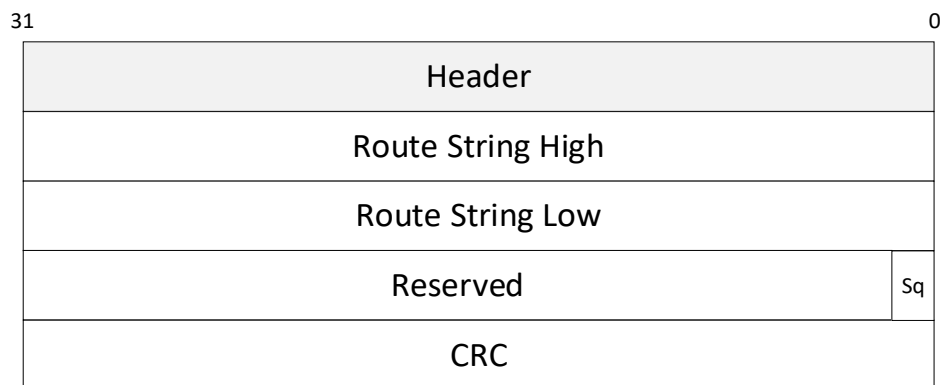
Figure 6-11. Notification Acknowledgement Packet

6.4.2.9 Enhanced Notification Acknowledgement Packet

An Enhanced Notification Acknowledgment Packet shall have the format shown in Figure 6-12 and the fields defined in Table 6-8.

Table 6-8. Content of an Enhanced Notification Acknowledgement Packet

DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header. HEC – See Section 5.1.2.1.1 Length – 10h HopID – 00h SuppID – 0b PDF – 8h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2
3	0	<i>Sequence (Sq)</i>	Sequence – Used to associate a Notification Acknowledgement with a Notification Packet. This field shall contain the same value as the associated Notification Packet.
3	31:1	<i>Rsvd</i>	Reserved.
4	31:0	<i>CRC</i>	CRC – See Table 6-1.

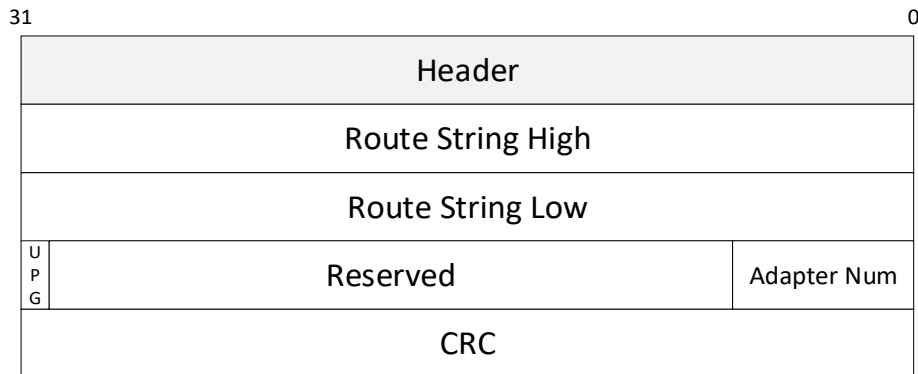
Figure 6-12. Enhanced Notification Acknowledgement Packet**6.4.2.10 Hot Plug Event Packet**

This packet is used by a Router to notify a Connection Manager that a Hot Plug or Hot Unplug Event has occurred. A Hot Plug Event Packet shall have the structure defined in Table 6-9 and Figure 6-13.

Table 6-9. Content of a Hot Plug Event Packet

DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header. HEC – See Section 5.1.2.1.1 Length – 10h HopID – 00h SuppID – 0b PDF – 5h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2.
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2.

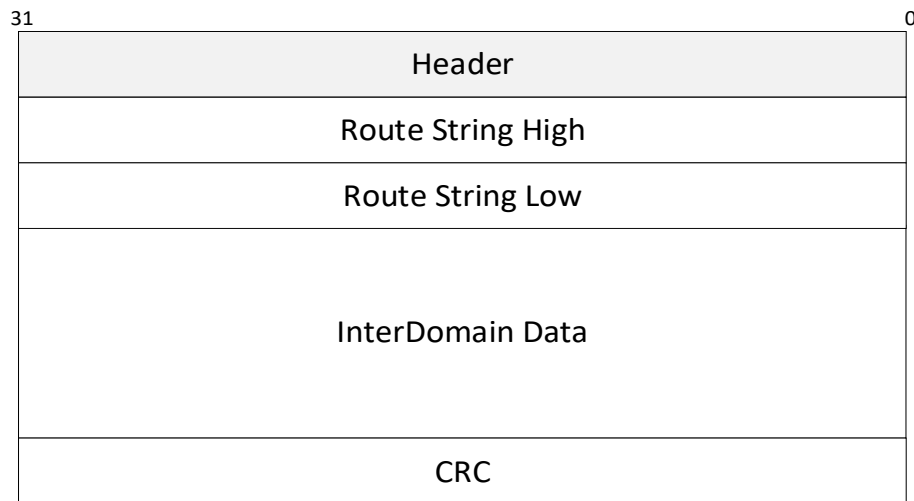
DW	Bits	Field	Description
3	5:0	<i>Adapter Num</i>	Adapter Num – Adapter Number that experienced the Hot Plug or Hot Unplug Event.
	30:6	<i>Rsvd</i>	Reserved.
	31	<i>UPG</i>	UPG – Shall be set to 0b for a Hot Plug Event or 1b for a Hot Unplug Event.
4	31:0	<i>CRC</i>	CRC – See Table 6-1.

Figure 6-13. Hot Plug Event Packet**6.4.2.11 Inter-Domain Request**

An Inter-Domain Request is used for Inter-Domain communication between two Connection Managers. An Inter-Domain Request shall have the format shown in Figure 6-14 and fields as defined in Table 6-10.

Table 6-10. Content of an Inter-Domain Request

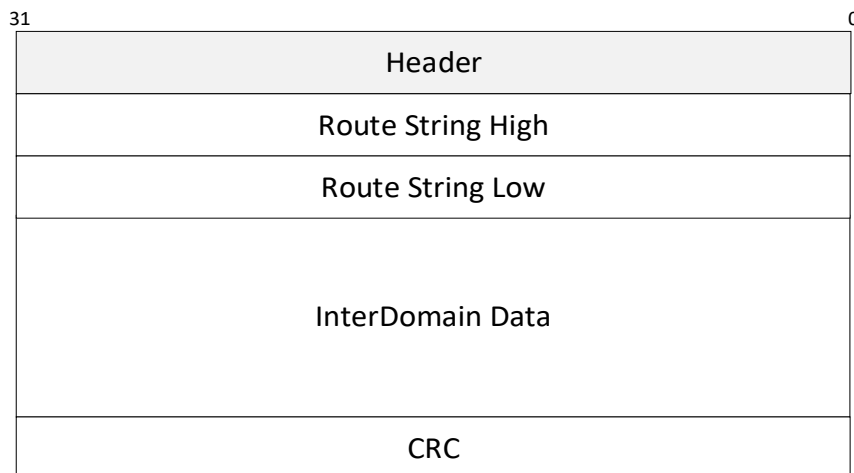
DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header. HEC – See Section 5.1.2.1.1 Length – See Section 5.1.2 HopID – 00h SuppID – 0b PDF – 6h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2 and Figure 6-16. The Route String shall include the TopologyID of the Inter-Domain Router (i.e. the Router in the Domain that interfaces to the Inter-Domain Link). The <i>CM</i> bit shall be set to 0b.
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2 and Figure 6-16. The Route String shall include the TopologyID of the Inter-Domain Router (i.e. the Router in the Domain that interfaces to the Inter-Domain Link).
(N+3):3	31:0	<i>InterDomain Data</i>	InterDomain Data – N number of DWs to be transferred to the other Connection Manager. The contents of this field are outside the scope of this specification. See the USB4 Inter-Domain Specification for definition.
N+4	31:0	<i>CRC</i>	CRC – See Table 6-1.

Figure 6-14. Inter-Domain Request**6.4.2.12 Inter-Domain Response**

An Inter-Domain Response is used to respond to an Inter-Domain Request. An Inter-Domain Response shall have the format shown in Figure 6-15 and fields as defined in Table 6-11.

Table 6-11. Content of an Inter-Domain Response

DW	Bits	Field	Description
0	31:0	<i>Header</i>	Header – Transport Layer Packet Header. HEC – See Section 5.1.2.1.1 Length – See Section 5.1.2 HopID – 00h SupplD – 0b PDF – 7h
1	31:0	<i>Route String High</i>	Route String High – See Section 6.4.2.2 and Figure 6-16. The Route String shall include the TopologyID of the Inter-Domain Router (i.e. the Router in the Domain that interfaces to the Inter-Domain Link). The <i>CM</i> bit shall be set to 0b.
2	31:0	<i>Route String Low</i>	Route String Low – See Section 6.4.2.2 and Figure 6-16. The Route String shall include the TopologyID of the Inter-Domain Router (i.e. the Router in the Domain that interfaces to the Inter-Domain Link).
(N+3):3	31:0	<i>InterDomain Data</i>	InterDomain Data – N number of DWs to be transferred to the other Connection Manager. The contents of this field are outside the scope of this specification. See the USB4 Inter-Domain Specification for definition.
N+4	31:0	<i>CRC</i>	CRC – See Table 6-1.

Figure 6-15. Inter-Domain Response**6.4.3 Control Packet Routing****6.4.3.1 Upstream-Bound Packets**

An Uninitialized Router shall discard a Control Packet with the *CM* bit set to 1b and shall not send any packets in response. An Enumerated Router shall forward a Control Packet with the *CM* bit set to 1b to its Upstream Adapter.

6.4.3.2 Downstream-Bound Packets

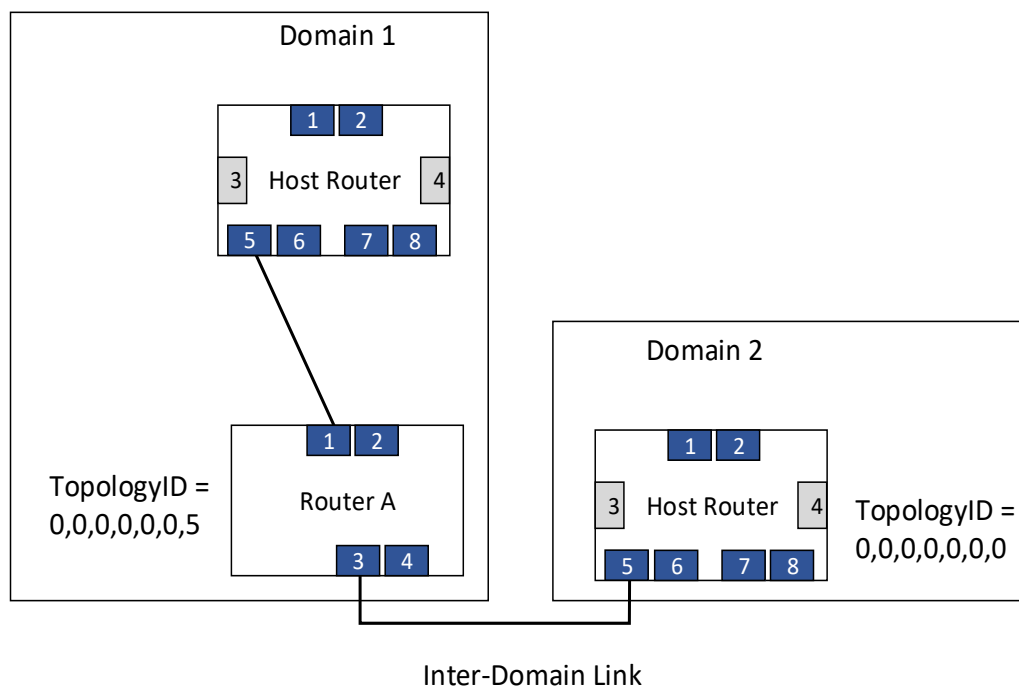
When a Router receives a Control Packet with the *CM* bit set to 0b on its Upstream Adapter, it shall route the packet as follows:

- If the *TopologyID Valid* bit in Router Configuration Space is set to 0b, then the Router shall process the packet as follows:
 - If the packet is a Read Request or a Write Request that targets Router Configuration Space, the Router shall process the packet as described in Section 6.4.3.3.
 - Else, Router shall drop the packet and shall not send any packets in response.
- Else the Router shall extract the Egress Adapter Number from the Route String that corresponds to the Router's depth in the Spanning Tree (as present in the *Depth* field in Router Configuration Space). For example, given a Route String with a TopologyID of 0,0,0,0,3,1,8 and a Router with a depth of 2, the Egress Adapter Number is 3.
 - If the extracted Adapter Number is 0, the Control Adapter of the Router shall consume the packet. The Router shall process the packet using the Enumerated Router Flow in Section 6.4.3.2.1.
 - If the extracted Adapter Number refers to a Protocol Adapter, the packet shall be dropped and the Router shall send the Connection Manager a Notification Packet with Event Code = ERR_ADP as defined in Table 6-12.
 - If the extracted Adapter Number refers to a disconnected or disabled Adapter, the Router shall drop the packet and shall send the Connection Manager a Notification Packet with Event Code = ERR_CONN as defined in Table 6-12.
 - If the extracted Adapter Number refers to a connected Adapter and the *Lock* bit in the Adapter Configuration Space is set to 1b, the Router shall drop the packet and shall send the Connection Manager a Notification Packet with Event Code = ERR_LOCK as defined in Table 6-12.
 - Else, the Router shall forward the packet over the Egress Adapter that matches the extracted Adapter Number.

When a Router receives a Control Packet with the *CM* bit set to 0b on a Lane Adapter that is not the Upstream Adapter, it shall route the packet as follows:

- If the *TopologyID Valid* bit in Router Configuration Space is set to 0b, then the Router shall process the packet as follows:
 - If the packet is a Read Request or a Write Request, then the Router shall drop the packet and shall send the Adapter that originated the Request a Notification Packet with Event Code = ERR_NUA as defined in Table 6-12.
 - Else, Router shall drop the packet and shall not send any packets in response.
- Else:
 - If the packet is an Inter-Domain Request or an Inter-Domain Response, the Router shall modify the packet as follows and then send the packet over the Upstream Adapter:
 - Replace the Route String in the packet with the Route String of the receiving Router within the receiving Domain, then add the Ingress Adapter Number of the Adapter connected to the Inter-Domain Link.
For example, Figure 6-16 shows two Domains that are connected by an Inter-Domain Link. When the Host Router in Domain 1 sends an Inter-Domain Packet to the Host Router in Domain 2, the Route String in the Packet has a TopologyID of [0,...,0,3,5]. The Host Router in Domain 2 then updates the Route String in the packet to [0,...,0,0,5].
 - Set the *CM* bit to 1b.
 - Update the *CRC* field.
 - If the packet is a Read Request or a Write Request, then the Router shall drop the packet and shall send the Adapter that originated the Request a Notification Packet with Event Code = ERR_ENUM as defined in Table 6-12.
 - Else, Router shall drop the packet and shall not send any packets in response.

Figure 6-16. Example of Control Packet Routing Between Domains



**CONNECTION MANAGER NOTE**

The Connection Manager shall set the Lock bit in a Downstream Facing Port to 0b before it enumerates a Router connected to the Downstream Facing Port.

6.4.3.2.1 Enumerated Router Flow

The following describes how an enumerated Router handles a Control Packet:

- If the Control Packet is either a Read Request or a Write Request, the Router shall process the packet as described in Section 6.4.3.3.
- If the Control Packet is a Hot Plug Acknowledgment Packet, the Router shall process the packet as described in Section 6.8.
- If the Control Packet is a Notification Acknowledgment Packet, the Router shall process the packet as described in Section 6.6.
- Else, the Router shall drop the Control Packet and shall not send any packets in response.

6.4.3.3 Processing of Read and Write Requests

A Router that is the target of a Read Request or a Write Request shall process the Control Packet according to the following rules:

- If the packet addresses any Configuration Space other than the Router Configuration Space and the *Adapter Num* field in the packet exceeds the value of the *Max Adapter* field in Router Configuration Space:
 - The read or write operation shall not be performed and a Response Packet shall not be sent.
 - The Router shall send the Connection Manager a Notification Packet with Event Code = ERR_ADP as defined in Table 6-12.
- Else, if the packet is a Write Request and the *Write Size* field in the packet is zero, then the write operation shall not be performed. The Router shall send a Write Response.
- Else, if the packet is a Read Request or a Write Request and it targets a Lane Adapter that is unused (see Section 5.2.1), the Router may send the Connection Manager a Notification Packet with Event Code = ERR_ADDR as defined in Table 6-12.
- Else, if the packet is a Write Request and the *Length* field in the packet header does not equal the expected length $([Write\ Size + 4] * 4)$:
 - The Router shall not perform a write operation and shall not send a Write Response.
 - The Router shall send the Connection Manager a Notification Packet with Event Code = ERR_LEN as defined in Table 6-12.
- Else, if the packet is a Write Request and if the *Address* and *Write Size* fields in the packet extend beyond the address range supported:
 - The part of the write data that fits within the supported address range shall be written. The part of the write data that fits outside the supported address range shall be dropped.
 - A Write Response shall not be sent.
 - The Router shall send the Connection Manager a Notification Packet with Event Code = ERR_ADDR as defined in Table 6-12.

- Else, if the packet is a Read Request and if the *Address* and *Read Size* fields in the packet extend beyond the address range supported:
 - A Read Response shall not be sent.
 - The Router shall send a Notification Packet on its Upstream Facing Port with Event Code = ERR_ADDR as defined in Table 6-12.
- Else, if the packet is a Read Request and the *Read Size* field in the packet is zero then the Router shall send a Read Response without a *Read Data* field.
- Else, if the packet is a Read Request and *Read Size* field in the packet contains a value larger than 60:
 - A Read Response shall not be sent.
 - The Router shall send the Connection Manager a Notification Packet with Event Code = ERR_LEN as defined in Table 6-12.
- Else, process the packet and send a Response Packet.
 - A Router shall send a Write Response for a Write Request to a Path Configuration Space only after it has executed the Write Request, including setting the entry in the Routing Table and in the Egress Arbiter.

Note: Unless specified otherwise, sending a Write Response does not indicate that the Router has taken any action yet related to the contents of the Write Request.

6.4.4 Control Packet Reliability

The following rules provide reliable transport for Control Packets:

- Each Router along the Path of a Control Packet shall check the validity of the *CRC* field. If a packet fails the CRC check, the Router shall discard the packet.
- Unless otherwise specified, a Router that is the target of a Read Request shall send a Read Response within tCPResponse of receiving the Request.
- Unless otherwise specified, a Router that is the target of a Write Request shall send a Write Response within tCPResponse of receiving the Request.
- A Router forwarding a Control Packet shall send the packet on an Egress Adapter not later than tCPForward from the time the packet was received on an Ingress Adapter.
- A Router that receives a Read Request or a Write Request may drop the packet if it is received before the Router has responded to the previous Read Request or Write Request.



CONNECTION MANAGER NOTE

A Connection Manager can optionally implement a timeout mechanism and may retry a Control Packet if no response is received within the timeout interval. If a Connection Manager implements a timeout, it is recommended that the timeout is at least 10 ms for Control Packets within a Domain and is at least 1 second for Inter-Domain Control Packets.



CONNECTION MANAGER NOTE

A Connection Manager uses the Sequence Number in a Response Packet to match it to the corresponding Request Packet.

6.5 Notification Events

Table 6-12 lists the events that generate a Notification Packet. All Event Codes not listed in Table 6-12 are reserved.

Table 6-12. Notification Events

Event Code	Reference	Initiator	Event Code	Event Info
Error Events				
ERR_CONN	Section 6.4.3	Router	0	The Adapter Number of the unconnected Adapter.
ERR_LINK	Section 4.4.2	Router	1	The Adapter Number of the Adapter that experienced the error.
ERR_ADDR	Section 6.4.3.3	Router	2	The Adapter Number of the Adapter that is the target of the Read/Write request.
ERR_ADP	Section 6.4.3.3 Section 6.4.3	Router	4	1. The Adapter Num value in the Read or Write Request; or 2. The Adapter Number of the non-Lane Adapter that triggered the event.
ERR_ENUM	Section 6.4.3	Router	8	00h.
ERR_NUA	Section 6.4.3	Router	9	00h.
ERR_LEN	Section 6.4.3.3	Router	11	The Adapter Num value in the Request Packet.
ERR_HEC	Section 5.1.2.1.1	Router	12	The Adapter Number of the Ingress Adapter that experienced the error.
ERR_FC	Section 5.3.2.1.2	Router	13	The Adapter Number of the Ingress Adapter that experienced the error.
ERR_PLUG	Section 6.8.1.1	Router	14	The Adapter that does not reach CLO state within tTrainingAbort1 time after entering the Training state.
ERR_LOCK	Section 6.4.3.2	Router	15	The Adapter Number of the locked Adapter
Notifications				
HP_ACK	Section 6.8	Connection Manager	7	The <i>Adapter Num</i> field from the Hot Plug Event Packet.
ROP_CMPLT	Section 8.3.1	Router	33	00h – Completion of Router Operation. 01h – <i>Router Ready</i> bit set to 1b. 02h – <i>Configuration Ready</i> bit set to 1b. 03h – <i>Sleep Ready</i> bit set to 1b. All other values are reserved.
POP_CMPLT	Section 8.3.2	Router	34	The Adapter Number of the Lane 0 Adapter of the USB4 Port executing the Operation.
PCIE_WAKE	Section 11.1.4	Router	35	00h
DP_CON_CHANGE	Section 10.8.1.3.3	Router	36	[3:0] – Connector Number. [4] – IRQ_HP.D. [5] – Plug/Unplug.
LINK_RECOVERY	Section 4.4.7	Router	38	The Adapter Number of the Lane 0 Adapter that completed Gen 4 Link Recovery.

ASYM_LINK	Section 4.2.2	Router	39	The Adapter Number of the Lane 0 Adapter that finished the Asymmetric transition.
Protocol Adapter Events				
DP_BW	Section 10.7	Router	32	The DP IN Adapter Number.
DPTX_DISCOVERY	Section 10.8.2	Router	37	The DP IN Adapter Number.

6.6 Notification Acknowledgement

A Router expects a Notification Acknowledgment from the Connection Manager in response to the following packets:

- A Notification Packet with Event Code = ERR_LINK.
- A Notification Packet with Event Code = ERR_HEC
- A Notification Packet with Event Code = ERR_FC
- A Notification Packet with Event Code = ERR_PLUG
- A Notification Packet with Event Code = DP_BW
- A Notification Packet with Event Code = PCIE_WAKE
- A Notification Packet with Event Code = DP_CON_CHANGE
- A Notification Packet with Event Code = DPTX_DISCOVERY

If the *Sequence bit in Notification Packet* capability is disabled (see Section 8.3.1.3.3), then reception of a Notification Acknowledgment Packet is considered a Notification Acknowledgment event.

If the *Sequence bit in Notification Packet* capability is enabled, then reception of an Enhanced Notification Acknowledgment Packet is considered a Notification Acknowledgment event.

A Router shall retransmit a Notification Packet that requires a Notification Acknowledgment if a Notification Acknowledgment Packet is not received within the time specified by the *Notification Timeout* field in Router Configuration Space. A Router shall retransmit a Notification Packet that requires a Notification Acknowledgment until a Notification Acknowledgment is received for it when the Notification Retry Limit Capability is Disabled or not supported. When the Notification Retry Limit Capability is Enabled, a Router shall retransmit a Notification Packet that requires a Notification Acknowledgment until either a Notification Acknowledgment is received for it or the Notification Retry Limit is reached (see Section 8.3.1.3.2.4).

A Router shall not send a Notification Packet for a different event that requires a Notification Acknowledgment while a previous packet that requires a Notification Acknowledgment is pending (i.e. before a Notification Acknowledgment Packet or an Enhanced Notification Acknowledgment Packet is received).

A Router may send Notification Packets that do not require a Notification Acknowledgment while a previous packet that requires a Notification Acknowledgment is pending.



CONNECTION MANAGER NOTE

If a Notification Acknowledgment Packet is received after the Notification Timeout expired, it is possible that a Router will associate the Notification Acknowledgment Packet with a subsequent Notification Packet. This can result in the Router not retransmitting a Notification Packet even though it did not reach the Connection Manager. To avoid this, a Ver. 2 Connection Manager shall enable the Sequence bit in Notification Packet capability if supported by the Router (see Section 8.3.1.3.3).

If the Sequence bit in Notification Packet capability is disabled, a Connection Manager shall respond to a Notification Packet with a Notification Acknowledgment Packet. If the Sequence bit in Notification Packet capability is enabled, a Connection Manager shall respond to a Notification Packet with an Enhanced Notification Acknowledgment Packet.

The Connection Manager shall process Notification Packets from a specific Router in the order received.



CONNECTION MANAGER NOTE

A Connection Manager shall send a Notification Acknowledgment Packet in response to the following Notification Packets:

- *A Notification Packet with Event Code = ERR_LINK*
- *A Notification Packet with Event Code = ERR_HEC*
- *A Notification Packet with Event Code = ERR_FC*
- *A Notification Packet with Event Code = ERR_PLUG*
- *A Notification Packet with Event Code = DP_BW*

A Ver. 2 Connection Manager shall send a Notification Acknowledgment Packet in response to the following Notification Packets:

- *A Notification Packet with Event Code = PCIE_WAKE*
- *A Notification Packet with Event Code = DP_CON_CHANGE*
- *A Notification Packet with Event Code = DPTX_DISCOVERY*

6.7 Router Enumeration and Initialization

Router enumeration is the process by which a Connection Manager detects a connected Router and assigns it a TopologyID. After a Connection Manager enumerates a Router, the Router is part of the Connection Manager's Domain.



CONNECTION MANAGER NOTE

The following assumes that the Connection Manager USB4 Version field is set to indicate that it is using Ver. 2.0 of the USB4 Specification.

On transition to the Uninitialized state, a TBT3-Compatible Router shall:

- Expose USB4 Ports and PCIe Adapters as defined in Section 13.3.1.
- Set its sleep and wake behavior as defined in Section 13.2.4.

On transition to the Uninitialized state, a TBT3-Compatible Router with an Upstream Facing Port running in TBT3 Mode shall:

- Expose the additional registers defined in Section 13.6.

When the *TopologyID Valid* bit is set to 1b, a Router is enumerated. A TBT3-Compatible Router shall do the following after it is enumerated:

- Expose all its USB4 Ports and PCIe Adapters (if any) to the Connection Manager.
- Set the *Lock* bit to 1b on all Downstream Facing Ports.
- Set its sleep and wake behavior as defined in Section 4.4.7.

- Disable access to the additional registers defined in Section 13.6.

The TBT3-Compatible Router shall then set the *Router Ready* bit to 1b. The Router shall set the *Router Ready* bit to 1b within tSetRR time after the *TopologyID Valid* bit is set to 1b.

A TBT3-Compatible Router shall also send the Connection Manager a Notification Packet with *Event Code* = ROP_CMPLT and the *Event Info* field set to 01h.

On transition to the Uninitialized state, a Router that is not TBT3-Compatible shall:

- Expose all its USB4 Ports and PCIe Adapters (if any) to the Connection Manager.
- Set the *Lock* bit to 1b on all Downstream Facing Ports.
- Set sleep and wake behavior to default as defined in Section 4.4.7.

The Router that is not TBT3-Compatible shall then set the *Router Ready* bit to 1b.



CONNECTION MANAGER NOTE

A Connection Manager detects a connected Router by either:

- *Receiving a Hot Plug Event Packet from the Router with the UPG bit set to 0b (see Section 6.8); or*
- *Issuing a Read Request to the Router and receiving a Read Response.*

A Connection Manager shall abide by the following rules when enumerating a Router:

- *The Connection Manager may enumerate an Uninitialized Router at any time but is not required to do so.*
- *The Connection Manager shall not enumerate a Router that is connected to a Downstream Facing Port via an Adapter with an Adapter Type that equals Unsupported Adapter.*
- *The Connection Manager may issue Read Requests to an Uninitialized Router.*
- *The Connection Manager shall not issue a Write Request to an Uninitialized Router other than the Write Request that enumerates the Router.*
- *The Connection Manager may identify Inter-Domain Links by sending a Read Request or a Write Request and receiving a Notification Packet with Event Code = ERR_ENUM or Event Code = ERR_NUA.*

After enumerating a Router, the Connection Manager may read the contents of the Router's DRAM. If, after reading the contents of DRAM, the Connection Manager decides that it does not want the Router in its Domain, it may issue a Downstream Port Reset to the Router as described in Section 6.9. It is recommended that the Connection Manager keep a record of the Router's UUID so that on a subsequent Hot Plug event, the Connection Manager can compare the stored UUID value to the UUID value of the plugged Router to determine whether to enumerate the hot-plugged Router.

After setting the *Router Ready* bit to 1b, a Device Router waits for the Connection Manager to set the *Configuration Valid* bit to 1b. When the *Configuration Valid* bit in Router Configuration Space is set to 1b, a Device Router shall:

- If the *USB3 Tunneling On* bit is set to 1b, establish USB3 tunneling functionality.

- If the *PCIe Tunneling On* bit is set to 1b, establish PCIe tunneling functionality.

The Device Router shall then set the *Configuration Ready* bit in Router Configuration Space to 1b. The Device Router shall set the *Configuration Ready* bit to 1b within tSetCR time after the *Configuration Valid* bit is set to 1b.

After setting the *Configuration Ready* bit to 1b, a Device Router shall send the Connection Manager a Notification Packet with *Event Code* = ROP_CMPLT and the *Event Info* field set to 02h.



IMPLEMENTATION NOTE

A Device Router may decide to establish USB3 tunneling functionality when its Upstream Facing Port operates in USB4 Mode.

6.8 Hot Plug and Hot Unplug Events

There are two types of Hot Plug Events:

- **Router Hot Plug** – Occurs when a Router detects that another Router is hot-plugged into a Downstream Facing Port. Router Hot Plug is further defined in Section 6.8.1.
- **Adapter Hot Plug** – Occurs when a Protocol Adapter detects the Hot Plug of a device behind the Protocol Adapter. The methods for communicating a DP Adapter Hot Plug to a Connection Manager are defined in 10.3.3. No other Protocol Adapters report Adapter Hot Plug Events.

There are two types of Hot Unplug Events:

- **Router Hot Unplug** – Occurs when a Router detects that another Router is hot-removed from a Downstream Facing Port. Router Hot unplug is further defined in Section 6.8.2.
- **Adapter Hot Unplug** – Occurs when a Protocol Adapter detects the Hot Unplug of a device behind the Protocol Adapter. The methods for communicating a DP Adapter Hot Unplug to a Connection Manager are defined in 10.3.3. No other Protocol Adapters report Adapter Hot Unplug Events.

A Router expects a Hot Plug Acknowledgment Packet from the Connection Manager in response to a Hot Plug Event Packet. A Router shall retransmit a Hot Plug Event Packet if a Hot Plug Acknowledgment Packet acknowledging the Hot Plug or the Hot Unplug Event is not received within the time specified by the *Notification Timeout* field in Router Configuration Space, when the Notification Retry Limit Capability is Disabled or not supported. When the Notification Retry Limit Capability is Enabled, a Router shall retransmit a Hot Plug Event Packet until either a Hot Plug Acknowledgment Packet is received for it, or the Notification Retry Limit is reached (see Section 8.3.1.3.2.4).

A Router only reports one Hot Plug or Unplug event at a time. A Router shall not send a Hot Plug Event Packet for a new Hot Plug Event from any Adapter until it receives a Hot Plug Acknowledgment Packet for the previous Hot Plug/Unplug Event. A Router shall not send a Hot Unplug Event Packet for a new Hot Plug Event from any Adapter until it receives a Hot Plug Acknowledgment Packet for the previous Hot Plug/Unplug Event.

After receiving a Hot Plug Acknowledgment Packet, a Router shall not send any additional Hot Plug Event Packets for that Hot Plug/Unplug Event. A Router shall ignore a Hot Plug Acknowledgment Packet for a Hot Plug/Unplug Event that was already acknowledged.

A Router shall not generate two consecutive Hot Plug Events or two consecutive Hot Unplug Events for a given Adapter. The next event after a Hot Plug Event for a given Adapter shall always be a Hot Unplug Event. Similarly, the next event after a Hot Unplug Event for a given Adapter shall always be a Hot Plug Event.

A Router shall always report a Hot Plug Event or a Hot Unplug Event. When a Hot Plug Event Packet cannot be sent, the Router shall store the event and shall send Hot Plug Event Packet when conditions allow.



IMPLEMENTATION NOTE

Some Hot Plug Events can cancel each other out and thus do not require storage. For example, if an Adapter detects a Hot Plug then a Hot Unplug before a Hot Plug Event Packet was sent for the first Hot Plug, there is no need to send Hot Plug Event Packets for either the hot plug or the hot unplug.



CONNECTION MANAGER NOTE

A Connection Manager shall send a Hot Plug Acknowledgment Packet in response to a Hot Plug Event Packet. It does not have to send the Hot Plug Acknowledgment Packet within a specific time after receiving the Hot Plug Event Packet. However, a Router will continue to resend a Hot Plug Event Packet and will not send any new Hot Plug Event Packets until it receives a Hot Plug Acknowledgment Packet.

A Connection Manager can send one Hot Plug Acknowledgement Packet per Hot Plug or Hot Unplug Event (regardless of the number of Hot Plug or Hot Unplug Event Packets received for that event) or it can send a Hot Plug Acknowledgement Packet for each Hot Plug/Unplug Packet. A Connection Manager shall respond to Hot Plug Event Packets from a Router in the order received.

6.8.1 Router Hot Plug

Router Hot Plug handling for Routers that detect a Router Hot Plug on a Downstream Facing Port is described in Sections 6.8.1.1 and 6.8.1.2 respectively for Routers in the Enumerated and Uninitialized states. Section 6.8.1.3 describes how a newly connected Router handles a Router Hot Plug.

6.8.1.1 Enumerated Routers

When a Router in the Enumerated state detects a Router Hot Plug on one of its Downstream Facing Ports (See Section 4.1.2.2), it shall perform the following steps:

1. Perform Lane Initialization on the Lanes of the Downstream Facing Port with the Hot Plugged Router. See Section 4.1.2 for more information on Lane Initialization.
2. For each Adapter in the USB4 Port that reaches CL0 state, send a Hot Plug Event Packet with the *UPG* bit set to 0b to the Connection Manager.
3. If one of the Adapters in the USB4 Port does not reach CL0 state within *tTrainingAbort1* time after entering the Training state and the “Hot Plug Failure Indication” capability is enabled in the Router (see Section 8.3.1.3.2.1), then the Router shall send a Notification Packet with Event Code = *ERR_PLUG* as defined in Table 6-12.

6.8.1.2 Uninitialized Routers

When a Router in the Uninitialized state detects a Router Hot Plug, it shall not send a Hot Plug Event Packet until it transitions to the Enumerated state. After transitioning to the Enumerated state, the Router shall follow the procedure in Section 6.8.1.1 for each connected Adapter in the Downstream Facing Port.

6.8.1.3 Hot Plugged Router

A hot plugged Router shall enable the following for HopID 0:

- Forwarding of Control Packets to and from the Control Adapter.

- Egress scheduling.

6.8.2 Router Hot Unplug

Section 6.8.2.1 describes how a Router handles a Hot Unplug on the Upstream Facing Port. Section 6.8.2.2 describes how a Router handles a Hot Unplug on a Downstream Facing Port.

6.8.2.1 Hot Unplug on the Upstream Facing Port

If a Router is still powered on after being unplugged, it shall initiate a disconnect on the Upstream Facing Port by driving its SBTX line low (see Section 4.4.5.1.1).

6.8.2.2 Hot Unplug on a Downstream Facing Port

When a Router detects a Router Hot Unplug on a Downstream Facing Port, it shall initiate a disconnect on the Downstream Facing Port by driving its SBTX line low (see Section 4.4.5.2.1).

If the Router is not enumerated, it shall not send a Hot Plug Event Packet.

6.9 Downstream Facing Port Reset

When the *Downstream Port Reset* bit in a Downstream Facing Port is set to 1b, a Router shall discard any pending Transactions on the Sideband Channel and initiate a disconnect on the Downstream Facing Port by driving its SBTX line low. See Section 4.4.5.1.1 for disconnect when Link Partner is an Upstream Facing Port and Section 4.4.5.2.1 for disconnect when Link Partner is a Downstream Facing Port.

The Router shall drive the SBTX line high when the *Downstream Port Reset* bit of the Downstream Facing Port is set to 0b. Lane Initialization then takes place. A Router shall be ready for the *Downstream Port Reset* bit to be set to 0b *tClearDPR* time after the *Downstream Port Reset* bit is set to 1b.



CONNECTION MANAGER NOTE

A Connection Manager should use a Downstream Port Reset to change Link Parameters. To change Link Parameters, the Connection Manager sets one or more of the following fields in the Adapter Configuration Space of the Downstream Facing Port, then initiates a Downstream Facing Port Reset:

- *Target Link Speed field initiates a change in speed.*
- *Request RS-FEC Gen 2 bit initiates a change in RS-FEC at Gen 2 speeds.*
- *Request RS-FEC Gen 3 bit initiates a change in RS-FEC at Gen 3 speeds.*



CONNECTION MANAGER NOTE

*A Connection Manager shall not set the Downstream Port Reset bit to 0b less than 10 ms (*tClearDPR* max time) after setting the Downstream Port Reset bit to 1b. It is recommended that a Connection Manager execute the following steps when performing a Downstream Facing Port Reset:*

1. *The Connection Manager sets the Downstream Port Reset bit of a Downstream Facing Port to 1b.*
2. *The Connection Manager waits for at least 10 ms.*
3. *The Connection Manager sets the Downstream Port Reset bit of the Downstream Facing Port to 0b.*

6.10 Host Router Reset

A Connection Manager initiates a Host Router reset by setting the *Host Router Reset* bit to 1b in a Host Router.

A Host Router shall perform the following after the Connection Manager initiates a Host Router reset:

- Transition to the Uninitialized Plugged state (see Section 6.3).
- Discard all Transport Layer Packets.
- Remove all Tunneled Paths.
- Discard any completions received for read requests to host memory.
- Disconnect each Downstream Facing Port by driving SBTX to a logical low state for tDisconnectTx.
- Restore all Configuration Spaces to their default values, except the following:
 - The *Target Link Speed* field, *Request RS-FEC Gen 2* bit, and *Request RS-FEC Gen 3* bit shall maintain their value prior to the reset.
- Restore the Host Interface registers and the E2E flow control counters to their default values.
- De-allocate any assignment of DP stream resources to DP IN Adapters.

Note: A Host Router reset is confined to the Host Router within a USB4 Host. The Host Router reset does not reset any other components in the USB4 Host such as the internal USB3 Host Controller, USB 2.0 Host, the non-tunneled USB data path, DP Source, or PCIe Controller (see Figure 2-1 for an example of a USB4 Host showing these components).

A Host Router shall complete a Host Router reset within tHRReset time after the *Host Router Reset* bit is set to 1b. It is recommended that a Host Router complete a Host Router reset within 200 ms whenever possible. The Host Router shall set the *Host Router Reset* bit to 0b once the Host Router reset is complete.

After the Host Router sets the *Host Router Reset* bit to 0b, it shall not do any of the following:

- Issue Notification Packets for events that occurred prior to the Host Router reset.
- Retransmit a Notification Packet for events that occurred prior to the Host Router reset.
- Issue responses for Control Packets received prior to the Host Router reset.



CONNECTION MANAGER NOTE

The Connection Manager shall disable all Transmit Descriptor Rings and wait for at least 1 millisecond prior to setting the Host Router Reset bit to 1b. After the Connection Manager sets the Host Router Reset bit to 1b, it shall not access the Receive Descriptor Rings until the Host Router Reset bit is set to 0b. After a Connection Manager initiates a Host Router reset, it is not guaranteed that responses arrive for any outstanding Transactions on the Sideband Channel.

A PCIe Host Router shall:

- Initiate a Host Router reset when the *Host Router Reset* bit in the Host Interface Adapter Layer (Section 12.6.3.1.2) is set to 1b.
- Restore the contents of the Host Interface Memory BAR space, other than the *Host Router Reset* register (see Section 12.6.3.1.2), to its default state.
- Set the *Host Router Reset* bit to 0b when the Host Router completes its reset operation.

The PCI Endpoint within the Host Router shall not be reset, including its PCI configuration space and MSI/MSI-X Capability Structures.



CONNECTION MANAGER NOTE

A Connection Manager shall not write to any registers in the Host Interface Memory BAR space while a Host Router reset is in progress. Router behavior is not defined if the Memory BAR space is written to during a Host Router reset.

While the Host Router Reset bit is set to 1b, the read value of registers in the Host Router Memory BAR space (with the exception of the Host Router Reset register) is undefined.

6.11 Timing Parameters

Table 6-13 lists the timing parameters for the Configuration Layer.

Table 6-13. Configuration Layer Timing Parameters

Parameter	Description	Min	Max	Units
tCPResponse	The time between receiving a Control Packet and sending a response.	--	2	ms
tCPForward	The time between receiving a Control Packet and forwarding it on an Egress Adapter.	--	500	μs
tHRReset	The time to complete a Host Router reset.	---	500	ms
tSetRR	The time from when the <i>TopologyID Valid</i> bit is set to 1b to when the <i>Router Ready</i> bit is set to 1b.	--	50	ms
tSetCR	The time from when the <i>Configuration Valid</i> bit is set to 1b to when the <i>Configuration Ready</i> field is set to 1b.	--	50	ms
tClearDPR	Time from when the <i>Downstream Port Reset</i> bit is set to 1b to when the Router is ready for the <i>Downstream Port Reset</i> bit to be set to 0b.	--	10	ms

7 Time Synchronization

The Time Synchronization Protocol provides a mechanism for synchronizing the real-time clocks and absolute time of connected Routers to a high degree of accuracy and precision.

A Router with one or more Downstream Facing Port shall support the Time Synchronization Protocol described in this chapter.

A Router that supports one or more of the following shall support the Time Synchronization Protocol described in this chapter:

- DP tunneling
- USB3 tunneling with exposed USB3 downstream Port(s)
- PCIe tunneling that supports PTM

A Router that does not support the Time Synchronization Protocol shall set the *Time Synchronization Protocol Not Supported* bit in the TMU Router Configuration Capability to 1b.



CONNECTION MANAGER NOTE

When enumerating a Router, if the Time Synchronization Protocol Not Supported bit is set to 1b, the Connection Manager shall not enable TMU on the Downstream Facing Port connected to this Router's Upstream Facing Port.

A Router shall implement the TMU Router Configuration Capability and the TMU Adapter Configuration Capability as described in Sections 8.2.1.2 and 8.2.2.2.



IMPLEMENTATION NOTE

A Peripheral Device Router that does not tunnel any time sensitive protocols does not need the Time Synchronization Protocol for its operation. However, it does need to implement the TMU registers because a Connection Manager may require them in order to enumerate the Router, regardless of whether or not the Time Synchronization Protocol is supported. The TMU registers in a Router that does not support the Time Synchronization Protocol may be set to their default values and have Read Only access.

Support for Inter-Domain Time Synchronization is optional for a Host Router. A Host Router that does not support Inter-Domain Time Synchronization shall set the *IDNS* bit in the TMU Router Configuration Capability to 1b. A Host Router that does not support Inter-Domain Time Synchronization can still be the Inter-Domain Time Source for a Host Router that support InterDomain Time Synchronization.

7.1 Time Synchronization Architecture

The Time Synchronization Protocol is a distributed protocol that defines how the real-time clocks in a USB4 Fabric synchronize with each other. The real-time clocks are organized into a hierarchy with the Host Router at the top of the hierarchy determining the reference time for the entire Domain. Clock synchronization is achieved by exchanging Ordered Sets and Time Sync Packets where downstream USB4 Hubs and USB4 Peripheral Devices use both local timestamps and the timing information in the Time Sync Packets to adjust their clocks to the time of the Host Router.

When Inter-Domain time synchronization is disabled, the Time Synchronization Protocol executes within the scope of a single Domain. All Time Sync Packets, state machines and other entities are associated with a single Domain. The time established within one Domain by the protocol is independent of the time in other Domains.

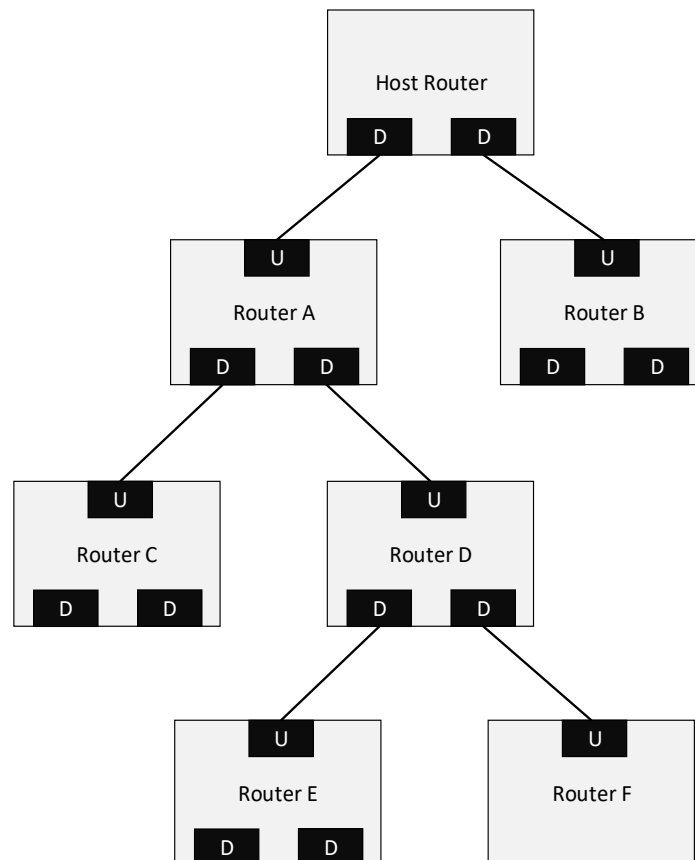
When Inter-Domain time synchronization is enabled, the Time Synchronization Protocol executes within the scope of an interconnected set of Domains. The Connection Managers of the Domains establish an Inter-Domain clock synchronization hierarchy by selecting one of the Host Routers to be the time source for all Domains. The Time Synchronization Protocol then synchronizes the clocks of the other Domains to the Inter-Domain Host Router clock.

7.1.1 Synchronization Hierarchy

7.1.1.1 Intra-Domain Hierarchy

Figure 7-1 shows an example of the time synchronization hierarchy within a Domain. The time synchronization hierarchy follows the Spanning Tree of the Domain. The Host Router of the Domain provides the clock for the Domain.

Figure 7-1. Time Synchronization Hierarchy within a Domain (Informative)



7.1.1.2 Inter-Domain Hierarchy

When multiple Domains are connected together, each Domain is synchronized to its own Host Router Clock. The Connection Managers of the Domains then enable time synchronization across the Domains. If there are more than one Inter-Domain Links between two Domains, then only one Inter-Domain Link is enabled to perform Time Sync handshakes.

When time synchronization is enabled across an Inter-Domain Link, one Domain is the Time Source and the other Domain follows. The Time Source Domain has the *IDTR* (Inter-Domain Time Responder) bit in the TMU Adapter Configuration Capability set to 1b and the *IDTI* (Inter-

Domain Time Initiator) bit set to 0b. The Domain that follows the Inter-Domain Host Router Time, has the *IDTI* bit set to 1b and *IDTR* bit set to 0b.

In the case where there are multiple daisy-chained Domains connected to one another, the overall Inter-Domain topology follows a Spanning Tree similar to the Intra-Domain hierarchy. The hierarchy between Domains is determined by the *IDTR* and *IDTI* bits.

7.1.2 Time Sync Parameters

7.1.2.1 Local Time

A Router shall provide a free-running clock for use in capturing the time stamps needed for the Time Synchronization Protocol. This free-running clock is called the Local Clock. The Local Clock shall run at a frequency of 125 MHz or greater with an accuracy of +/- 100ppm relative to the nominal Local Clock frequency. The Local Clock shall not be spread-spectrum.

A Router shall use an 80-bit Local Time counter with the format shown in Figure 7-2 to track Local Time. The *Nanoseconds* field represents the number of whole nanoseconds and the *Fractional Nanoseconds* field represents a fraction of a nanosecond that is less than 1. For example, a Local Time value of 524.25 is stored as 0...020C4000h.

The Local Time counter shall be incremented up with the Local Clock. The Local Time Counter shall not be cleared when the TMU is enabled. The Local Time counter holds an unsigned fractional value.

Figure 7-2. Local Time Counter Format



Note: If the Local Clock frequency is such that each tick cannot be represented fully with the Local Time Counter, it affects the overall accuracy of the Local Time Counter. For example, if the Local Clock frequency is 300 MHz, the period is 3.333... ns. The accuracy of each tick with ideal clock would be ~1.53 ppm.

7.1.2.2 Time Offset

The time offset between Local Time and Host Router Time is stored in the *TimeOffsetFromHR* register in the TMU Adapter Configuration Capability in Router Configuration Space. The *TimeOffsetFromHR* register shall have the format shown in Figure 7-3.

Figure 7-3. TimeOffsetFromHR Register Format



The *TimeOffsetFromHR* register holds a signed fractional value and uses 2's complement representation. For example, 2.5 ns is represented as 0000 0000 0002 8000h and -2.5 ns is represented as FFFF FFFF FFFD 8000h.

Note: A value of 7FFF FFFF FFFF FFFFh is used to indicate that the time offset is too big to be represented.

The *TimeOffsetFromHR* register shall be updated at the conclusion of every Time Sync Handshake.

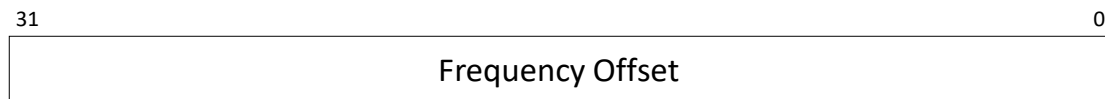
7.1.2.3 Frequency Offset

The frequency offset between the Local Clock and the Host Router Clock is stored in the *FreqOffsetFromHR* register in the TMU Adapter Configuration Capability in Router Configuration Space. The *FreqOffsetFromHR* register holds the frequency offset as a signed fractional value represented using 2's complement notation. The frequency offset shall be computed according to Equation 7-4.

For example, a frequency offset of 1ppm is represented as $F = 218DEFh$ in the *FreqOffsetFromHR* register.

The *FreqOffsetFromHR* register shall be updated at the conclusion of every Time Sync Handshake.

Figure 7-4. *FreqOffsetFromHR* Register Format



7.2 Time Stamp Measurement

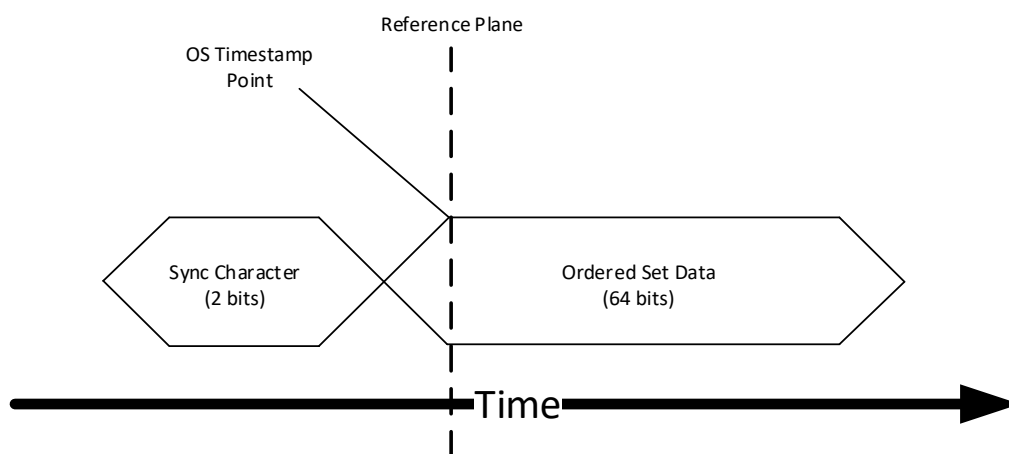
Section 7.2.1 defines the time stamp measurement requirements for a Gen 2 or Gen 3 Link. Section 7.2.2 defines the time stamp measurement requirements for a Gen 4 Link.

7.2.1 Time Stamp Measurement for Gen 2 and Gen 3 Links

A USB4 Port shall generate a time stamp whenever it either sends or receives a Time Sync Notification Ordered Set (TSNOS). The USB4 Port shall use the value in the Local Time counter to capture time stamps.

The start of the first bit of the TSNOS is referred to as the Time Stamp Point. This applies to both Single-Lane Links and Symmetric Links. A time stamp shall be taken at the Time Stamp Point of the First TSNOS. If one or more back-to-back TSNOS are received immediately after the first TSNOS, they shall be ignored. The same transmit reference plane shall be used for all transmitted TSNOS and the same receive reference plane shall be used for all received TSNOS. However, the reference plane may be different for the transmit and receive Paths through the Physical Layer. The time stamp measurement shall have a resolution of at least 8 ns (i.e. the period of the Local Clock).

Figure 7-5. Time Measurement Model for 64/66b Encoding



The time stamp in a Time Sync Packet shall have the format shown in Figure 7-2.

7.2.2 Time Stamp Measurement for Gen 4 Links

A Downstream Facing Port shall generate a Time Stamp Point periodically every *AdapterTimeSyncInterval* as configured in the TMU_ADP_CS_9 register. An Upstream Facing Port shall generate a Time Stamp Point when it instructs the Logical Layer to send a Gen 4 Time Sync Notification Ordered Set (Gen 4 TSNOS). All USB4 Ports shall generate a timestamp when they receive a Gen 4 TSNOS. A USB4 Port shall use the value in the Local Time counter to capture timestamps.

A Downstream Facing Port shall send 24 Gen 4 TSNOS at the start of the next RS-FEC block after the Time Stamp Point. An Upstream Facing Port shall send 24 Gen 4 TSNOS at the start of the next RS-FEC block after receiving an indication to send the Gen 4 TSNOS. The *Symbols Delay* field shall have the same value in all 24 Gen 4 TSNOS. The *Symbols Delay* field shall not exceed 1000.

When a USB4 Port detects a Gen 4 TSNOS, the Time Stamp Point is a combination of the first bit of the RS-FEC block on which the Gen 4 TSNOS was received and the *Symbols Delay* field within the Gen 4 TSNOS.

Figure 7-6. Example of a Symbols Delay Calculation

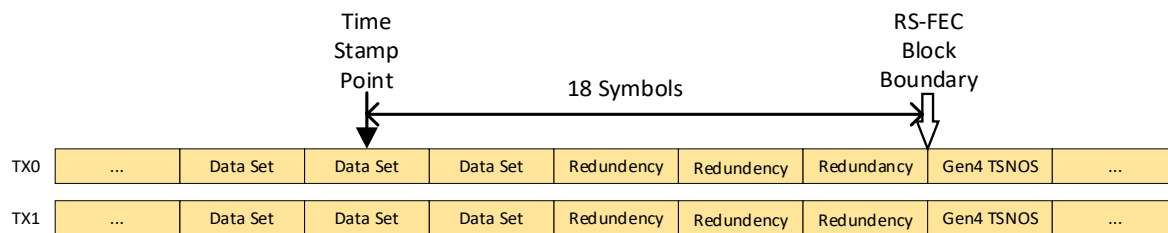


Figure 7-6 shows an example of a Gen 4 TSNOS sent after the Time Stamp Point occurred in the previous RS-FEC block time frame. The Gen 4 TSNOS is sent at the beginning of the next RS-FEC block. In this example, the *Symbols Delay* field in the Gen 4 TSNOS is set to 18 since the time from the Time Stamp Point to the beginning of the RS-FEC block is 18 Symbol Time.

The same transmit reference plane shall be used for all transmitted Gen 4 TSNOS. The same receive reference plane shall be used for all received Gen 4 TSNOS. However, the reference plane may be different for transmit and receive Paths through the Physical Layer. The time stamp measurement shall have a resolution of at least 8 ns (i.e. the period of the Local Clock).

7.2.3 Asymmetry Corrections

Time stamps shall be corrected for asymmetry between transmit and receive Paths. An Upstream Facing Port shall correct for asymmetry by performing the following computations:

$$t1 = \text{Delay Request Sent Time Stamp} + \text{TxTimeToWire}$$

$$t4 = \text{Delay Response Received Time Stamp} - \text{RxTimeToWire}$$

$$tu1 = \frac{\text{Delay Request Received Time Stamp} - \text{RxTimeStamp}}{\text{RxTimeToWire}} - (\text{Symbols Delay}) \times (\text{Symbol Time}) -$$

$$tu2 = \text{Delay Response Sent Time Stamp} + \text{TxTimeToWire}$$

where, TxTimeToWire is the value in the *TxTimeToWire* field of the TMU_ADP_CS_1 register of the Upstream Facing Port, RxTimeToWire is the value in the *RxTimeToWire* field of the TMU_ADP_CS_2 register of the Upstream Facing Port, and RxTimeStamp is defined below for each Link speed.

Note: The reference plane is a virtual representation of the RX and TX pipeline depth. The reference plane is constant regardless of whether or not RS-FEC is activated.

A Downstream Facing Port shall correct for asymmetry by performing the following computations:

$t2 = \text{Delay Request Received Time Stamp} - \text{RxTimeToWire}$

$t3 = \text{Delay Response Sent Time Stamp} + \text{TxTimeToWire}$

$td1 = \text{Delay Request } \textcolor{red}{\text{Sent}} \text{ Time Stamp} + \text{TxTimeToWire}$

$td2 = \text{Delay Response Received } \textcolor{red}{\text{Rx}} \text{Time Stamp} - (\text{Symbols Delay}) \times (\text{Symbol Time}) - \text{RxTimeToWire}$

where, TxTimeToWire is the value in the *TxTimeToWire* field of the TMU_ADP_CS_1 register of the Downstream Facing Port, RxTimeToWire is the value in the *RxTimeToWire* field of the TMU_ADP_CS_2 register of the Downstream Facing Port, and RxTimeStamp is defined below for each Link speed.

For a Gen 2 or Gen 3 Link:

- The time duration between when a USB4 Port generates a time stamp and when it transmits first bit of a TSNOS on the wire shall be equal to the value in the *TxTimeToWire* field of the TMU_ADP_CS_1 register.
- The time duration between when a USB4 Port receives the first bit of a TSNOS on the wire and when it generates a time stamp shall be equal to the value in the *RxTimeToWire* field of the TMU_ADP_CS_2 register.
- ~~RxTimeStamp~~ Point is define in Section 7.2.1.
- Symbols Delay is 0.

For a Gen 4 Link:

- The time duration between when a USB4 Port generates a Time Stamp Point and when it transmits first bit of a TSNOS on the wire shall be calculated using Equation 7-1.

Equation 7-1. Time Difference from Time Stamp Point to TSNOS Transmission

$$\Delta T = (\text{Symbols Delay}) \times (\text{Symbol Time}) + \text{TxTimeToWire}$$

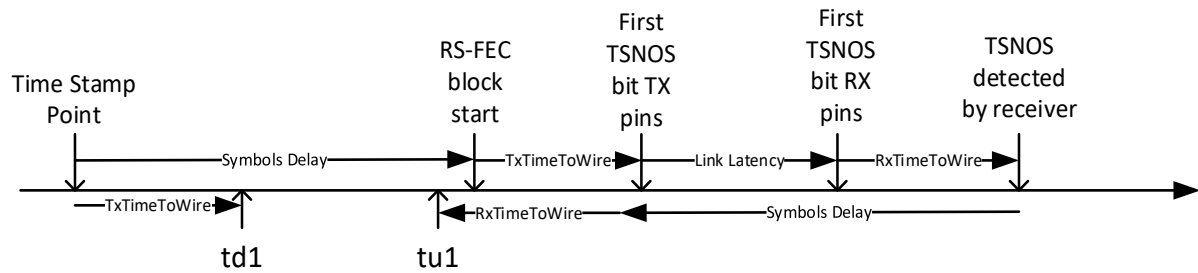
~~RxTimeStamp is the time when a USB4 Port detects the first TSNOS, subtracted by the value of the Symbols Delay field multiplied by the Symbol Time.~~

- The time duration between when a USB4 Port receives the first bit of a TSNOS on the wire and when it generates a Time Stamp Point shall be calculated using Equation 7-2.

Equation 7-2. Time Difference from TSNOS Reception to Time Stramp Point

$$\Delta T = (\text{Symbols Delay}) \times (\text{Symbol Time}) + \text{RxTimeToWire}$$

Figure 7-7 shows an example of how a Downstream Facing Port and an Upstream Facing Port use the TSNOS to generate time stamps for a Gen 4 Link.

Figure 7-7. Time Stamp Generation using TSNOS for a Gen 4 Link

Note: The values in the TxTimeToWire and RxTimeToWire fields are vendor defined.



IMPLEMENTATION NOTE

The values of the TxTimeToWire and RxTimeToWire may differ when the Link is operating at different speeds or is on different configurations (e.g. RS-FEC on/off, number of Lanes enabled, and Symmetric/Asymmetric Link).

7.3 Time Sync Protocol

7.3.1 Time Sync Handshake

The Time Sync Handshake is used to measure the time offset between two USB4 Ports.

For a Gen 2 or Gen 3 Link, there are three types of Time Sync Handshakes: Bi-Directional, Uni-Directional and Enhanced Uni-Directional. Bi-Directional Time Sync Handshakes are described in Section 7.3.1.1. Uni-Directional Time Sync Handshakes are described in Section 7.3.1.2. Enhanced Uni-Directional Time Sync Handshakes are described in Section 7.3.1.3.

For a Gen 4 Link, a USB4 Port uses Enhanced Uni-Directional Time Sync Handshakes, which are described in Section 7.3.1.3.

Bi-Directional Time Sync Handshakes only use HiFi Mode. Uni-Directional Time Sync Handshakes can use HiFi Mode or LowRes Mode. The mode is configured using the *TSPacketInterval* field.

Enhanced Uni-Directional Time Sync Handshakes use HiFi Mode. The mode is configured using the *AdapterTimeSyncInterval*, *ReplenishN*, *ReplenishTimeout*, and *ReplenishThreshold* fields.

A Router shall support Bi-Directional Time Sync Handshakes in HiFi Mode. A Router shall support Uni-Directional Time Sync Handshakes in HiFi Mode and LowRes Mode. A Router shall support Enhanced Uni-Directional Time Sync Handshake in HiFi Mode.



CONNECTION MANAGER NOTE

When using Bi-Directional Handshakes, a Router only support HiFi Mode. A Connection Manager shall not configure a Router in LowRes Mode when using Bi-Directional Handshakes.



IMPLEMENTATION NOTE

A Link cannot enter a Low Power state when Bi-Directional Time Sync Handshakes are enabled in HiFi Mode (the handshake frequency is too high to allow time for Low Power state entry and exit). Because of this, a Device Router should only request Bi-Directional HiFi Mode if it is absolutely required for device functionality (e.g. a USB4 Device that uses

PCIe PTM for audio and requires higher accuracy than Uni-Directional HiFi Mode can support). A Device Router uses DROM to indicate which type of Time Sync Handshakes it needs to operate. See the USB4 DROM Specification for more details.

A Time Sync Handshake uses three types of Time Sync Messages: Delay Request Message, Delay Response Message, and Follow-Up Packet. The Delay Request and Delay Response Messages are implemented using the TSNOS described in Section 7.3.3.1. A Follow-Up Packet is a Transport Layer Packet and has the format described in Section 7.3.3.2.

A Time Sync Handshake takes place between two USB4 Ports as follows:

- When the USB4 Ports are connected by a Single-Lane Link, a Time Sync Handshake shall occur over that Link.
- When the USB4 Ports are connected by an Aggregated Link, the Delay Request and Delay Response Ordered Sets in the Time Sync Handshake shall be sent on both Lane 0 and Lane 1. The Follow-Up Packet shall be sent using both Lanes. The timestamp shall be calculated based on the time when the first Ordered Set from the Link Partner is received.
- For a Gen 2 or Gen 3 Link, a Receiver shall ignore a TSNOS that arrives back-to-back after another TSNOS.



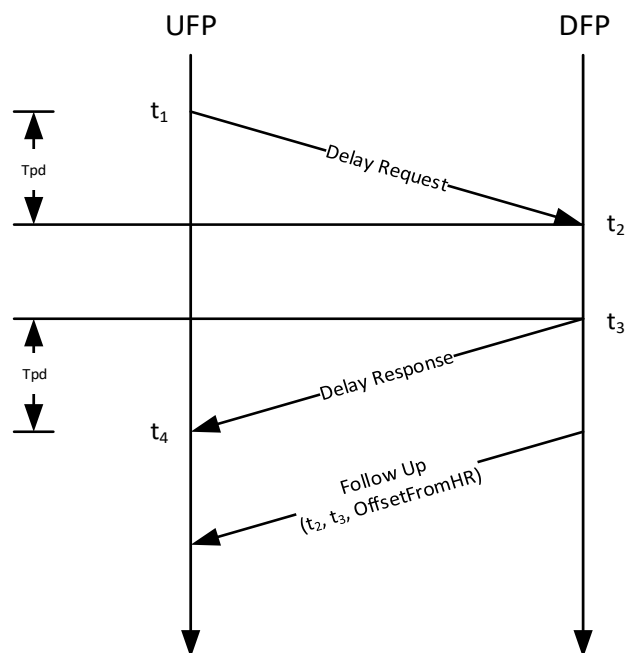
CONNECTION MANAGER NOTE

When configuring a USB4 Port for a Single-Lane Link, a Connection Manager shall disable the Lane 1 Adapter, before enabling Time Sync Handshakes.

7.3.1.1 Bi-Directional Time Sync Handshake

Figure 7-8 shows a Bi-Directional Time Sync Handshake.

Figure 7-8. Bi-Directional Time Sync Handshake



A Downstream Facing Port shall not initiate a Bi-Directional Time Sync Handshake.

An Upstream Facing Port shall send a Delay Request to the Downstream Facing Port at the interval specified in the *TSPacketInterval* field in the *TMU_RTR_CS_3* register in Router Configuration Space. A Downstream Facing Port shall transmit a Delay Response Message within *RespTimeout* time of receiving a Delay Request Message. A Downstream Facing Port shall transmit a Follow-Up Packet within *SendTimeout* time of transmitting the associated Delay Response Message.

Note: A Connection Manager can control the Time Sync Handshake rate by writing to the TSPacketInterval field in the TMU_RTR_CS_3 register in Router Configuration Space.

An Upstream Facing Port shall generate time stamp t_1 upon transmission of a Delay Request and shall generate time stamp t_4 upon reception of a Delay Response. A Downstream Facing Port shall generate time stamp t_2 upon receipt of a Delay Request and shall generate time stamp t_3 upon transmission of a Delay Response. Section 7.2 defines how time stamps are measured. Section 7.2.3 defines how timestamps are corrected for asymmetry. Transmission and reception of a Follow-Up Packet does not result in the generation of time stamps.

If an error occurs during the transmission or reception of a Time Sync Packet, the entire Time Sync Handshake shall be voided (i.e. neither time stamps nor values from the Follow-Up Packet shall be used).

Figure 7-9 shows the state machine that is recommended for an Upstream Facing Port using Bi-Directional Time Sync Handshake. The state machine uses the following timeout values:

- *ReqTimeout* is the maximum time between a Time Sync event and transmission of Delay Request. See Table 7-1 for the recommended value.

Note: A Router assumes that the transmission of Delay Requests is constant and consistent. However, any variance in the time it takes to transmit Delay Request adds to overall noise. The purpose of ReqTimeout is to add robustness and make sure the state machine doesn't get stuck as a result of such noise.

- *RespTimeout* is the maximum time between sending a Delay Request and receiving a Delay Response. See Table 7-1 for the recommended value.
- *FPTimeout* is the maximum time between receiving a Delay Response and receiving a Follow-Up Packet. See Table 7-1 for the recommended value.

Table 7-1. Bidirectional UFP Timeout Values

Timeout Name	Timeout Recommended Value
<i>ReqTimeout</i>	1 μ s
<i>RespTimeout</i>	2 μ s
<i>FPTimeout</i>	10 μ s

Note: In the state machine shown in Figure 7-9 and Figure 7-10, a Link Event occurs when the USB4 Port receives an Ordered Set related to Link negotiation or training. A Time Sync Event occurs once every TSPacketInterval and indicates the start of a new Time Sync Handshake.

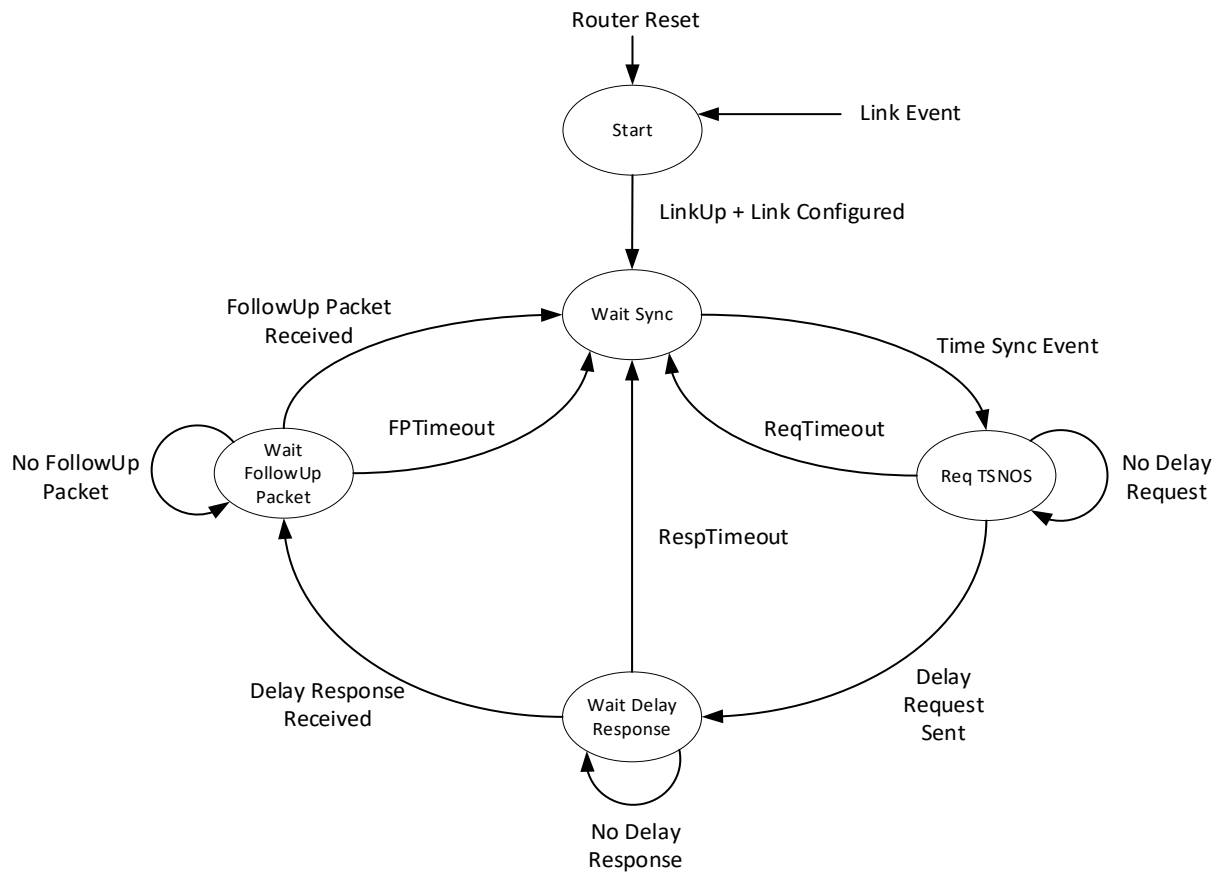
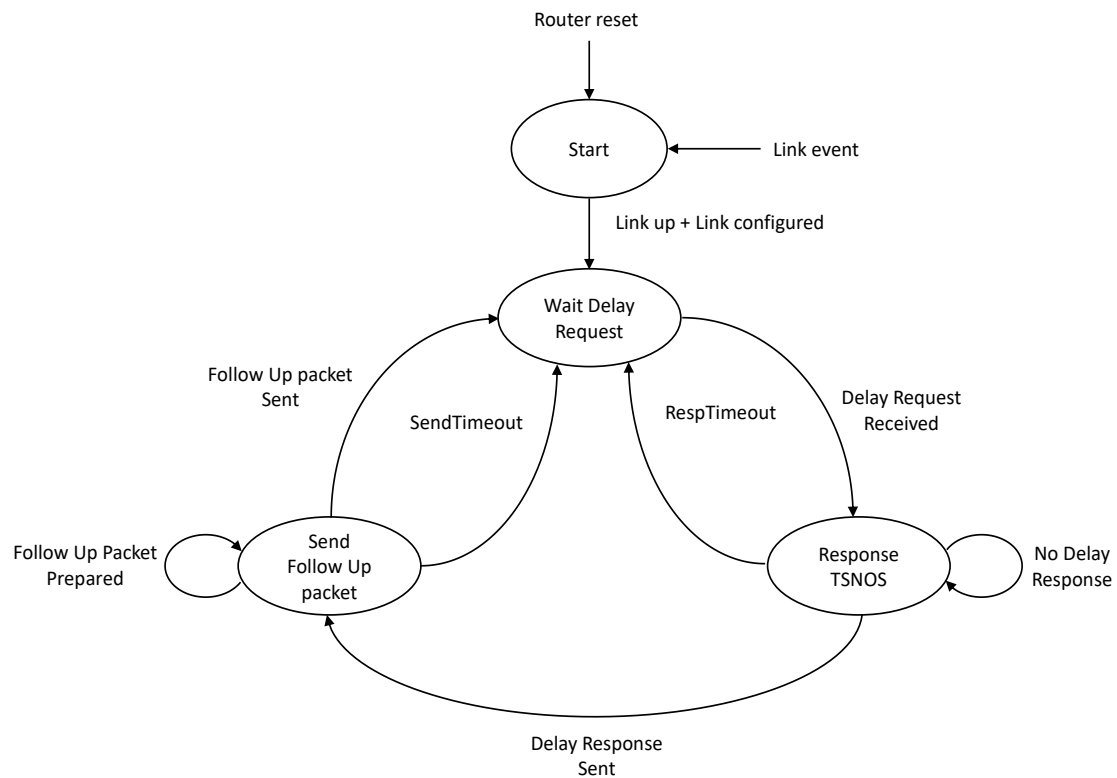
Figure 7-9. UFP State Machine for Bi-Directional Time Sync Handshake (Recommended)

Figure 7-10 shows the state machine that is recommended for a Downstream Facing Port using Bi-Directional Time Sync Handshake. The state machine uses the following timeout values:

- **RespTimeout** is the maximum time between receiving a Delay Request and sending a Delay Response. See Table 7-2 for the recommended value.
- **SendTimeout** is the maximum time between sending a Delay Response and sending a Follow-Up Packet. See Table 7-2 for the recommended value.

Table 7-2. Bidirectional DFP Timeout Values

Timeout Name	Timeout Recommended Value
RespTimeout	1 μ s
SendTimeout	8 μ s

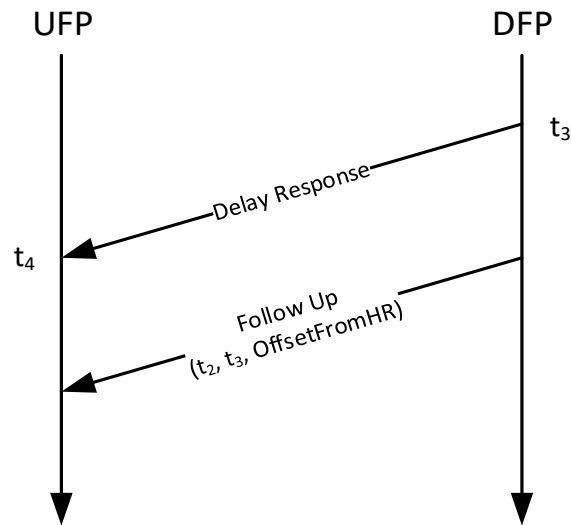
Figure 7-10. DFP State Machine for Bi-Directional Time Sync Handshake (Recommended)

When using Bi-Directional Time Sync Handshakes, a Downstream Facing Port shall do the following upon receiving a Delay Request:

1. Take the t_2 timestamp.
2. Send a Delay Response:
 - a. The Delay Response shall be sent within RespTimeout time after receiving the Delay Request.
 - b. The Downstream Facing Port shall take the t_3 timestamp upon transmitting the Delay Response.
3. Compute the updated TimeOffsetFromHR parameter according to Equation 7-9 using the t_3 timestamp from Step 2b.
4. Send a Follow-Up Packet with the TimeOffsetFromHR calculated in Step 3.

7.3.1.2 Uni-Directional Time Sync Handshake

The Uni-Directional Time Sync Handshake is shown in Figure 7-11.

Figure 7-11. Uni-Directional Time Sync Handshake

When using Uni-Directional Time Sync Handshakes, only the Downstream Facing Port shall initiate a Time Sync Handshake.

When the [Link Transmitter](#) is not in [CL2, CL1 or CL0s Tx-a Low Power state](#), a Downstream Facing Port shall send a Delay Response to the Upstream Facing Port at the interval specified in the *TSPacketInterval* field in the TMU_RTR_CS_3 register in Router Configuration Space. A Downstream Facing Port shall transmit a Follow-Up Packet within SendTimeout time after transmitting the associated Delay Response Packet.

When the Link is in a Low Power state, a Downstream Facing Port may “pause” Time Sync Handshakes by not sending a Delay Response to the Upstream Facing Port. The Downstream Facing Port may pause Time Sync Handshakes for any period of time while the Link is in the Low Power state. The Downstream Facing Port shall resume Time Sync Handshakes upon exiting the Low Power state.



IMPLEMENTATION NOTE

*Pausing Time Sync Handshakes affects time synchronization accuracy in an Upstream Facing Port. When resuming Time Sync Handshakes, the value of the timestamp in the first Follow Up Packet may not be as expected. Accuracy is not guaranteed until *tConvergeTime* after Time Sync Handshakes are resumed. It is important that a Router implementation take this into consideration when pausing and resuming Time Sync Handshakes in order to not disrupt tunneled traffic.*

When using Uni-Directional Time Sync Handshakes, the propagation delay (T_{pd}) between the Downstream Facing Port and Upstream Facing Port cannot be computed. Therefore, Uni-Directional Time Sync Handshakes are only intended for use when a constant time offset between Routers is not needed (e.g. video tunneling). The format of the Follow-Up Packet is the same as for Bi-Directional Time Sync Handshake, keeping *RequestReceiptTS* (t_2) and *ResponseOriginTS* (t_3) equal.

Uni-Directional Time Sync Handshakes shall be used when the following conditions are true:

- Both Link Partners support Uni-Directional Time Sync Handshakes.

- Both Link Partners have the *EnableUniDirectionalMode* field in the TMU_AD_P_CS_3 register in Adapter Configuration Space set to 1b.



CONNECTION MANAGER NOTE

When configuring a Link to use Uni-Directional Time Sync Handshakes, it is recommended that the *EnableUniDirectionalMode* field in the Upstream Facing Port be set to 1b before setting the *EnableUniDirectionalMode* field to 1b in the Downstream Facing Port.

Figure 7-12 shows the state machine that is recommended for a Downstream Facing Port using Uni-Directional Time Sync Handshakes.

Note: In the state machine shown in Figure 7-12, a Link Event occurs when the USB4 Port transmits an Ordered Set related to Link negotiation or training.

Figure 7-12. DFP State Machine for Uni-Directional Time Sync Handshake (Recommended)

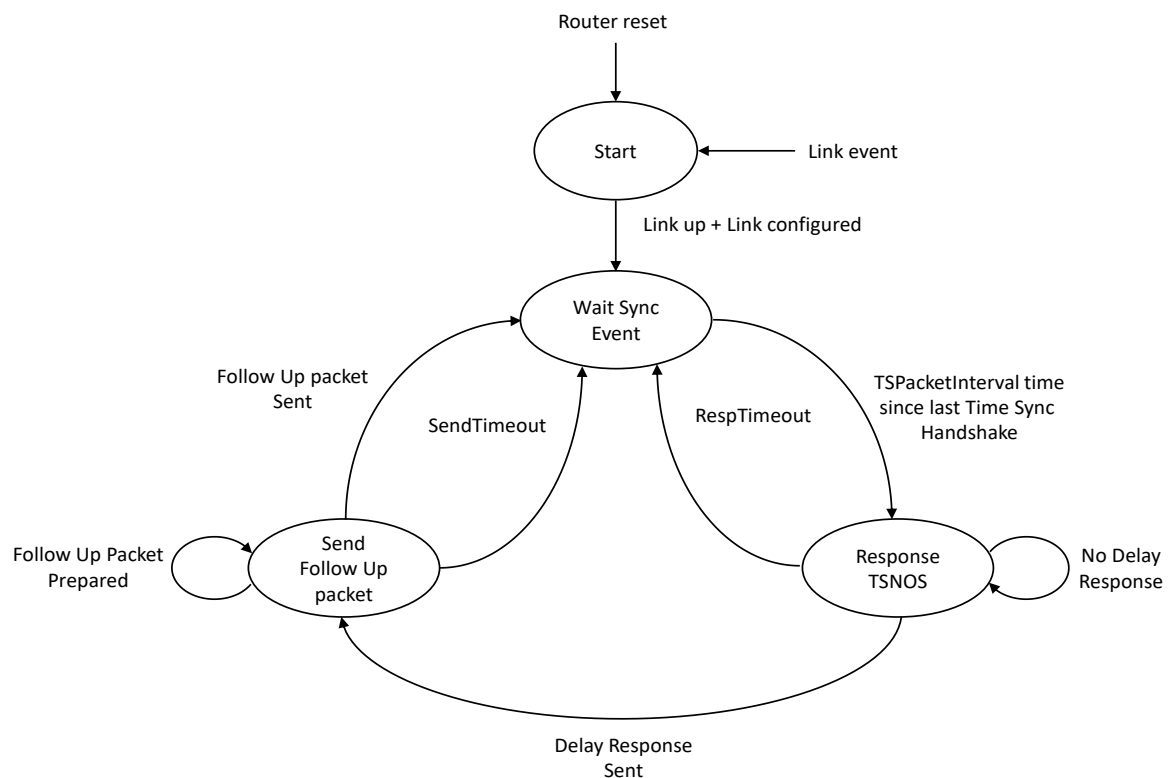


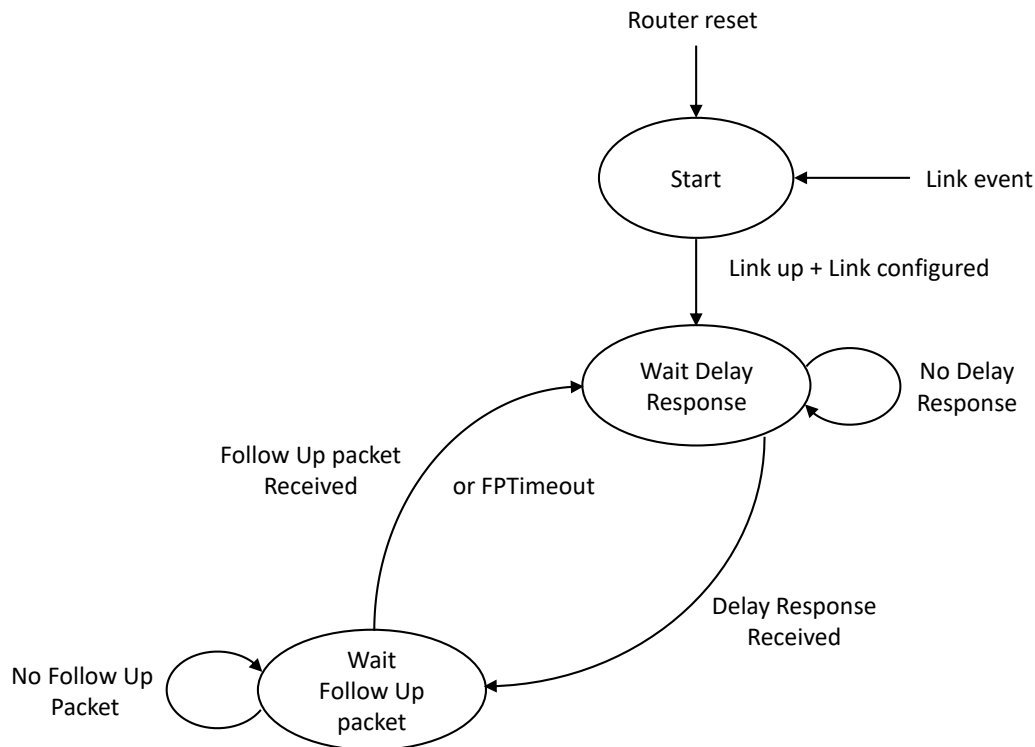
Figure 7-13 shows the state machine that is recommended for an Upstream Facing Port using Uni-Directional Time Sync Handshakes. The state machine uses the following timeout values:

- FPTimeout is the maximum time between receiving a Delay Response and receiving a Follow-Up Packet. See Table 7-5 for the recommended value.

Table 7-3. Uni-Directional UFP Timeout Values

Timeout Name	Timeout Recommended Value
FPTimeout	10 μ s

Note: In the state machine shown in Figure 7-13, a Link Event occurs when the USB4 Port receives an Ordered Set related to Link negotiation or training.

Figure 7-13. UFP State Machine for Uni-Directional Time Sync Handshake (Recommended)

7.3.1.3 Enhanced Uni-Directional Time Sync Handshake

When Enhanced Uni-Directional Time Sync Handshakes are enabled, the first *DirSwitchN* number of handshakes are initiated by the Downstream Facing Port. These handshakes use Inversed Bi-Directional mode, which is described in Section 7.3.1.3.1. After executing the first *DirSwitchN* handshakes in Inversed Bi-Directional mode, the Downstream Facing Port continues to initiate handshakes but transitions to Adaptive Uni-Directional mode, which is described in Section 7.3.1.3.2.



IMPLEMENTATION NOTE

There are Connection Managers in the eco-system that will enable Enhanced Uni-directional Time Sync when the Upstream Facing Port does not support TMU. This configuration may cause a scenario where the Downstream Facing Port will not receive any Delay Response. It is recommended that the Downstream Facing Port will move to Adaptive Uni-directional mode after transmitting DirSwitchN Delay Requests even if it didn't manage to complete DirSwitchN successful TMU handshakes.

Enhanced Uni-Directional Time Sync Handshakes shall be used when all the following conditions are true:

- The *Enable Enhanced Uni-Directional* bit in the TMU_ADAP_CS_8 register in the TMU Adapter Configuration Space is set to 1b.
- The *AdapterTimeSyncInterval* field in the TMU_ADAP_CS_9 register in the TMU Adapter Configuration Space is set to 16.

When using Enhanced Uni-Directional Time Sync Handshakes, only the Downstream Facing Port shall initiate a Time Sync Handshake. When a USB4 Port is using Enhanced Uni-Directional Time Sync Handshakes, it shall ignore the value of the *TSPacketInterval* in the TMU_RTR_CS_3 register.



CONNECTION MANAGER NOTE

When the Routers on both sides of a Link support Version 2.0 of the USB4 Specification and support TMU, a Ver. 2 Connection Manager shall enable Enhanced Uni-Directional Time Sync Handshakes.

Before enabling Enhanced Uni-Directional TMU, which begins with Inversed Bi-Directional mode, the Connection Manager will disable CLx states on both sides of the link. After enabling the TMU, the Connection Manager may enable CLx states 50ms later to avoid interference with Timing Convergence

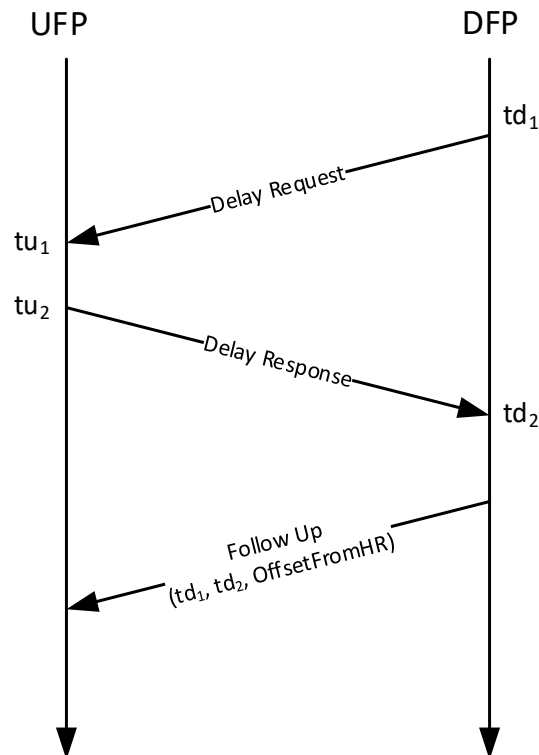
*When enabling Enhanced Uni-Directional Time Sync Handshakes, the Connection Manager shall configure the *AdapterTimeSyncInterval* field and Enable Enhanced Uni-Directional mode in the Upstream Facing Port before doing the same in the Downstream Facing Port.*

*A Router that only supports Version 1.0 of the USB4 Specification does not support Enhanced Uni-Directional Time Sync Handshakes. A Connection Manager shall not enable Enhanced Uni-Directional Time Sync Handshakes if either Router on the Link does not support Version 2.0 of the USB4 Specification. A Connection Manager can use the *USB4 Version* field in Router Configuration Space to determine what version of the USB4 Specification a Router supports.*

7.3.1.3.1 Inversed Bi-Directional Mode

A Downstream Facing Port shall send a Delay Request to the Upstream Facing Port at the interval specified in the *AdapterTimeSyncInterval* field in the TMU_ADP_CS_9 register in TMU Adapter Configuration Space. An Upstream Facing Port shall transmit a Delay Response within *RespTimeout* time of receiving a Delay Request. A Downstream Facing Port shall transmit a Follow-Up Packet within *SendTimeout* time of receiving the associated Delay Response. Both the Downstream Facing Port and Upstream Facing Port shall assert an objection to CLx states while the Time Sync Handshakes are in Inversed Bi-Directional mode.

Figure 7-23 shows the Inversed Bi-Directional Time Sync Handshake.

Figure 7-14. Inversed Bi-Directional Time Sync Handshake

A Downstream Facing Port shall generate time stamp td_1 upon transmission of a Delay Request and shall generate time stamp td_2 upon reception of a Delay Response.

An Upstream Facing Port shall generate time stamp tu_1 upon receipt of a Delay Request and shall generate time stamp tu_2 upon transmission of a Delay Response.

Section 7.2 defines how time stamps are measured. Section 7.2.3 defines how timestamps are corrected for asymmetry. Transmission and reception of a Follow-Up Packet does not result in the generation of time stamps.

If an error occurs during the transmission or reception of a Time Sync Packet, the entire Time Sync Handshake shall be voided (i.e. neither the time stamps nor the values from the Follow-Up Packet shall be used).

If the Downstream Facing Port sent DirSwitchN Delay Requests and did not receive any Delay Response it is recommended to transisiton to Adaptive Uni-directional mode.

Figure 7-15 shows the state machine that is recommended for a Downstream Facing Port using Inversed Bi-Directional Time Sync Handshakes. The state machine uses the following timeout values:

- ReqTimeout is the maximum time between a Time Sync event and transmission of Delay Request. See Table 7-4 for the recommended value.

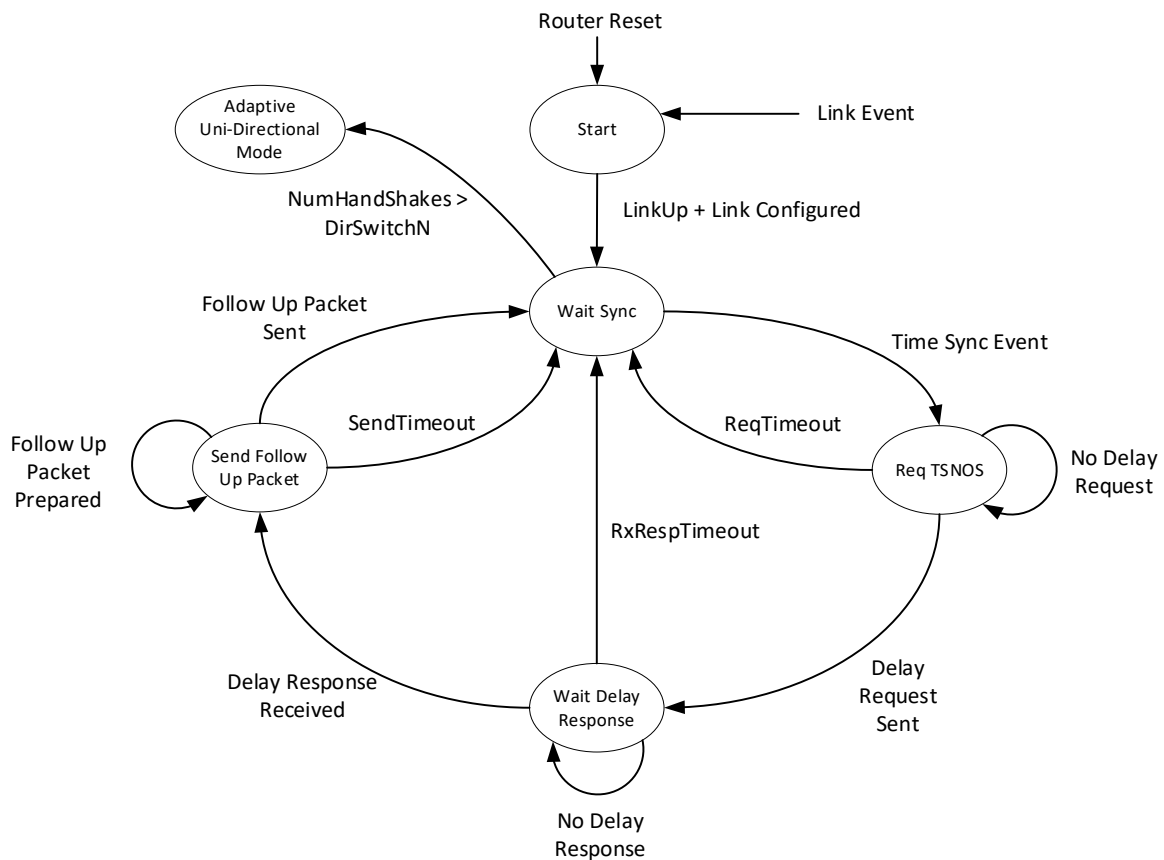
Note: A Router assumes that the transmission of Delay Requests is constant and consistent. However, any variance in the time it takes to transmit Delay Request adds to overall noise. The purpose of ReqTimeout is to add robustness and make sure the state machine doesn't get stuck as a result of such noise.

- RxRespTimeout is the maximum time between sending a Delay Request and receiving a Delay Response. See Table 7-4 for the recommended value.

- SendTimeout is the maximum time between receiving a Delay Response and sending a Follow-Up Packet. See Table 7-4 for the recommended value.

Table 7-4. Inversed Bi-Directional DFP Timeout Values

Timeout Name	Timeout Recommended Value
ReqTimeout	1 μ s
RxRespTimeout	2 μ s
SendTimeout	8 μ s

Figure 7-15. DFP State Machine for Inversed Bi-Directional Time Sync Handshake (Recommended)

When using Inversed Bi-Directional Time Sync Handshake, a Downstream Facing Port shall do the following upon receiving a Delay Response:

1. Take the td_2 timestamp.
2. Send a Follow-Up Packet with the calculated TimeOffsetFromHR. The value of the *S2U* (Switch to Uni-Directional) bit in the Follow-Up Packet shall be 0b for the first *DirSwitchN*-1 successful Handshakes. Otherwise, it shall be set to 1b.

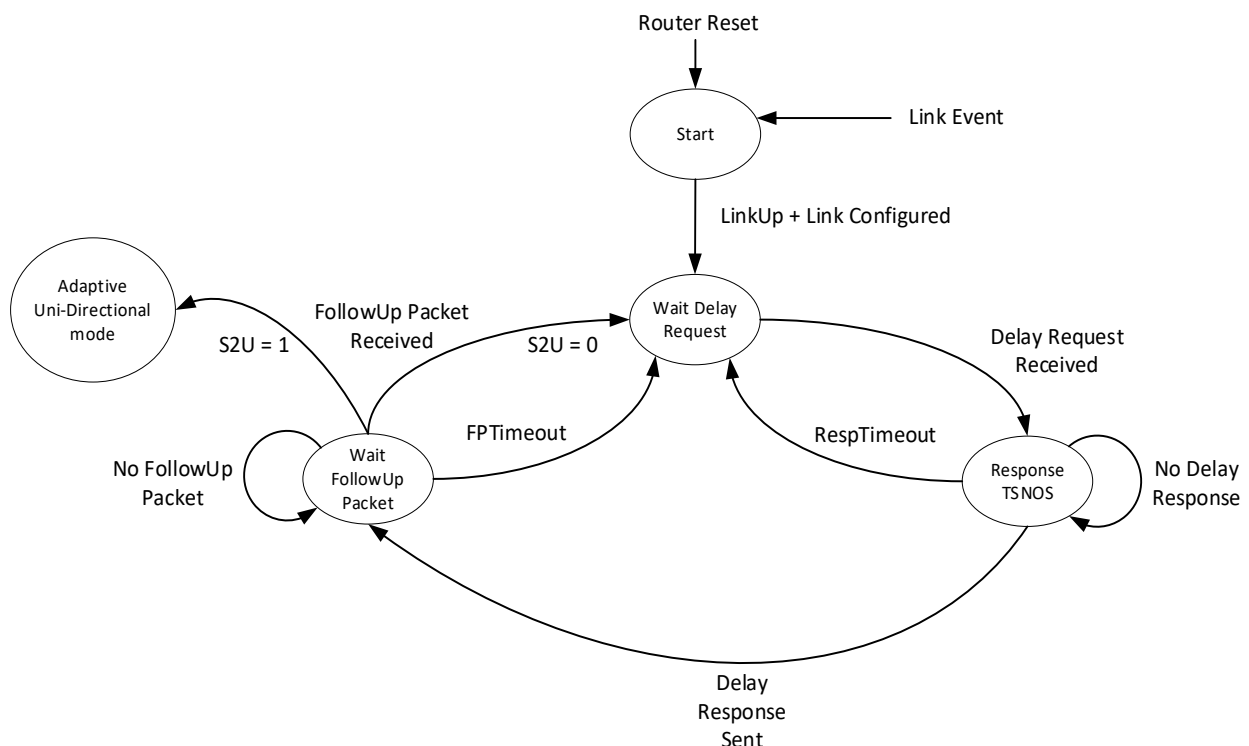
When an Upstream Facing Port receives a Follow-Up Packet with the *S2U* bit set to 1b, it shall transition to Adaptive Uni-Directional Mode.

Figure 7-16 shows the state machine that is recommended for an Upstream Facing Port using Inversed Bi-Directional Time Sync Handshake. The state machine uses the following timeout values:

- RespTimeout is the maximum time between receiving a Delay Request and sending a Delay Response. See Table 7-5 for the recommended value.
- FPTimeout is the maximum time between sending a Delay Response and receiving a Follow-Up Packet. See Table 7-5 for the recommended value.

Table 7-5. Inversed Bi-Directional UFP Timeout Values

Timeout Name	Timeout Recommended Value
RespTimeout	1 μ s
FPTimeout	10 μ s

Figure 7-16. UFP State Machine for Inversed Bi-Directional Time Sync Handshake (Recommended)

When using Inversed Bi-Directional Time Sync Handshake, an Upstream Facing Port shall do the following upon receiving a Delay Request:

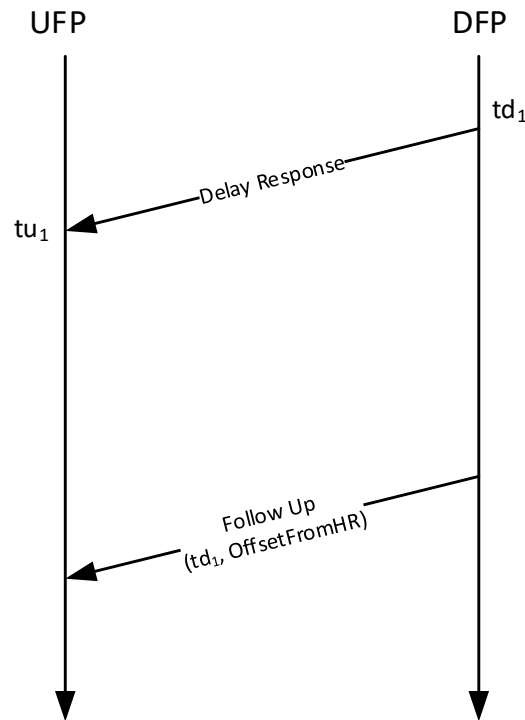
1. Take the tu_1 timestamp.
2. Send a Delay Response.
 - a. Delay Response shall be sent within RespTimeout time of receiving the Delay Request.
 - b. The Upstream Facing Port shall take the tu_2 timestamp upon Delay Response transmission.

7.3.1.3.2 Adaptive Uni-Directional Mode

When the ~~TransmitterAdapters on a Link are is~~ not in a ~~CL2, CL1 or CL0s Tx~~ state, the Downstream Facing Port shall send a Delay Response to the Upstream Facing Port at the interval specified in the *AdapterTimeSyncInterval* field in the TMU_ADP_CS_9 register in TMU Adapter

Configuration Space. A Downstream Facing Port shall transmit a Follow-Up Packet after the Delay Response was sent and within SendTimeout time of transmitting the associated Delay Response. The Downstream Facing Port shall assert an objection to CLx states in the time after sending the Delay Response and before sending the Follow-Up Packet. Figure 7-17 shows the Adaptive Uni-Directional Time Sync Handshake.

Figure 7-17. Adaptive Uni-Directional Time Sync Handshake



A Downstream Facing Port shall generate time stamp td_1 upon transmission of a Delay Response. An Upstream Facing Port shall generate time stamp tu_1 upon receipt of a Delay Response. Section 7.2 defines how time stamps are measured. Section 7.2.3 defines how timestamps are corrected for asymmetry. Transmission and reception of a Follow-Up Packet does not result in the generation of time stamps.

If an error occurs during the transmission or reception of a Time Sync Packet, the entire Time Sync Handshake shall be voided (i.e. neither time stamps nor values from the Follow-Up Packet shall be used).

Figure 7-18 shows the state machine that is recommended for a Downstream Facing Port using Adaptive Uni-Directional mode. The state machine uses the following timeout values:

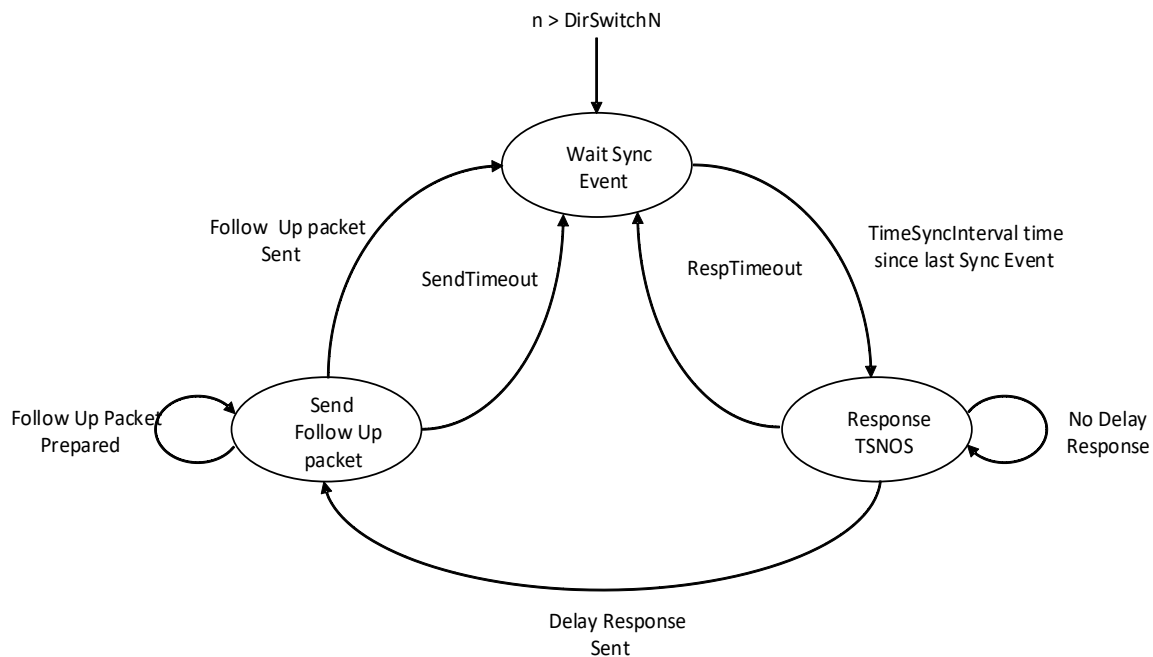
- RespTimeout is the maximum time between a Time Sync event and transmission of Delay Response. See Table 7-6 for the recommended value.

Note: A Router assumes that the transmission of Delay Responses is constant and consistent. However, any variance in the time it takes to transmit Delay Response adds to overall noise. The purpose of RespTimeout is to add robustness and make sure the state machine doesn't get stuck as a result of such noise.

- SendTimeout is the maximum time between sending a Delay Response and sending a Follow-Up Packet. See Table 7-6 for the recommended value.

Table 7-6. Adaptive Uni-Directional DFP Timeout Values

Timeout Name	Timeout Recommended Value
RespTimeout	1 μ s
SendTimeout	8 μ s

Figure 7-18. DFP State Machine for Adaptive Uni-Directional Time Sync Handshake (Recommended)

When there is a transition from “Response TSNOS” state to “Wait Sync Event” state due to the expiration of **RespTimeout** and $\text{SleepCyclesN} < 7FFFh$, the Downstream Facing Port shall increment the *SleepCyclesN* by 1. When there is a transition from “Send Follow-Up Packet” state to “Wait Sync Event” state due to the expiration of **SendTimeout** and $\text{SleepCyclesN} < 7FFFh$, the Downstream Facing Port shall increment *SleepCyclesN* by 1. *SleepCyclesN* shall be set to 0h after a Follow-Up Packet is sent. The **RespTimeout** can expire when one or more Adapters on the Link are in CL1 or CL0s (TX) state, the Port is executing the Gen 4 Recovery flow, or for any other reason. Time Sync Events continue to occur at the same *AdapterTimeSyncInterval* rate even when an Adapter is in CL1 or CL0s (TX) state.

In the Follow-Up Packet associated with the first Time Sync Handshake after exiting missing Time Sync Handshake(s), the Downstream Facing Port shall set the value of the *SleepCyclesN* field to match the number of handshakes missed by the Downstream Facing Port. If the number of missed handshakes is greater than *Replenish Threshold* the Downstream Facing Port will assert an objection to CLx states until it completes *ReplenishN* number of handshakes. See Section 4.2.1.6.3 for more information about objections.

When an Adapter is in CL1 or CL0s (TX) state, a Downstream Facing Port may “pause” Time Sync Handshakes by not sending a Delay Response to the Upstream Facing Port. The Downstream Facing Port may pause Time Sync Handshakes for maximum of *Replenish Timeout* skipped handshakes while the Adapter is in CL1 or CL0s (TX) state. The Local Time counter shall continue counting while the Adapter is in CL1 or CL0s (TX) state. If the Adapter stays in CL1 or CL0s (TX) state for more than *Replenish Timeout* skipped handshakes, the Downstream Facing Port will initiate an exit from CL1 or CL0s (TX) state. The Downstream Facing Port shall resume Time Sync Handshakes upon exiting CL1 or CL0s (TX) state keeping the same *AdapterTimeSyncInterval* and the updated Local Time counter value.

When an Adapter is in the CL2 state, a Downstream Facing Port shall stop Time Sync Handshakes. When exited CL2 state back to CL0 state, the Time Sync Handshakes shall start in Inversed Bi-Directional mode as if the TMU was enabled, including objecting to CLx states before the transition to Adaptive Uni-Directional mode. A Router shall reach the required time synchronization accuracy within $t_{\text{ConvergeTime}}$ after Time Sync Handshakes are resumed when exiting CL2.

Note: During the transition to CL0, DFP and UFP may not synchronize perfectly. Consequently, DFP handshakes initiated immediately after entering CL0 could time out if UFP is still transitioning from CL2 to CL0.

Figure 7-19 shows the state machine that is recommended for an Upstream Facing Port using Adaptive Uni-Directional Time Sync Handshakes. The state machine uses the following timeout values:

FPTimeout is the maximum time between receiving a Delay Response and receiving a Follow-Up Packet. See Table 7-5 for the recommended value.

Table 7-7. Uni-Directional UFP Timeout Values

Timeout Name	Timeout Recommended Value
FPTimeout	10 μ s

Figure 7-19. UFP State Machine for Adaptive Uni-Directional Time Sync Handshake (Recommended)

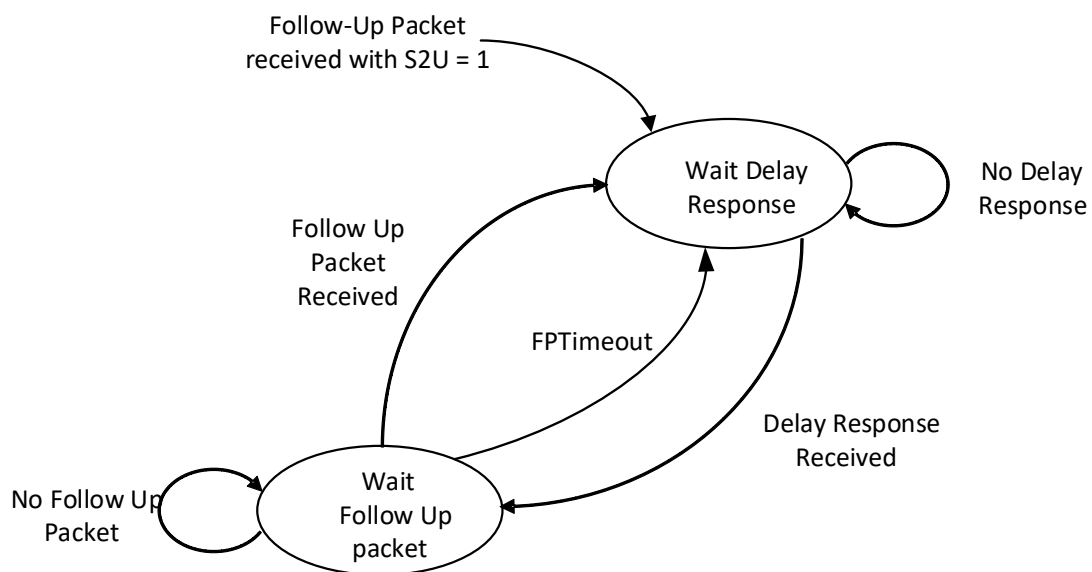
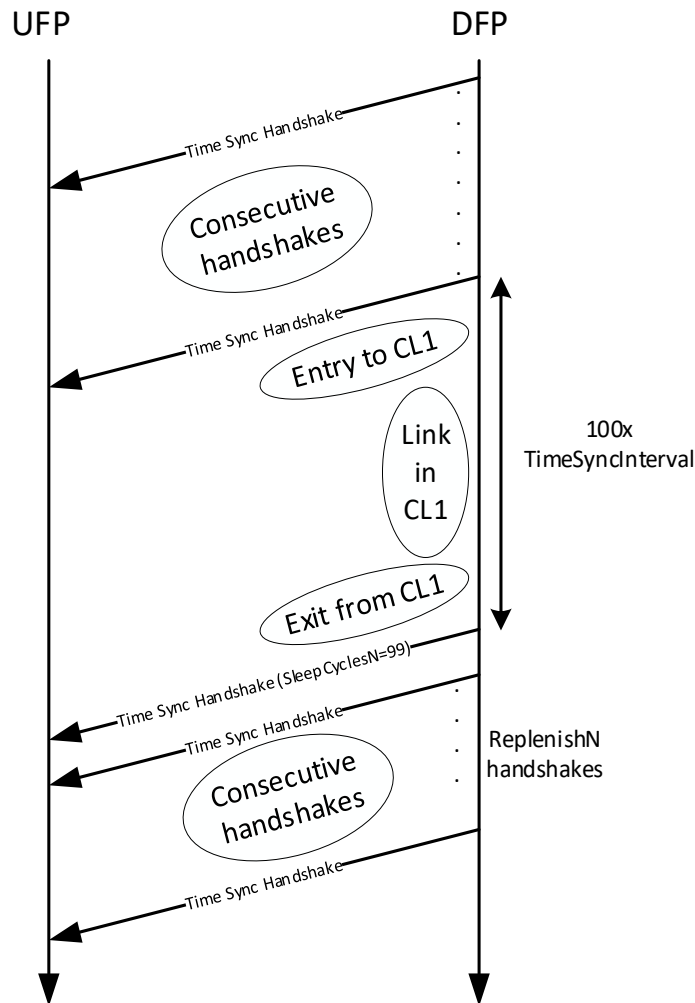


Figure 7-20 Shows an example of Time Sync Handshakes that are paused due to entry to CL1. In this example, the *Replenish Threshold* < 99. While in CL1 state (from the point the Downstream Facing Port stopped sending Delay Responses to the first Delay Response after exiting CL1) the Downstream Facing Port missed 99 Time Sync Handshakes. When exiting CL1 state, the Downstream Facing Port will assert an objection to CL1 until finishing at least *ReplenishN* number of handshakes. In the first Time Sync Handshake, the value of *SleepCyclesN* in the Follow-Up Packet will be 99.

Figure 7-20. Example of Time Synchronization Handshakes Paused by CL1

7.3.2 Inter-Domain Time Sync

Time synchronization between multiple Domains is possible when the Connection Managers of the Domains establish an Inter-Domain clock synchronization hierarchy. The Inter-Domain clock synchronization hierarchy is defined by the *IDTR* and *IDTI* bits as follows:

- A Domain is the Inter-Domain Time Source when the *IDTR* bit in the *TMU_ADAP_CS_3* register of the TMU Adapter Configuration Capability is set to 1b in the USB4 Port that is part of the Inter-Domain Link. The USB4 Port with the *IDTR* bit set to 1b is referred to as the "IDTR Port" in this section.
- A Domain follows the Inter-Domain Time Source when the *IDTI* bit in the *TMU_ADAP_CS_3* register of the TMU Adapter Configuration Capability is set to 1b in the USB4 Port that is part of the Inter-Domain Link. The USB4 Port with the *IDTI* bit set to 1b is referred to as the "IDTI Port" in this section.

A USB4 Port shall perform Time Sync Handshakes as described in Section 7.3 across the Inter-Domain Link when either the *IDTR* or *IDTI* bit is set to 1b. When the *IDTR* bit is set to 1b, a USB4 Port shall behave as a Downstream Facing Port. When the *IDTI* is set to 1b, a USB4 Port shall behave as an Upstream Facing Port.

After completing a Time Sync Handshake across an Inter-Domain Link, the IDTI Port shall calculate the following:

- The Inter-Domain time stamp (see Section 7.4.2.1).

- The Inter-Domain frequency offset (see Section 7.4.2.2).
- The Inter-Domain time offset (see Section 7.4.2.3).

If the Router with the IDTI Port is on a Host Router, it shall update the *InterDomainTimeStamp*, *FreqOffsetFromInterDomainHR* and *TimeOffsetFromInterDomainHR* fields in Router Configuration Space. If the IDTI Port is on a Device Router, it shall prepare an Inter-Domain Time Stamp Packet as described in Section 7.3.3.3 where:

- The *IDTimeStamp* field contains the calculated Inter-Domain time stamp.
- The *FreqOffsetFromInterDomainHR* field contains calculated the Inter-Domain frequency offset.
- The *TimeOffsetFromInterDomainHR* field contains the calculated Inter-Domain time offset.

Note: The Inter-Domain Time Stamp Packet is sent up the Spanning Tree via the Upstream Facing Port and then forwarded by each Router on the way until it reaches Host Router.

If the *TSInterDomainInterval* field in Router Configuration Space is 0, the IDTI Port shall send the Inter-Domain Time Stamp Packet after each Inter-Domain Time Sync Handshake. If the *TSInterDomainInterval* field in Router Configuration Space is not 0, the IDTI Port shall send the Inter-Domain Time Stamp Packet at time intervals equal to $(TSInterDomainInterval + 1) * TSPacketInterval$ number of microseconds. In a Device Router, the Inter-Domain Time Stamp Packet, whether it was generated in the TMU or received in the TMU from a DFP, shall be sent to the UFP.

When a Host Router receives an Inter-Domain Time Stamp Packet:

- If the *IDE* bit in the *TMU_RTR_CS_0* register of the Host Router's TMU Router Configuration Capability is set to 1b, the Host Router shall update its *TimeOffsetFromInterDomainHR* and *FreqOffsetFromInterDomainHR* registers using the time offset and frequency offset respectively contained in the Inter-Domain Time Stamp Packet.

Note: The updated values in the Host Router's TimeOffsetFromInterDomainHR and FreqOffsetFromInterDomainHR registers are propagated in the Domain via Follow-Up Packets using the corresponding fields of the packet: IDTimeStamp, TimeOffsetFromInterDomain and FreqOffsetFromInterDomain. This results in all the Routers in the Domain synchronizing their time to the Inter-Domain Host Router Clock.

- If the *IDE* bit in the Host Router is set to 0b, the Host Router shall drop the Inter-Domain Time Stamp Packet and shall not update its *TimeOffsetFromInterDomainHR* or *FreqOffsetFromInterDomainHR* registers.

If the IDTI Port is on a Host Router, there are no Inter-Domain Time Stamp Packets and the Inter-Domain parameters are computed directly when Inter-Domain Time Sync is enabled.



CONNECTION MANAGER NOTE

It is recommended that a Connection Manager not set the IDE bit to 1b until after computations over the Inter-Domain Link are stable.

At any instant of time, a Router can compute the Inter-Domain Host Router Time as described in Section 7.4.2.4.

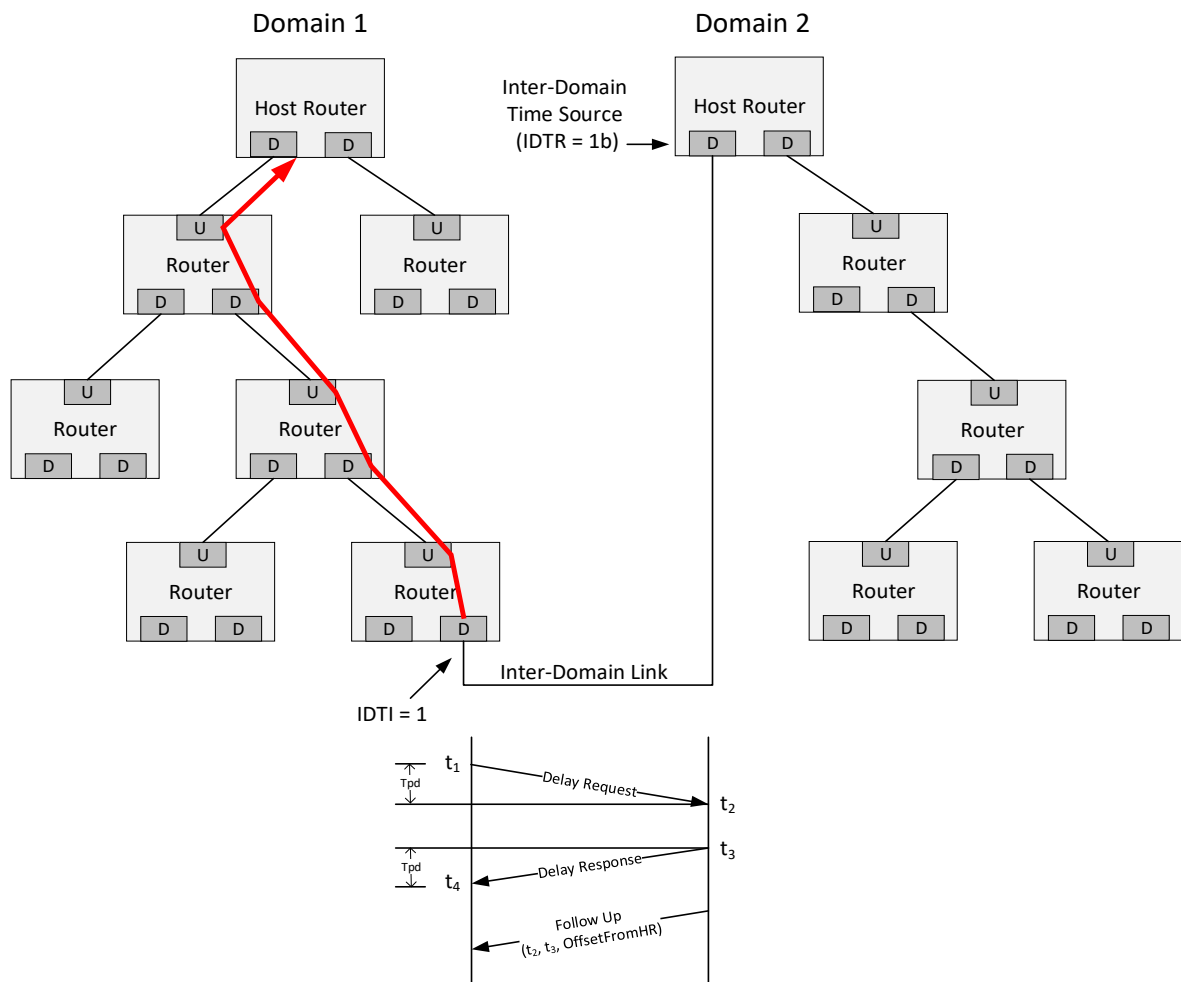
Figure 7-21 shows an example of Inter-Domain time synchronization between two Domains where the following takes place:

1. The Connection Manager detects an Inter-Domain Link between Domain 1 and Domain 2.

2. The Connection Manager sets the *IDTI* bit to 1b in Domain 1 and the *IDTR* bit to 1b in Domain 2, making Domain 2 the Inter-Domain Time Source with Domain 1 following the Domain 2 time.
3. Either Enhanced Uni-Directional, Bi-Directional, or Uni-Directional Time Sync handshakes take place across the Inter-Domain Link.
4. Domain 1 calculates the time and frequency offsets between the IDTI Port and the Inter-Domain Time Source.
5. The Router with the IDTI Port sends an Inter-Domain Time Stamp Packet to the Host Router in Domain 1.
6. Host Router in Domain 1 receives the Inter-Domain Time Stamp Packet and updates its time and frequency offsets.
7. The updated time is propagated throughout Domain 1 via Time Sync Handshakes within the Domain.

The red line in Figure 7-21 designates the route on which an Inter-Domain Time Stamp Packet is sent to the top of the tree.

Figure 7-21. Inter-Domain Time Sync Protocol (Informative)



7.3.3 Packet Formats**7.3.3.1 Time Sync Notification Ordered Set Format**

Both a Delay Request and a Delay Response shall consist of a Time Sync Notification Ordered Set (TSNOS). Section 4.3.1.3.1 defines the TSNOS for a Gen 2 and Gen 3 Link. Section 4.3.2.6.5 defines the TSNOS for Gen 4 Link.

7.3.3.2 Follow-Up Packet Format

A Follow-Up Packet shall have the format shown in Figure 7-22.

Figure 7-22. Follow-Up Packet Format

31

PDF = 1	*	Rsvd	HopID = 3	Length = 60	HEC
ResponseTS 79:64				RequestTS 79:64	
RequestTS 63:32					
RequestTS 31:0					
ResponseTS 63:32					
ResponseTS 31:0					
TimeOffsetFromHR 63:32					
TimeOffsetFromHR 31:0					
FreqOffsetFromHR 31:0					
S 2 U	SleepCyclesN[14:0]			IDTimeStamp 79:64	
IDTimeStamp 63:32					
IDTimeStamp 31:0					
TimeOffsetFromInterDomain 63:32					
TimeOffsetFromInterDomain 31:0					
FreqOffsetFromInterDomain 31:0					
CRC32					

0

* SupplID = 0

A Follow-Up Packet shall have the *PDF* field set to 1, the *HopID* field set to 3, and the *Length* field set to 60. The payload shall contain the fields in Table 7-8.

Table 7-8. Follow-Up Packet Payload

DW	Bits	Field	Description
0	15:0	<i>RequestTS</i>	<p>For Inversed Bi-Directional Time Sync Handshakes:</p> <p>This field contains the time stamp from when the corresponding Delay Request Packet was sent (i.e. time stamp td_1). The time stamp shall include the asymmetry corrections performed at the Downstream Facing Port as described in Section 7.2.3.</p> <p>For Bi-Directional Time Sync Handshakes:</p> <p>This field contains the time stamp from when the corresponding Delay Request Packet was received (i.e. time stamp t_2). The time stamp shall include the asymmetry corrections performed at the Downstream Facing Port as described in Section 7.2.3.</p> <p>For Uni-Directional and Adaptive Uni-Directional Time Sync Handshakes:</p> <p>This field shall contain the same value as the <i>ResponseTS</i> field.</p> <p>This field shall have the format shown in Figure 7-2.</p>
1	31:0		
2	31:0		
0	31:16	<i>ResponseTS</i>	<p>For Inversed Bi-Directional Time Sync Handshakes:</p> <p>This field contains the time stamp from when the corresponding Delay Response Packet was received (i.e. time stamp td_2). The time stamp shall include the asymmetry corrections performed at the Downstream Facing Port as specified in Section 7.2.3.</p> <p>For Bi-Directional, Uni-Directional and Adaptive Uni-Directional Time Sync Handshakes:</p> <p>This field contains the time stamp from when the corresponding Delay Response Packet was sent (i.e. time stamp t_3 or td_1). The time stamp shall include the asymmetry corrections performed at the Downstream Facing Port as specified in Section 7.2.3.</p> <p>This field shall have the format shown in Figure 7-2.</p>
3	31:0		
4	31:0		
5	31:0	<i>TimeOffsetFromHR</i>	<p>This field contains the time offset between the Downstream Facing Port and the Host Router.</p> <p>This field shall have the format shown in Figure 7-3.</p>
6	31:0		
7	31:0	<i>FreqOffsetFromHR</i>	<p>This field contains the frequency offset between the Downstream Facing Port and the Host Router.</p> <p>This field shall have the format shown in Figure 7-4.</p>
8	31	<i>S2U</i>	<p>This field indicates when the transition from Inversed Bi-Directional mode to Adaptive Uni-Directional mode is complete.</p> <p>This bit shall be set to 1b after Enhanced Uni-Directional Time Sync Handshakes are enabled and <i>DirSwitchN</i> – 1 number of Follow-Up packets have been sent.</p> <p>Otherwise it shall be set to 0b.</p>
	30:16	<i>SleepCyclesN</i>	<p>This field indicates the number of missed Time Sync Handshakes.</p> <p>When Adaptive Uni-Directional mode is enabled, this field shall contain the number of missed Time Sync Handshakes. It shall be set to 0h when no Time Sync Handshakes were missed.</p> <p>In Bi-Directional, Uni-Directional, and Inversed Bi-Directional modes, this field shall be set to 0h.</p>

DW	Bits	Field	Description
	15:0	<i>IDTimeStamp</i>	<p>For a Host Router:</p> <p>If the <i>IDE</i> bit is set to 1b, this field contains the most recent value of the Inter-Domain time stamp received from the IDTI Port.</p> <p>If the <i>IDE</i> bit is set to 0b, then this field shall be set to 0.</p> <p>For a Device Router:</p> <p>This field shall contain the <i>IDTimeStamp</i> value from the last Follow-Up Packet that the Router received.</p>
9	31:0		
10	31:0		
11	31:0	<i>TimeOffsetFromInterDomainHR</i>	<p>For a Host Router:</p> <p>If the <i>IDE</i> bit is set to 1b, this field contains value of the <i>TimeOffsetFromInterDomainHR</i> field in the last received Inter-Domain Time Stamp Packet.</p> <p>If the <i>IDE</i> bit is set to 0b, then this field shall be set to 0.</p> <p>For a Device Router:</p> <p>This field shall contain the <i>TimeOffsetFromInterDomainHR</i> value in the last Follow-Up Packet that the Router received.</p>
12	31:0		
13	31:0	<i>FreqOffsetFromInterDomainHR</i>	<p>For a Host Router:</p> <p>If the <i>IDE</i> bit is set to 1b, this field contains value of the <i>FreqOffsetFromInterDomainHR</i> field in the last received Inter-Domain Time Stamp Packet.</p> <p>If the <i>IDE</i> bit is set to 0b, then this field shall be set to 0.</p> <p>For a Device Router:</p> <p>This field shall contain the <i>FreqOffsetFromInterDomainHR</i> value in the last Follow-Up Packet that the Router received.</p>
14	31:0	<i>CRC32</i>	<p>CRC32 remainder value computed over the entire packet payload. The CRC32 computation shall be based on the following specification:</p> <ul style="list-style-type: none"> • Width: 32 • Poly: 1EDC 6F41h • Init: FFFF FFFFh • RefIn: True • RefOut: True • XorOut: FFFF FFFFh

7.3.3.3 Inter-Domain Time Stamp Packet

An Inter-Domain Time Stamp Packet shall have the format shown in Figure 7-23.

Figure 7-23. Inter-Domain Time Stamp Packet Format

PDF = 2	*	Rsvd	HopID = 3	Length = 28	HEC
Reserved				IDTimestamp 79:64	
IDTimestamp 63:32					
IDTimestamp 31:0					
TimeOffsetFromInterDomainHR 63:32					
TimeOffsetFromInterDomainHR 31:0					
FreqOffsetFromInterDomainHR					
CRC32					

* SuppID = 0

An Inter-Domain Time Stamp Packet shall have the *PDF* field set to 2, the *HopID* field set to 3, and the *Length* field set to 28. The payload shall contain the fields in Table 7-9.

Table 7-9. Inter-Domain Time Stamp Packet Payload

DW	Bits	Field	Description
0	31:16	<i>Reserved</i>	This field shall be set to zero.
0,1,2	79:0	<i>IDTimestamp</i>	This field contains the value of the Inter-Domain timestamp. It is computed using Equation 7-14. This field shall have the format shown in Figure 7-2.
3,4	63:0	<i>TimeOffsetFromInterDomainHR</i>	This field contains the time offset between the Host Router in the Domain with the IDTI Port and the Inter-Domain Time Source. It is computed using Equation 7-19. This field shall have the format shown in Figure 7-3.
5	31:0	<i>FreqOffsetFromInterDomainHR</i>	This field contains the frequency offset between the Host Router in the Domain with the IDTI Port and the Inter-Domain Time Source. It is computed using Equation 7-16. This field shall have the format shown in Figure 7-4.
6	31:0	<i>CRC32</i>	CRC32 remainder value computed over the entire packet payload. The CRC32 computation shall be based on the following specification: <ul style="list-style-type: none"> Width: 32 Poly: 1EDC 6F41h Init: FFFF FFFFh RefIn: True RefOut: True XorOut: FFFF FFFFh

7.4 Time Computations

A Router shall be able to compute the Host Router Time at any instant in time. A Router can do this by maintaining a continuous notion of Host Router Time or it can use some other means that are implementation specific.

Section 7.4.1 describes how to compute Host Router Time within a single Domain. Section 7.4.2 describes how to compute Host Router Time within multiple interconnected Domains.

Table 7-10 lists the variables used for the time computations in this section. Table 7-11 lists the index notations and their meanings.

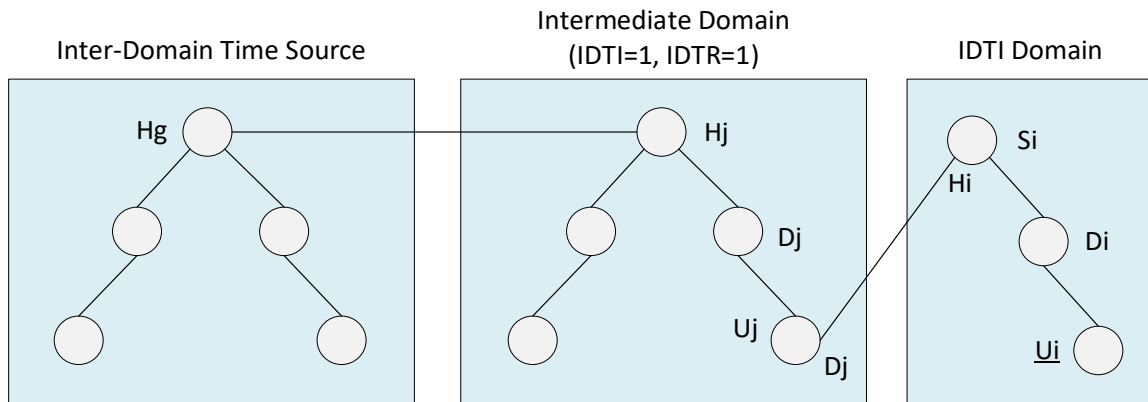
Table 7-10. Definition of Variables

Variable	Description
$f(U,D)$	Frequency ratio between the UFP (U) and DFP (D).
$f(U,H)$	Frequency ratio between the UFP and Host Router (H).
$F(U,D)$	Frequency offset between the UFP and DFP.
$F(U,H)$	Frequency offset between the UFP and Host Router.
$F(D,H)$	Frequency offset between the DFP and Host Router.
T_{pd}	Propagation delay between the UFP and DFP.
$O_{last}(D,H)$	Most recent time offset between the DFP and Host Router.
$t_{last}(D)$	Time when $O_{last}(D, H)$ was computed at the DFP.

Table 7-11. Index Notation

Index	Description
n	Current computation cycle. <i>Note: This index also advances when handshakes are missed.</i>
N	Current computation cycle of the frequency offset. This computation occurs every w number of Time Sync Handshakes. For example, if $w = 800$, then the first frequency offset computation occurs when $n = 800$, $N = 1$, and the next occurs when $n = 1600$, $N = 2$, and so on.
w	Number of Time Sync Handshakes over which the frequency offset is computed. This value is obtained from the <i>Freq Measurement Window</i> field in the <code>TMU_RTR_CS_0</code> register in the TMU Router Configuration Capability in Router Configuration Space.
U_i	A UFP in Domain i .
D_i	A DFP in Domain i .
H_i	The Host Router in Domain i .
t_h	Host Router Time.

Figure 7-24 shows an example of an Inter-Domain topology for time synchronization. The Host Router in Domain i is marked as H_i . The Downstream Facing Port and Upstream Facing Port in Domain i are marked as D_i and U_i respectively. In the following sections the subscript i refers to the ITDI Domain, the subscript j refers to the ITDR Domain and the subscript g refers to the Time Source Domain. Note that a Router can have both its Upstream Facing Port and Downstream Facing Port involved in the Time Sync Handshake and computations. In addition, a Router may also have the *ITDI* and *ITDR* bits set to 1b, which means that it performs Inter-Domain calculations both as a Time Source and a follower.

Figure 7-24. Inter-Domain Topology (Informative)**7.4.1 Intra-Domain Equations**

A Router shall use the following series of computations to calculate the current Host Router Time within a single Domain:

- An Upstream Facing Port uses Equation 7_3 to compute the frequency ratio between itself and its Link Partner.
- An Upstream Facing Port uses Equation 7_4 to compute the frequency offset. The Upstream Facing Port uses the frequency ratio obtained in Step 1 as input to the computation.
- An Upstream Facing Port uses Equation 7_5 to compute the frequency ratio between itself and the Host Router. The Upstream Facing Port uses the *FreqOffsetFromHR* value in the last Follow-Up Packet received from its Link Partner as input to the computation.
- An Upstream Facing Port uses Equation 7_6 to compute the frequency offset between itself and the Host Router. The Upstream Facing Port use the frequency ratio computed above as input to the computation.
- An Upstream Facing Port uses Equation 7_7 to compute the propagation delay of the cable between the Upstream Facing Port and its Link Partner.
- The Link Partner (i.e. the Downstream Facing Port upstream of the Upstream Facing Port) uses Equation 7_9 to compute the most updated time offset from the Host Router. The Link Partner uses the most recent result from Equation 7_12, as input to the computation.

For example, in a Spanning Tree with 3 Routers (A->B->C), Router A is the Host Router and is therefore the Domain Time Source. Because Router A is the Domain Time Source, the value of Equation 7_9 is 0 at Router A. When Router A sends a Follow-Up Packet to Router B, the *TimeOffsetFromHR* field will be 0. When Router B receives a Follow-Up Packet from Router A, it computes the time offset from the Host Router using Equation 7_12 and stores it for further usage. When Router B sends a Follow-Up Packet to Router C, the time offset from the Host Router previously computed by Router B is out-of-date. Because of this, Router B uses Equation 7_9 to compute the updated time offset from Host Router between itself and Router A, before sending a Follow-Up Packet with the updated time offset to Router C.

- An Upstream Facing Port uses Equation 7_10 (Bi-Directional Time Sync Handshake) or Equation 7_11 (Uni-Directional Time Sync Handshake) to compute the time offset from its Link Partner.
- An Upstream Facing Port uses Equation 7_12 to compute the time offset from the Host Router. The Upstream Facing Port uses the time offset from Equation 7_10 or Equation 7_11, and the value in the last received Follow-Up Packet as input to the computation.

- An Upstream Facing Port uses Equation 7-13 to compute the current time offset from the Host Router. The Upstream Facing Port uses the time offset computed in Equation 7-12 and the frequency offset computed in Equation 7-5 as input to the computation.
- When Enhanced Uni-Directional mode is enabled, the equations use $t_3 = td_1$ and $t_4 = tu_1$
- When using Equation 7-11 in Adaptive Uni-Directional mode, the *Const* value is the average T_{pd} calculated using Equation 7-8 in Inversed Bi-Directional mode.

Equation 7-37-2. Frequency Ratio between UFP and DFP

$$f(U_i, D_i)[N] = \frac{t_4[n] - t_4[n-w]}{t_3[n] - t_3[n-w]}$$

Equation 7-47-3. Frequency Offset between UFP and DFP

$$F(U_i, D_i)[N] = \{f(U_i, D_i)[N] - 1\} \cdot 2^{41}$$

Equation 7-57-4. Frequency Ratio between UFP and Host Router

$$f(U_i, H_i)[N] = f(U_i, D_i) \cdot \left\{ 1 + \frac{F(D_i, H_i)[N]}{2^{41}} \right\}$$

where $F(D_i, H_i)[N]$ is the value in the *FreqOffsetFromHR* field of the most recently received Follow-Up Packet.

Equation 7-67-5. Frequency Offset between UFP and Host Router

$$F(U_i, H_i)[N] = \{f(U_i, H_i)[N] - 1\} \cdot 2^{41}$$

Equation 7-77-6. Propagation Delay (Bi-Directional Time Sync Handshake only)

$$T_{pd}[n] = \frac{(t_4[n] - t_1[n]) - (t_3[n] - t_2[n])}{2}$$

Equation 7-87-7. Propagation Delay (Inversed Bi-Directional Time Sync Handshake only)

$$T_{pd}[n] = \frac{(td_2[n] - td_1[n]) - (tu_2[n] - tu_1[n])}{2}$$



IMPLEMENTATION NOTE

It is recommended that the value for the Link T_{pd} be an average of the values calculated in the first DirSwitchN number of handshakes.

Equation 7-97-8. Time Offset that DFP Sends in Follow-Up Packet

$$O(D_i, H_i)[n] = O_{last}(D_i, H_i) - (t_3[n] - t_{last}(D_i)[n]) \cdot \frac{F(D_i, H_i)[N]}{2^{41} + F(D_i, H_i)[N]}$$

where:

- $O_{last}(D_i, H_i)$ is the most recent computed time offset from Host Router by the Downstream Facing Port (see Equation 7-10).
- $t_{last}(D_i)[n]$ is the most recent t_4 time stamp in the Downstream Facing Port when the last Time Sync Handshake was performed at the Upstream Facing Port of the Router.
- $F(D_i, H_i)[N]$ is the most recent frequency offset from the Host Router computed by the Downstream Facing Port (see Equation 7-6).

Note: The value of $F(D_i, H_i)[N]$ is the same as $F(U_i, H_i)[N]$ in the same Router.

Equation 7-10~~7-9~~. Time Offset from DFP for Bi-Directional Time Sync Handshake

$$O(U_i, D_i)[n] = t_3[n] - t_4[n] + Tpd[n]$$

Equation 7-11~~7-10~~. Time Offset from DFP for Uni-Directional Time Sync Handshake

$$O(U_i, D_i)[n] = t_3[n] - t_4[n] + Const$$

where *Const* is implementation specific (and helps to minimize time offset caused by Uni-Directional Time Sync Handshake where propagation delay is not computed).

Equation 7-12~~7-11~~. Time Offset from Host Router

$$O(U_i, H_i)[n] = O(U_i, D_i)[n] + O(D_i, H_i)[n]$$

Equation 7-13~~7-12~~. Host Router Time at Any Given Time (t_{now})

$$t_h = t_{last}(U_i)[n] + O(U_i, H_i)[n] + (t_{now} - t_{last}(U_i)[n]) \cdot \frac{2^{41}}{2^{41} + F(U_i, H_i)[n]}$$

where $F(U_i, H_i)[N]$ is the frequency offset of the Upstream Facing Port from the Host Router.

Note: Equation 7-13 is a subset of Equation 7-20 (Inter-Domain Host Router Time).

7.4.2 Inter-Domain Equations

The purpose of an Inter-Domain Time Sync Handshake is to determine the time and frequency offsets from the Inter-Domain Host Router. Using this information, a Router in any Domain can compute the Inter-Domain Host Router Time at any moment.

A Domain that contains an IDTI Port performs the following steps to compute the Inter-Domain Host Router Time:

1. Compute time synchronization parameters the same as an Upstream Facing Port in a single Domain using Equation 7-12.

Note: Inter-Domain computations are done in parallel to the Intra-Domain computations and the two processes are independent of each other, although some parameters from the Intra-Domain computations are used for Inter-Domain time synchronization.

2. Compute the following three parameters:
 - Inter-Domain time stamp (Section 7.4.2.1).
 - Inter-Domain frequency offset (Section 7.4.2.2).
 - Inter-Domain time offset (Section 7.4.2.3).
3. Use the Parameters in Step 2 to compute the Inter-Domain Host Router Time (Section 7.4.2.4).

Note: In this section, t_1 , t_2 , t_3 and t_4 refer to the timestamps from the handshake between an IDTI Port and an IDTR Port.

7.4.2.1 Inter-Domain Time Stamp Computation

The Inter-Domain Time Stamp is a translated $t_4[n]$ time stamp from the Local Clock of a Router (U_i) to the time units of Domain i . The computations in this section are used to convert time stamps taken at a Router's Local Clock into the equivalent Host Router Time.

The following formula is used to compute an Inter-Domain time stamp.

Equation 7-14~~7-13~~. Inter-Domain Time Stamp

$$t_{last-id}[n] = t_{last}(U_i)[n] + O(U_i, H_i)[n] + (t_4[n] - t_{last}(U_i)[n]) \cdot \frac{2^{41}}{2^{41} + F(U_i, H_i)[N]}$$

where:

- i represents the current Domain.
- $t_{last}(U_i)[n]$ is the time stamp at the instant the last computation of the IDTI Port was executed, which is the t_4 time stamp in the Upstream Facing Port time sync handshake.
- $t_4[n]$ is the Time stamp from the Inter-Domain Time Sync Handshake.
- $O(U_i, H_i)[n]$ is the most updated time offset computed by this Router in its own Domain i .

7.4.2.2 Inter-Domain Frequency Offset Computation.

The frequency ratio between the Host Router in the Domain with the IDTI Port and the Inter-Domain Time Source is computed using Equation 7-15.

Equation 7-157-14. Frequency Ratio between the Host Router of the Domain with the IDTI Port and the Inter-Domain Time Source

$$f(H_i, H_g)[N] = \frac{f(U_i, D_j)[N] \cdot f(D_j, H_j)[N] \cdot f(H_j, H_g)[N]}{f(U_i, H_i)[N]}$$

where:

- $f(U_i, H_i)[N]$ is the most recent frequency ratio computed as part of the Intra-Domain flow (Equation 7-5).
- $f(U_i, D_j)[N]$ is the frequency ratio between the Local Clock of the IDTR Port and the Local Clock of the IDTI Port, computed as part of the Inter-Domain flow using Equation 7-5.
- $f(D_j, H_j)[N]$ is the frequency ratio derived from the *FreqOffsetFromHR* field in the last Follow-Up Packet sent by the IDTR Port via the Inter-Domain Link.
- $f(H_j, H_g)[N]$ is the frequency ratio derived from the *FreqOffsetFromInterDomainHR* field in the last Follow-Up Packet sent by the IDTR Port via the Inter-Domain Link.

Equation 7-167-15. Frequency Offset of Inter-Domain from Inter-Domain Host Router

$$F(H_i, H_g)[N] = \{f(H_i, H_g)[N] - 1\} \cdot 2^{41}$$

7.4.2.3 Inter-Domain Time Offset Computation

The time offset of the IDTR Port that is sent in the Follow-Up Packet at the end of an Inter-Domain Time Sync Handshake is computed using the following equation.

Equation 7-177-16. Time Offset from the IDTR Port

$$\phi_j[n] = O(D_j, H_j)[n] - (t_3[n] - t_{last}(U_j)[n]) \cdot \frac{F(D_j, H_j)[n]}{2^{41} + F(D_j, H_j)[n]}$$

where:

- $F(D_j, H_j)[N]$ is the frequency offset of the IDTR Port in its own Domain.
- $O(D_j, H_j)[n]$ is the most recent computed time offset from Host Router by the Downstream Facing Port (see Equation 7-10) of the IDTR Port in its own Domain.
- $t_3[n]$ is the time stamp of the IDTR Port during the current Inter-Domain Time Sync Handshake.
- $t_{last}(U_j)[n]$ is the last computation time stamp of the IDTR Port in its own Domain as part of the Upstream Facing Port calculations.

The time offset between the IDTI Port and the Inter-Domain Time Source is computed using Equation 7-18.

Equation 7-187-17. Time Offset between the IDTI Port and Inter-Domain Time Source

$$O(D_i, H_j)[n] = O(U_i, D_j)[n] + \emptyset_j[n]$$

where:

- $O(U_i, D_j)[n]$ is the time offset from the IDTR Port as computed by the IDTI Port at the end of an Inter-Domain Time Sync Handshake (Equation 7-10).
- $\emptyset_j[n]$ is the Inter-Domain time offset sent by the IDTR Port in the Follow-Up Packet (TimeOffsetFromHR).

The time offset between the Host Router of the Domain with the IDTI Port and the Inter-Domain Time Source is computed using Equation 7-19.

Equation 7-197-18. Time Offset between the Host Router of the Domain with the IDTI Port and the Inter-Domain Time Source

$$O(H_i, H_g)[n] = O(D_i, H_j)[n] + O(H_j, H_g)[n] - O(U_i, H_i)[n] + \left((t_4[n] - t_{last}(U_i)[n]) \cdot \frac{F(U_i, H_i)[N]}{2^{41} + F(U_i, H_i)[N]} \right) - \left((t_4[n] - t_{last-id}[n] + O(U_i, H_j)[n]) \cdot \frac{F(H_j, H_g)[N]}{2^{41} + F(H_j, H_g)[N]} \right)$$

where:

- $F(U_i, H_i)[N]$ is the frequency offset from the Host Router in the Domain of the IDTI Port.
- $F(H_j, H_g)[N]$ is the frequency offset from the Inter-Domain Time Source as sent by the IDTR Port in the Follow-Up Packet (FreqOffsetFromInterDomainHR).
- $t_{last}(U_i)[n]$ is the time stamp of last computation of the IDTI Port in its own Domain.
- $t_{last-id}[n]$ is the Inter-Domain time stamp supplied in the Follow-Up Packet (IDTimeStamp).
- $t_4[n]$ is the time stamp of the current Inter-Domain Time Sync Handshake between the IDTI Port and the IDTR Port.
- $O(U_i, H_i)[n]$ is the time offset from the Host Router in the Domain of the IDTI Port.
- $O(H_j, H_g)[n]$ is the time offset from the Inter-Domain Time Source as sent by the IDTR Port in a Follow-Up Packet (TimeOffsetFromInterDomainHR).
- $O(D_i, H_j)[n]$ is the time offset from the Inter-Domain Time Source as computed in Equation 7-18.

7.4.2.4 Inter-Domain Host Router Time Computation

A Router can compute the Inter-Domain Host Router Time (t_{idg}) using Equation 7-20.

Equation 7-207-19. Inter-Domain Host Router Time

$$t_{idg} = t_{last-id}[n] + O(H_i, H_g)[n] + \frac{t_{last}(U_i)[n] + O(U_i, H_i)[n] + \left\{ \frac{t_{now} - t_{last}(U_i)[n]}{1 + \frac{F(U_i, H_i)[N]}{2^{41}}} \right\} - t_{last-id}[n]}{1 + \frac{F(H_i, H_g)[N]}{2^{41}}}$$

where:

- t_{now} is the time at which the computation is being performed.
- $t_{\text{last-id}}[n]$ is the Inter-Domain time stamp in the *IDTimeStamp* field of the last received Follow-Up Packet.
- $O(H_i, H_g)[n]$ is that last computed Inter-Domain time offset from Inter-Domain Host Router.
- $t_{\text{last}}(U_i)[n]$ is the time stamp of the last Upstream Facing Port computation in the current Router (t_4).
- $O(U_i, H_i)[n]$ is the most updated time offset from the Host Router of the current Router's Domain.
- $F(U_i, H_i)[N]$ is the frequency offset from the Host Router computed in the current Router.
- $F(H_i, H_g)[N]$ is the frequency offset from the Inter-Domain Host Router in the *FreqOffsetFromInterDomainHR* field of the last received Follow-Up Packet.

If the IDTI Port is on a Host Router, all the components for Equation 7-20 are computed in the Host Router (i.e. Equation 7-18 and Equation 7-19 are not forwarded in the Follow-Up Packet).

7.4.3 Filtering

In order to achieve the required accuracy, it is recommended to use the following filters in the process of computing: Propagation Delay (Tpd), Time Offset and Frequency Offset computations.

Section 7.4.3.1 describes the first order IIR filter that should be applied on Propagation Delay (Tpd), and Frequency Offset computations. Section 7.4.3.2 describes the second order IIR that should be applied on Time Offset computation.

7.4.3.1 First order IIR

The first order IIR filter is described in Equation 7-22:

Equation 7-21~~7-20~~. First order IIR Low Pass Filter

$$Y[n] = \left(1 - \frac{1}{2^p}\right) \cdot Y[n-1] + \frac{1}{2^p} \cdot X[n]$$

where:

- $X[n]$ is the new input to filter.
- $Y[n-1]$ is the previous value of the filter.
- $Y[n]$ is the new value of the filter.
- p is the filter strength.

The values in the following registers in Router Configuration Space can be used for filtering frequency offset, and propagation delay:

- FreqAvgConst.
- DelayAvgConst.

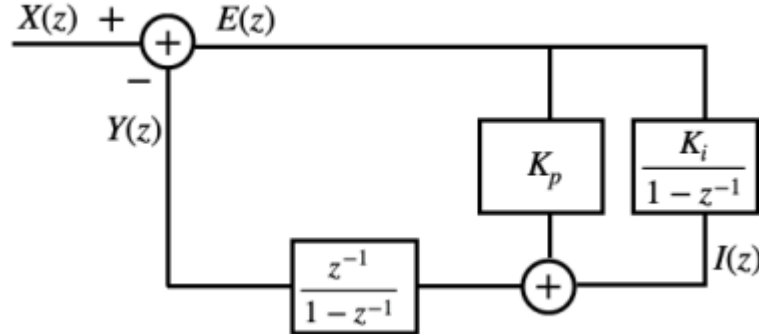
It is recommended that a USB4 Port apply IIR filters with strength (p) of at least 4.

7.4.3.2 Second order IIR filter

Time Offset filtering should utilize a filter capable of autonomously estimating noise without compromising Time Offset accuracy. The second order IIR filter described below will effectively learn the noise characteristics, eliminating noise interference after an initial convergence phase without attenuating the Time Offset.

Figure 7-25 illustrates the filter, and Equation 7-22, Equation 7-23 and Equation 7-24 describe the steps to calculate the filter output.

Figure 7-25. 2nd order IIR Filter



Equation 7-22~~7-21~~. W-1

$$E[n] = X[n] - Y[n]$$

Equation 7-23~~7-22~~. W-2

$$I[n] = I[n - 1] + E[n] \cdot K_i$$

Equation 7-24~~7-23~~. W-3

$$Y[n + 1] = Y[n] + E[n] \cdot K_p + I[n]$$

where:

- $X[n]$ is the new input to filter.
- $Y[n]$ is the new value of the filter.
- $Y[n+1]$ is the next value of the filter in the following handshake.
- $K \triangleq 2^{-p_p}$ and $K_i \triangleq 2^{-p_i}$ while p_p and p_i are the filter strengths

7.4.3.2.1 Calculations on handshake resumption

As result of handshake suspension (for example during CLx residency, or missing handshakes due to link errors), the filter is not being updated. To compensate for this period and calculate the new value of the filter, the following estimation is used by using Equation 7-25 and Equation 7-26. This estimation is applied only in the first handshake after pause.

Equation 7-25~~7-24~~. Z-1

$$I[n - 1] = I[n - \text{SleepCyclesN} - 1]$$

Equation 7-26~~7-25~~. Z-2

$$Y[n] = Y[n - \text{SleepCyclesN}] + \text{SleepCyclesN} \cdot I[n - 1]$$

where:

- SleepCycleN is the number of skipped handshakes(s).
- n-SleepCycleN-1 is the last handshake index before handshake(s) was skipped.
- $I[n\text{-SleepCycleN-1}]$ was calculated in handshake $[n\text{-SleepCycleN-1}]$.
- $Y[n\text{-SleepCycleN}]$ was calculated in handshake $[n\text{-SleepCycleN-1}]$.

Subsequently, to complete the compensation calculations (in the first handshake after pause), Equation 7-22, Equation 7-23 and Equation 7-24 should be used to compute $Y[n+1]$ and $I[n]$. In the following handshakes the filter returns to its normal operation using only equations Equation 7-22, Equation 7-23 and Equation 7-24.

7.4.3.2.2 Filter's strength

For USB4 Ports, employing IIR filters with $P_p = 5$ and $P_i = 17$ is recommended. However, in instances of missed handshakes or power-up events, adaptive behavior is advised. Table 7-12 below outlines the Filter's strength from the initial handshake until the convergence period's conclusion.

Table 7-12. Converge Phase Strengths

Handshake Index	P_p	P_i
1	Filter invalid	Filter invalid
2-3	1	6
4-7	2	7
8-15	3	8
16-31	4	9
32-63	5	10
64-127	5	11
128-255	5	12
256-511	5	13
512-1023	5	14
1024-2047	5	15
2048-3125	5	16
3126 and afterwards	5	17

7.5 Time Synchronization Accuracy Requirements

Time synchronization accuracy is measured in two ways: Paired Measurement and Standalone Measurement. Section 7.5.1 describes Paired Measurement. Section 7.5.2 describes Standalone Measurement.

When a Router is configured for HiFi Mode Time Sync Handshakes, the time synchronization accuracy is $t_{HiAccuracy}$. When a Router is configured for LowRes Mode Time Sync Handshakes, the time synchronization accuracy is $t_{LowAccuracy}$.

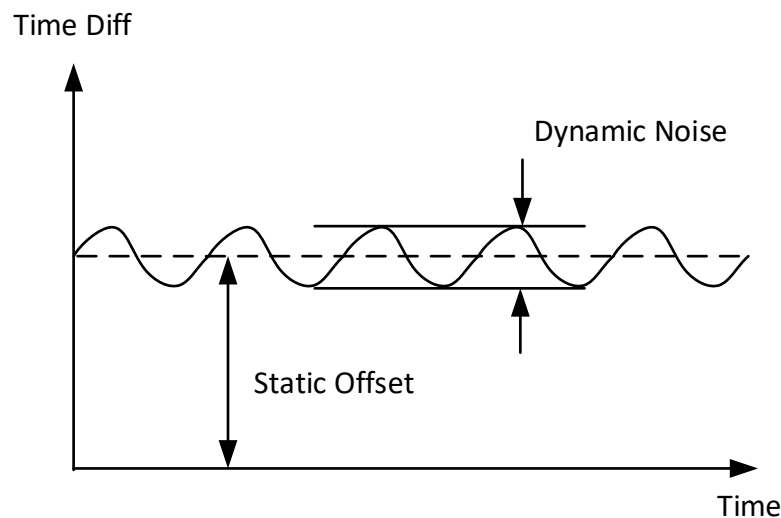
A Router shall reach the required time synchronization accuracy within $t_{\text{ConvergeTime}}$ after Time Sync Handshakes are enabled.

If Time Sync Handshakes are paused, an Upstream Facing Port shall reach the required time synchronization accuracy within $t_{\text{CLxConvergeTime}}$ after receiving a Delay Response Packet.

7.5.1 Paired Measurement

Paired Measurement is performed between two Routers (either in the same Domain or different Domains) that participate in a Time Sync Handshake. There are two parameters that affect time synchronization accuracy: Static Offset and Dynamic Noise. Figure 7-26 illustrates these parameters.

Figure 7-26. Dynamic Noise Types



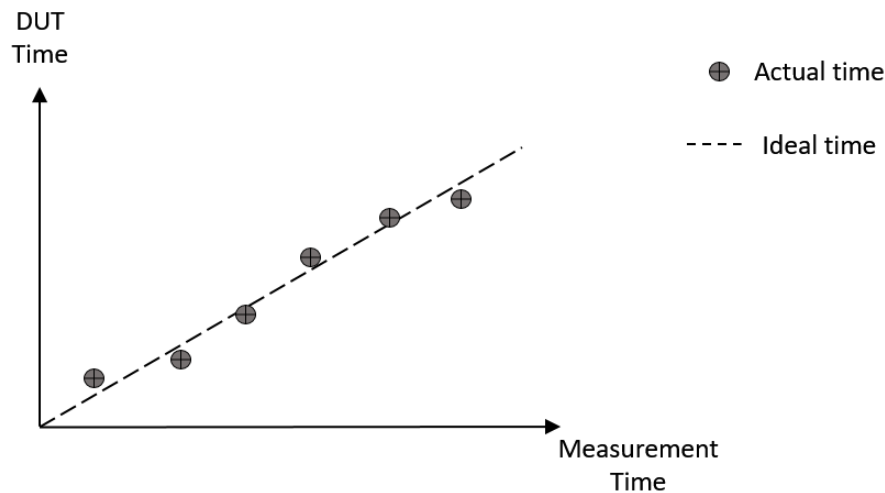
For Bi-Directional and Enhanced Uni-Directional Time Sync Handshakes, the Static Offset between two Routers connected to one another shall not add more than 8 ns per Link.

For Uni-Directional Time Sync Handshake, the Static Offset depends on the cable length and the number of Re-timers on the Link.

In HiFi Mode, the Dynamic Noise between two Routers connected to one another shall not add more than $t_{\text{HiAccuracy}}$. In LowRes Mode, the Dynamic Noise between two Routers connected to one another shall not add more than $t_{\text{LowAccuracy}}$.

7.5.2 Standalone Measurement

In this method the time noise is measured compared to an ideal line, extrapolated from the measurement points shown in Figure 7-27.

Figure 7-27. Standalone Measurement Points

In HiFi Mode, the noise between measurement points and the ideal line shall not be more than $t_{HiAccuracy}$. In LowRes Mode, the noise between measurement points and the ideal line shall not be more than $t_{LowAccuracy}$.

Note: This measurement is also used to analyze the frequency response of the noise during compliance testing.

In order to achieve the goal of $t_{HiAccuracy}$ static noise, the budget for $TxTimeToWire$ uncertainty shall not be more than 6.4 ns dynamic noise with no more than 6.4 ns static offset that changes after each power up. $RxTimeToWire$ shall not be more than 12.8 ns dynamic noise with no more than 6.4 ns static offset that changes after each power up.

Dynamic uncertainty in $TxTimeToWire$ and $RxTimeToWire$ shall be filtered out during calculations by IRR or other filtering.

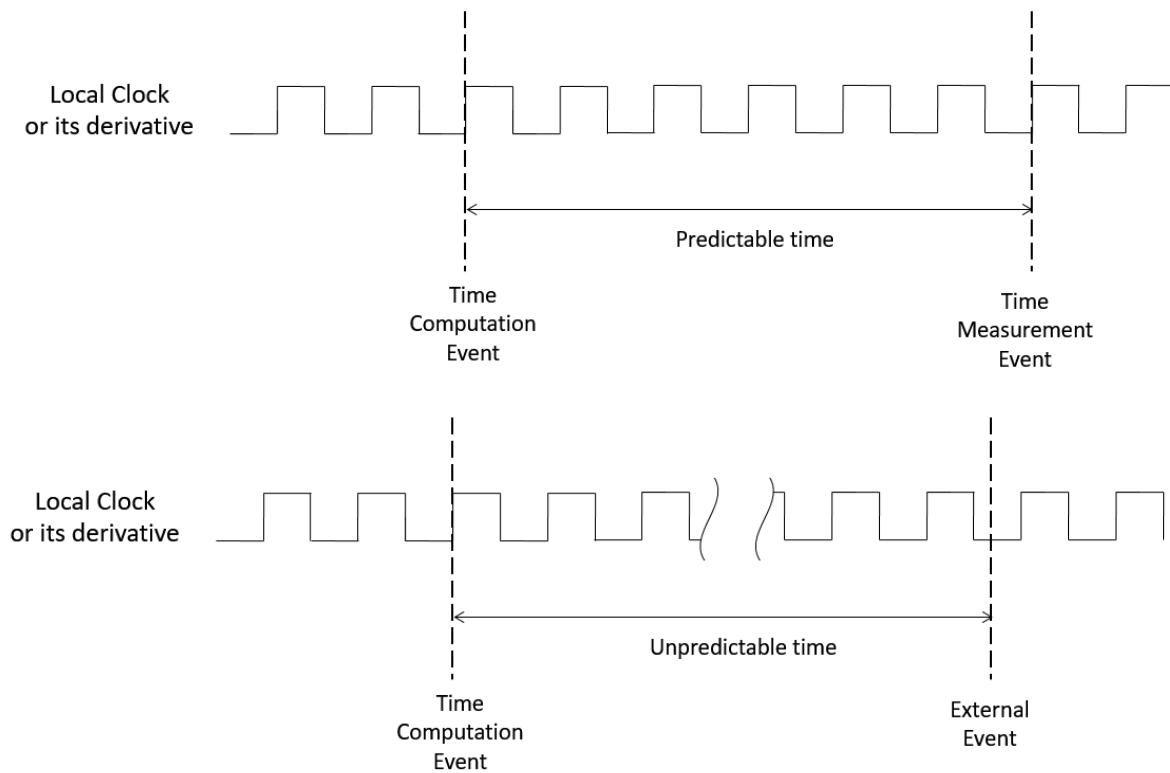
7.5.3 Measuring Method

When talking about time measurement, it is important to define the points when the time measurement is done. The computed Host Router Time is the most accurate on the computation edge of the clock.

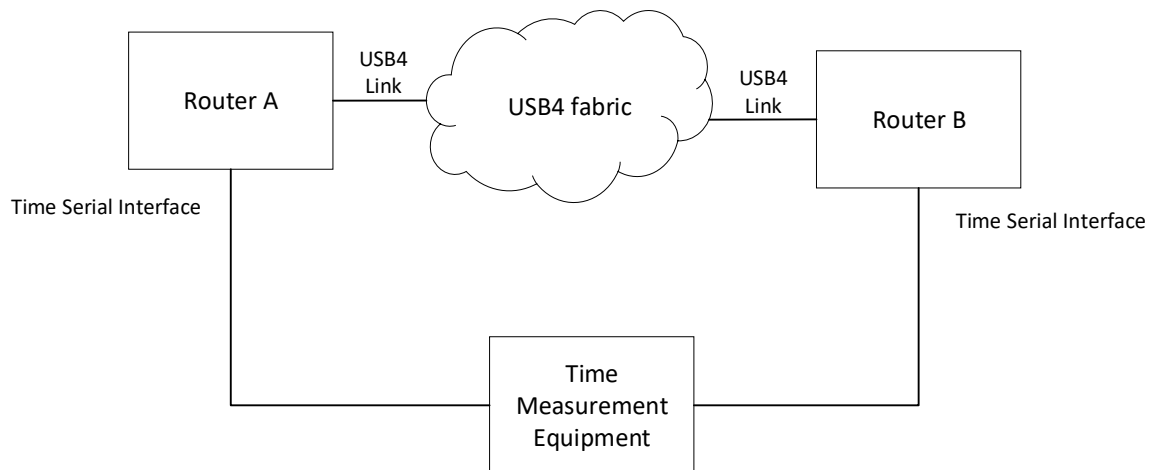
As shown in Figure 7-28, placing a Time Measurement Event at a predictable and consistent distance from a Time Computation Event helps reduce noise to the time measurement.

Sending a Serial Time Link Protocol (STLP) Packet is an example of a Time Measurement Event. An STLP Packet contains the current Host Router Time at the point of transmission of the first bit of the STLP Packet. See Appendix D for more information on the Serial Time Link Protocol.

External events that cannot be predicted and need to use the Host Router Time for timestamps (i.e. ITP, PTM), might have lower accuracy than internally generated events, depending on the method of maintaining the Host Router Time and the method of timestamp management.

Figure 7-28. Time Events

The recommended setup for performing time measurements is shown in Figure 7-29.

Figure 7-29. Measuring Method

7.5.4 Accuracy Parameters

Table 7-13 lists the accuracy parameters for time synchronization.

Table 7-13. Time Synchronization Accuracy Parameters

Parameter	Description	Min	Max	Units
tHiAccuracy	Time synchronization accuracy in HiFi Mode.	--	2	ns
tLowAccuracy	Time synchronization accuracy in LowRes Mode.	--	4	ns
tConvergeTime	Time, after Time Sync Handshakes are enabled, to reach the required time synchronization accuracy.	--	50	ms
tCLxConvergeTime	Time, after Time Sync Handshakes are resumed after pause, to reach the required time synchronization accuracy.	--	100	μs

7.6 Software Configuration

7.6.1 Intra-Domain Time Synchronization Setup

Within a single Domain, the Time Synchronization Protocol is disabled by default.

A Router that is hot-plugged to a Domain shall only initiate the Time Sync Handshake on its Upstream Facing Port when the following conditions are true:

- The physical layer has established the Link between the hot-plugged Router and the Domain.
- The *TSPacketInterval* field in the TMU_RTR_CS_3 register in Router Configuration Space is greater than 0.

7.6.2 Inter-Domain Time Synchronization Setup

When multiple Domains are connected together, the Time Synchronization Protocol is explicitly enabled by the Connection Manager.



CONNECTION MANAGER NOTE

A Connection Manager enables Inter-Domain time synchronization by:

1. *Selecting one Domain to act as the Inter-Domain Time Source. The Local Clock of the Host Router of the selected Domain becomes the Inter-Domain Time Source Clock.*
2. *Creating an Inter-Domain time synchronization hierarchy by creating a Spanning Tree of interconnected Domains.*
3. *Enabling the Time Synchronization Protocol across each Inter-Domain Link in the Spanning Tree of Interconnected Domains by setting the IDTR bit to 1b at one end of a Link and the IDTI bit to 1b at the other end of the Link.*
4. *Updating the LocalTime register of each Router in each Domain with an IDTI Port to the new Inter-Domain Time Source using the Time Posting registers.*
5. *Enabling the processing of Inter-Domain Time Stamp Packets by setting the Inter-Domain Enable bit to 1b in the TMU Router Configuration Capability of the Host Router in each Domain with a ITDI Port.*

7.6.3 Post Time Mechanism

The Post Time Mechanism is used to update the Local Time of a Router. A Router shall update its Local Time when the Post Time is greater than zero and is less than or equal to the *Nanoseconds* field in the Host Router Time ~~register~~. Time Posting shall only be activated when the Post Time High register is written. The Router updates its Local Time by writing the Post Local Time to the *Nanoseconds* field of its LocalTime register.

The Post Time is set by the Connection Manager in the *Post Time High* and *Post Time Low* fields in the TMU Router Configuration Capability in Router Configuration Space. The Post Local Time is set by the Connection Manager in the *Post Local Time Low* and *Post Local Time High* fields in the TMU Router Configuration Capability in Router Configuration Space.



CONNECTION MANAGER NOTE

The following is an example of how a Connection Manager uses the Post Time Mechanism to update a Router's Local Time:

1. *The Connection Manager reads the LocalTime register in the Host Router of the Domain (if doing Intra-Domain time synchronization) or the Inter-Domain Host Router (if doing Inter-Domain time synchronization).*
2. *The Connection Manager writes the Nanoseconds field of the Host Router Time to the Post Local Time registers in the TMU Router Configuration Capability of the Router.*
3. *The Connection Manager writes a value of 0x1 to the Post Time field in the TMU Router Configuration Capability of the Router, which causes the Router to update its Local Time to the value in the Post Local Time registers.*
4. *The Connection Manager periodically reads the Post Time field of the Router to determine when the Router is done updating its Local Time. The Router sets the Post Time field to 0x0 after it has updated its Local Time.*



CONNECTION MANAGER NOTE

When a Connection Manager receives a Hot Plug Event Packet for a Device Router, it uses the Post Time Mechanism to update the Local Time of the Device Router. It is recommended that a Connection Manager update the Local Time in the Device Router before enabling Time Synchronization in order to minimize time disruptions.

7.6.4 Time Disruption Bit

There are several system events that can cause a TMU to experience disruption in time. A Connection Manager uses the *Time Disruption* bit in Router Configuration Space to indicate to the Router when a time disruption event is occurring.



CONNECTION MANAGER NOTE

A Connection Manager shall set the Time Disruption bit in Router Configuration Space to 1b before any of the following time disruption events occur:

- *TMU mode changes (TSPacketInterval, Direction, Filters, Frequency Measurement Window).*
- *Inter-Domain time synchronization is enabled.*
- *Time Posting is applied.*

After the disruptive behavior has passed, the Connection Manager shall set the Time Disruption bit to 0b to indicate that time is reliable now.

8 Configuration Spaces

This chapter provides a detailed description of the configuration registers within the Configuration Spaces defined by the USB4® architecture. The Configuration Spaces are accessed via Read and Write Request packets as defined in Section 6.4.3.3.

8.1 Configuration Fields Access Types

Table 8-1 defines the access types that are allowed for a particular configuration register field.

Table 8-1. Configuration Register Fields Access Types

Access Type	Description
R/W	Read/Write. A field with this access type shall be capable of both read and write operations. The value read from this field shall reflect the last value written to it unless the field was reset in the interim.
R/W S	Read/Write Status. A field with this access type shall be capable of both read and write operations. The value read from this field may or may not reflect the last value written.
RO	Read Only. A write to a field with this access type shall have no effect. A read shall return a meaningful value.
R/Clr	Read Clear. A field with this access type shall be cleared to 0 after it is read. A write to a field with this attribute shall have no effect on its value.
W/Clr	Write Clear. A field with this access type shall be cleared to 0 after it is written to. A read shall return a meaningful value.
R/W SC	Read/Write Self Clearing. When set to 1b a field with this access type causes an action to be initiated. A field with this attribute shall read as 0b after the action is complete. The value returned prior to completion of the action is vendor defined.
Rsvd	Reserved. Reserved for future implementation. A write to this field shall have no effect. Unless defined otherwise, a read shall return 0.
RsvdZ	Reserved and Zero. Reserved for future implementation. A read shall return 0.
VD	Vendor Defined. A Vendor may put any value in this field.



CONNECTION MANAGER NOTE

A Connection Manager shall not change the value in a Vendor Defined field. A Connection Manager shall read a Vendor Defined field before writing to it, so it can write the correct value. A Connection Manager shall only write 0 to a field marked as RsvdZ.

The Connection Manager shall not write a register with a value that is marked as “Rsvd”.

8.2 Configuration Space Types

A Router shall implement the following Configuration Spaces:

- **Router Configuration Space:** This Configuration Space contains configuration information at a Router level. See Section 8.2.1 for details of the registers that make up the Router Configuration Space.
- **Adapter Configuration Space:** This Configuration Space contains configuration information at the Adapter level. Each Adapter other than the Control Adapter has its own Adapter Configuration Space. See Section 8.2.2 for details of the registers that make up the Adapter Configuration Space.
- **Path Configuration Space:** This Configuration Space contains configuration information at the Path level. Each Adapter other than the Control Adapter has its own Path Configuration Space with an entry in it for each of its Paths. See Section 8.2.3 for details of the registers that make up the Path Configuration Space.

A Router may also optionally implement the following Configuration Space:

- **Counters Configuration Space:** This Configuration Space contains performance statistics information at the Adapter level. See Section 8.2.4 for details of the registers that make the Counters Configuration Space. The Counters Configuration Space (CCS) Flag in the Adapter Configuration Space indicates whether an Adapter contains a Counters Configuration Space.

Note: The DW columns in the tables in this chapter refer to the Doubleword index of the register. In the case of a Capability, the index is relative to the beginning of the Capability.

All fields in a Configuration Space that are not Read Only (RO) shall contain their Default Values until a different value is written by a Connection Manager. Default Values are defined by the tables in this Chapter. A value of “Vendor Defined” in the Default Value column means that the default value is vendor defined and may vary.

8.2.1 Router Configuration Space

A Router Configuration Space shall have the format and contain the register fields depicted in Figure 8-1. The first set of Doublewords in Figure 8-1 describe the basic attributes of a Router. The rest of the Configuration Space is populated with a linked list of Capabilities.

Figure 8-1. Structure of the Router Configuration Space

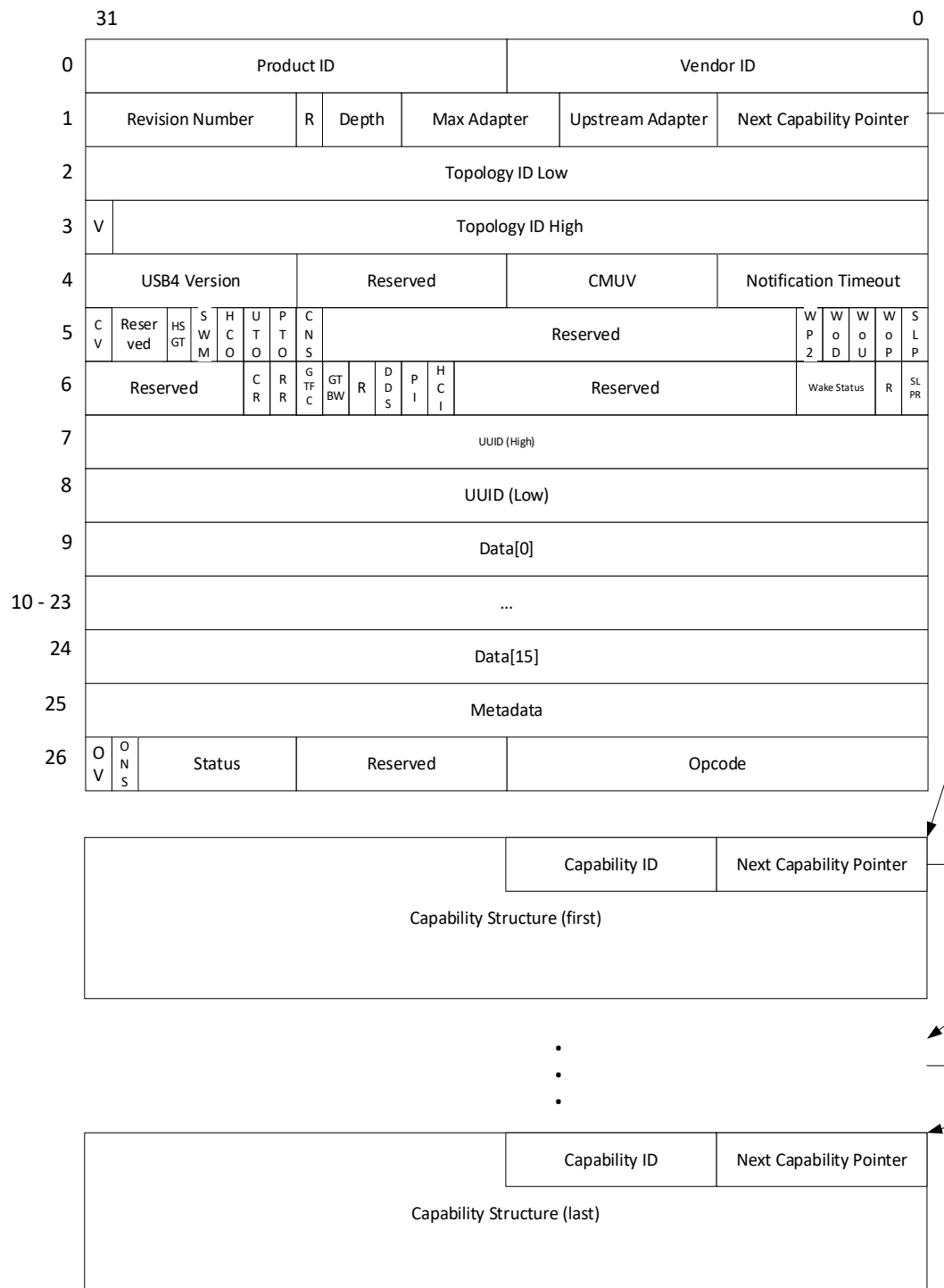


Table 8-2 lists the Capabilities supported by the Router Configuration Space. A Capability listed as “Required” shall be present in Router Configuration Space. A Capability listed as “Optional” may be present in Router Configuration Space.

Table 8-2. List of Router Configuration Capabilities

Capability	Required / Optional	Capability ID
TMU Router Configuration	Required	03h
Vendor Specific	Optional	05h

There are two types of Vendor Specific Configuration Capabilities: the Vendor Specific Capability and the Vendor Specific Extended Capability. The number of Vendor Specific Configuration Capabilities and the length of each Vendor Specific Configuration Capability is implementation specific. A Router that implements Vendor Specific Configuration Capabilities shall not depend on a Connection Manager's support for the Vendor Specific Configuration Capabilities.

Section 8.2.1.3 defines the required fields for a Vendor Specific Capability. Section 8.2.1.4 defines the required fields for a Vendor Specific Extended Capability.

Capabilities shall be linked in the following order:

- Required Capabilities.
- Optional Capabilities.
- Vendor Specific Capabilities.
- Vendor Specific Extended Capabilities.

8.2.1.1 Basic Configuration Registers

The registers in Router Configuration Space shall have the structure and fields described in Table 8-3.

Table 8-3. Router Configuration Space Basic Attributes

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ROUTER_CS_0	15:0	Vendor ID This field shall identify the manufacturer of the Router silicon. It is assigned by the USB-IF.	RO	Vendor ID
		31:16	Product ID This field shall contain a value that is assigned by the manufacturer of the Router silicon to identify the type of the Router.	RO	Vendor Defined
1	ROUTER_CS_1	7:0	Next Capability Pointer This field shall contain the Doubleword index of the first Capability in Router Configuration Space.	RO	Vendor Defined
		13:8	Upstream Adapter This field contains the Adapter Number of the Adapter that routes Control Packets to and from the Connection Manager. For a Host Router, the Host Interface Adapter is the Upstream Adapter. For a Device Router, the Upstream Adapter is the Lane 0 Adapter in the Upstream Facing Port.	RO	Vendor Defined
		19:14	Max Adapter This shall contain the Adapter Number of the highest numbered Adapter in the Router.	RO	Vendor Defined
		22:20	Depth This field contains the number of hops from the Router to the Host Router in the Spanning Tree topology. A Router shall support Depths up to and including 5.	R/W	0
		23	Reserved	Rsvd	0

		31:24	Revision Number This field shall contain the value assigned by the manufacturer to identify the revision number of the Router.	RO	Vendor Defined												
2	ROUTER_CS_2	31:0	TopologyID Low This field contains the least significant 32 bits of the TopologyID assigned to the Router by the Connection Manager. A Connection Manager shall set this field to a value that matches the value written to the <i>Depth</i> field.	R/W	0												
3	ROUTER_CS_3	23:0	TopologyID High This field contains the most significant 24 bits of the TopologyID assigned to the Router by the Connection Manager. A Connection Manager shall set this field to a value that matches the value written to the <i>Depth</i> field.	R/W	0												
		30:24	Reserved	Rsvd	0												
		31	TopologyID Valid (V) This bit indicates whether the Router is enumerated. 0b – Router is not enumerated 1b – Router is enumerated	R/W	0												
4	ROUTER_CS_4	7:0	Notification Timeout This field contains the timeout value in milliseconds used by the Router to retry Hot Plug Event Packets and packets that require a Notification Acknowledgment.	R/W	0Ah												
		15:8	Connection Manager USB4 Version (CMUV) This field identifies which version of the USB4 Specification the Connection Manager is using where: <table><tr><td>Major Version (Bits 15:12)</td><td>Minor Version (Bits 11:8)</td><td>Meaning</td></tr><tr><td>0</td><td>x</td><td>Connection Manager is a TBT3 Connection Manager</td></tr><tr><td>1</td><td>0</td><td>Connection Manager is a Ver. 1 Connection Manager or the Router is a Ver. 1 Router</td></tr><tr><td>2</td><td>0</td><td>Connection Manager is a Ver. 2 Connection Manager and the Router is a Ver. 2 Router</td></tr></table> If this field is set to a version number higher than the <i>USB4 Version</i> field, then the Router shall behave as if the Connection Manager is the same version as in the <i>USB4 Version</i> field.	Major Version (Bits 15:12)	Minor Version (Bits 11:8)	Meaning	0	x	Connection Manager is a TBT3 Connection Manager	1	0	Connection Manager is a Ver. 1 Connection Manager or the Router is a Ver. 1 Router	2	0	Connection Manager is a Ver. 2 Connection Manager and the Router is a Ver. 2 Router	R/W	0
			Major Version (Bits 15:12)	Minor Version (Bits 11:8)	Meaning												
			0	x	Connection Manager is a TBT3 Connection Manager												
1	0		Connection Manager is a Ver. 1 Connection Manager or the Router is a Ver. 1 Router														
2	0	Connection Manager is a Ver. 2 Connection Manager and the Router is a Ver. 2 Router															
23:16	Reserved	Rsvd	0														

		31:24	USB4 Version This field identifies which version of the USB4 specification is supported by the Router where: <table><tr><td></td><td>Major Version (Bits 31:29)</td><td>Minor Version (Bits 28:24)</td></tr><tr><td>Reserved for TBT3</td><td>000b</td><td>Not applicable</td></tr><tr><td>USB4 Ver. 1.0</td><td>001b</td><td>00000b</td></tr><tr><td>USB4 Ver. 2.0</td><td>010b</td><td>00000b</td></tr></table> All other values are reserved. A Router shall set this field to 40h.		Major Version (Bits 31:29)	Minor Version (Bits 28:24)	Reserved for TBT3	000b	Not applicable	USB4 Ver. 1.0	001b	00000b	USB4 Ver. 2.0	010b	00000b	RO	40h
	Major Version (Bits 31:29)	Minor Version (Bits 28:24)															
Reserved for TBT3	000b	Not applicable															
USB4 Ver. 1.0	001b	00000b															
USB4 Ver. 2.0	010b	00000b															
5	ROUTER_CS_5	0	Enter Sleep (SLP) A Connection Manager sets this bit to 1b to transition the Router into sleep state.	R/W	0												
		1	Enable Wake on PCIe (WoP) When set to 1b, a PCIe Wake indication from a PCIe device connected to a PCIe downstream port causes a Router in sleep state to convey a wake event to the host system. See Section 11.1.4.1 for the methods of handling a PCIe wake event in sleep state. When set to 0b, a PCIe Wake indication from a PCIe device connected to a PCIe downstream port is ignored. A Host Router shall hardwire this bit to 0b.	R/W	0												
		2	Enable Wake on USB3 (WoU) When set to 1b, a USB3 Wake indication from a USB device causes the Router to exit from sleep. When set to 0b, a USB3 Wake indication from a USB device does not cause the Router to exit from sleep. A Host Router shall hardwire this bit to 0b.	R/W	0												
		3	Enable Wake on DP (WoD) When set to 1b, an HPD change or reception of an HPD IRQ causes the Router to exit from sleep. When set to 0b, an HPD change or reception of an HPD IRQ does not cause the Router to exit from sleep. A Host Router shall hardwire this bit to 0b.	R/W	0												
		4	Enumerated State PCIe Wake (WP2) When set to 1b, a PCIe Wake indication from a PCIe device connected to a PCIe downstream port causes a Router in the Enumerated state to convey a wake event to the host system. See Section 11.1.4.2 for the methods of handling a PCIe wake event in Enumerated state. When set to 0b, a PCIe Wake indication from a PCIe device connected to a PCIe downstream port is ignored. A Host Router shall hardwire this bit to 0b.	R/W	0												
		22:5	Reserved	Rsvd	0												
		23	CM TBT3 Not Supported (CNS) This bit indicates whether a USB4 Connection Manager is TBT3-Compatible: 0b –TBT3-Compatible 1b – Not TBT3-Compatible A TBT3 Connection Manager does not write to this bit. A Router shall ignore this bit if the <i>Configuration Valid</i> bit is set to 0b. This field does not apply to Host Routers.	R/W	0b												

	24	PCIe Tunneling On (PTO) A Connection Manager uses this bit to let a Device Router know that it intends to enable PCIe Tunneling: 0b – PCIe tunneling will not be enabled 1b – PCIe tunneling will be enabled A Device Router shall ignore this bit if the <i>Configuration Valid</i> bit is set to 0b. This field does not apply to Host Routers.	R/W	0b
	25	USB3 Tunneling On (UTO) A Connection Manager uses this bit to let a Device Router know that it intends to enable USB3 Tunneling: 0b – USB3 tunneling will not be enabled 1b – USB3 tunneling will be enabled A Device Router shall ignore this bit if the <i>Configuration Valid</i> bit is set to 0b. This field does not apply to Host Routers.	R/W	0b
	26	Internal Host Controller On (HCO) A Connection Manager uses this bit to let a Device Router know that it intends to enable the Internal USB3 Host Controller: 0b – Internal host controller will not be enabled 1b – Internal host controller will be enabled A Device Router shall ignore this bit if the <i>Configuration Valid</i> bit is set to 0b. This field does not apply to Host Routers. A Connection Manager shall set this bit to 0b if the USB4 Upstream operates at USB4 mode and may set it to 1b if the USB4 Upstream Port operates in TBT3 Mode.	R/W	0b
	27	SW Mapping (SWM) A Connection Manager uses this bit to set the DPRX Discovery mapping mode: 0b – HW Mapping. Router autonomously maps connectors to DP OUT Adapters. 1b – SW Mapping. Router maps connectors to DP OUT Adapters as configured by the Connection Manager. A Connection Manager shall not set this bit to 1b if the <i>Partial DP Connectivity Implementation</i> bit is set to 0b. A Connection Manager shall not set this bit to 1b for a Host Router.	R/W	0b
	28	Host Supports USB3 Gen T (HSGT) A Connection Manager uses this bit to let a Device Router know if the host system supports USB3 Gen T Tunneling: 0b: The Connection Manager and/or the Host Router do not support USB3 Gen T Tunneling. 1b: Both the Connection Manager and the Host Router support USB3 Gen T Tunneling. A Device Router shall ignore this bit if the <i>Configuration Valid</i> bit is set to 0b. This field does not apply to Host Routers.	R/W	0b
	30:29	Reserved	Rsvd	0

		31	Configuration Valid (CV) A Connection Manager uses this bit to let a Device Router know whether the <i>PTO</i> , <i>UTO</i> , <i>HSGT</i> , and <i>HCO</i> fields are valid: 0b – <i>PTO</i> , <i>UTO</i> , <i>HSGT</i> , and <i>HCO</i> fields are not valid 1b – <i>PTO</i> , <i>UTO</i> , <i>HSGT</i> , and <i>HCO</i> fields are valid This field does not apply to Host Routers.	R/W	0
6	ROUTER_CS_6	0	Sleep Ready (SLPR) A Router sets this bit to 1b after the <i>Enter Sleep</i> bit is set to 1b and the Router is Ready for a sleep event. A Router sets this bit to 0b after entering sleep state.	RO	0
		1	Reserved Deprecated field (TBT3 Not Supported)	Rsvd	Vendor Defined
		2	Wake on PCIe Status A Router shall set this bit to 1b when a PCIe Wake indication from a PCIe device connected to a PCIe downstream port causes the Router to exit from sleep. A Router shall set this bit to 0b upon entry to sleep.	RO	0b
		3	Wake on USB3 Status A Router shall set this bit to 1b when a USB3 Wake indication causes the Router to exit from sleep. A Router shall set this bit to 0b upon entry to sleep.	RO	0b
		4	Wake on DP Status A Router shall set this bit to 1b when a DP Wake indication causes the Router to exit from sleep. A Router shall set this bit to 0b upon entry to sleep.	RO	0b
		17:5	Reserved	Rsvd	0
		18	Internal Host Controller Implemented (HCI) A Router shall set this bit to 0b if it does not implement an Internal USB3 Host Controller. A Router shall set this bit to 1b if it implements an Internal USB3 Host Controller. This field does not apply to Host Routers.	RO	Vendor Defined
		19	Partial DP Connectivity Implementation (PI) A Device Router shall set this bit to 1b if it supports Partial Implementation for DPRX Discovery. Otherwise it shall set this bit to 0b (Full Implementation). This field does not apply to Host Routers.	RO	Vendor Defined
		20	DPTX Discovery Support (DDS) A Router shall set this bit to 1b if it supports DPTX Discovery. Otherwise it shall set this bit to 0b.	RO	Vendor Defined
		21	Reserved	Rsvd	0
		22	Gen T Bundle Weight Mode (GTBW) A Router shall set this bit to 1b if it operates in Gen T Bundle Weight mode. Otherwise, it shall set this bit to 0b. This field only applies to Host Routers that implement USB3 Gen T Tunneling. All other Routers shall set this field to 0b.	RO	Vendor Defined
		23	Gen T Full Connectivity Support (GTFC) A Host Router shall set this bit to 1b if all its USB3 Gen T Adapters supports full connectivity as defined in Section 5.2.5. Otherwise, it shall be set to 0b.	RO	Vendor Defined

		24	Router Ready (RR) A Router sets this bit to 1b after configuring any hardware based on the value of the <i>Connection Manager USB4 Version</i> field. See Section 6.7 and Section 13.4.3 for more information.	RO	0
		25	Configuration Ready (CR) A Device Router shall set this bit to 1b when it is ready for the Protocol Tunneling enabled by the Connection Manager. A Host Router shall not set this bit to 1b.	RO	0
		31:26	Reserved	Rsvd	0
7	ROUTER_CS_7	31:0	UUID (High) This field contains bits 63:32 of the UUID value described in Section 8.2.1.1.1.	RO	Vendor Defined
8	ROUTER_CS_8	31:0	UUID (Low) This field contains bits 31:0 of the UUID value described in Section 8.2.1.1.1.	RO	Vendor Defined
9	ROUTER_CS_9	31:0	Data[0] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
10	ROUTER_CS_10	31:0	Data[1] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
11	ROUTER_CS_11	31:0	Data[2] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
12	ROUTER_CS_12	31:0	Data[3] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
13	ROUTER_CS_13	31:0	Data[4] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
14	ROUTER_CS_14	31:0	Data[5] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
15	ROUTER_CS_15	31:0	Data[6] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
16	ROUTER_CS_16	31:0	Data[7] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
17	ROUTER_CS_17	31:0	Data[8] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
18	ROUTER_CS_18	31:0	Data[9] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
19	ROUTER_CS_19	31:0	Data[10] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
20	ROUTER_CS_20	31:0	Data[11] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0

21	ROUTER_CS_21	31:0	Data[12] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
22	ROUTER_CS_22	31:0	Data[13] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
23	ROUTER_CS_23	31:0	Data[14] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
24	ROUTER_CS_24	31:0	Data[15] This field contains a DW written or read by the Connection Manager as part of a Router Operation.	R/W	0
25	ROUTER_CS_25	31:0	Metadata A Connection Manager uses this field to pass Router Operation metadata to the Router. The contents of this field vary with the Router Operation type and are defined in the Section 8.3.1.	R/W	0
26	ROUTER_CS_26	15:0	Opcode A Connection Manager uses this field to indicate the Router Operation to be executed. See Table 8-26 for the list of supported Router Operations.	R/W	0
		23:16	Reserved	Rsvd	0
		29:24	Status A Router uses this field to indicate the status of a Router Operation after completion. The values for this field vary with Router Operation type and are defined in the Section 8.3.1.	R/W	0
		30	Operation Not Supported (ONS) A Router uses this field to indicate whether the initiated Router Operation is supported: 0 – Supported 1 – Not Supported	R/W	0
		31	Operation Valid (OV) This field is set to 1b by the Connection Manager to indicate that a Router Operation is posted for processing. A Router shall process the Router Operation in the <i>Opcode</i> field when the value in this field changes from 0b to 1b. A Router shall set this field to 0b after it finishes processing the Router Operation.	R/W	0b

**CONNECTION MANAGER NOTE**

When writing to Router Configuration Space, a Connection Manager shall abide by the following rules:

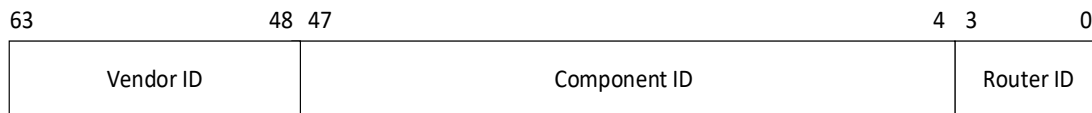
- *The Connection Manager shall read the Upstream Adapter field before writing to DW1 of Router Configuration Space (ROUTER_CS_1). When the Connection Manager writes to the Upstream Adapter field, it shall write the same value that was read so that the value in the Upstream Adapter field does not change.*
- *The Connection Manager shall use a single Write Request to enumerate a Router. The Write Request sets the Depth field, the TopologyID field, the Connection Manager USB4 Version field, and the TopologyID Valid bit (the latter to 1b).*
- *The Connection Manager shall write 0 in the Depth field of a Host Router.*
- *The Connection Manager shall not set the Notification Timeout field to 0.*
- *The Connection Manager shall write to the USB4 Version field the same value that was read.*
- *Unless specified otherwise, a Connection Manager shall not change the value in any of the fields in DW1 to DW3 after the TopologyID Valid bit is set to 1b.*
- *A Connection Manager shall not change the value in the Connection Manager USB4 Version field after setting the TopologyID Valid bit to 1b.*
- *The Connection Manager shall not write to DW26 of Router Configuration Space (ROUTER_CS_26) when the Operation Valid bit is 1b.*
- *For a Host Router, a Connection Manager shall not change the value in the following fields:*
 - *PCIe Tunneling On.*
 - *USB3 Tunneling On.*
 - *Internal Host Controller On.*
 - *Host Supports USB3 Gen T.*
 - *Configuration Valid.*
- *A Connection Manager shall set the Disable Hot Plug Events bit to the desired value:*
 - *In a Downstream Facing Port, before the Lock bit for the Port is set to 0b.*
 - *In a DP IN Adapter or a DP OUT Adapter before the AUX Enable bit and the Video Enable bit are set to 1b.*
- *For a Device Router:*
 - *The Connection Manager shall set the Configuration Valid field to 1b after setting the CNS, PTO, UTO, HSGT, and HCO fields to the desired values. A Ver. 2 Connection Manager shall not change these values once the Configuration Valid field is set to 1b.*
 - *The Connection Manager shall not set the UTO and HCO fields to 1b at the same time. At least one of the fields shall be set to 0b.*
 - *The Connection Manager shall set the Configuration Valid field to 1b before setting up any Paths through the Router.*
 - *A Connection Manager shall not set up USB3 and/or PCIe Tunneling until the Configuration Ready bit is set to 1b.*

8.2.1.1.1 UUID

Each Router contains a Universally Unique ID (UUID) assigned by the Router vendor. The UUID shall have the format shown in Figure 8-2 where:

- Vendor ID is a 16-bit ID assigned by the USB-IF, which identifies the silicon vendor. It shall contain the same value as the *Vendor ID* field in Router Configuration Space.
- Component ID is a 44-bit ID that is unique to a single piece of silicon that contains one or more Routers. Routers that reside in the same silicon shall have the same Component ID. Routers with the same Vendor ID that reside in separate silicon shall have different Component IDs.
- Router ID is a 4-bit ID that indicates the Router instance within the product.
 - A product containing multiple Router instances shall increment the Router ID for each Router instance, starting at 0. A product containing a single Router instance shall set this field to 0.

Figure 8-2. UUID Format



8.2.1.2 TMU Router Configuration Capability

A TMU Router Configuration Capability shall have the structure depicted in Figure 8-3 and the fields defined in Table 8-4.

A Router that does not support the Time Synchronization Protocol may implement all the fields in this section as Read Only (RO) type. If a Router does not support the Time Synchronization Protocol and it implements the *Post Time Low* and *Post Time High* registers as R/W, it shall clear these registers after they are written.

Any field that spans across multiple Doublewords (e.g. *LocalTime Low*, *LocalTime Middle*, and *LocalTime High*) shall use the Register Locking Mechanism defined in Section 8.2.1.2.1 and the Register Group Locking Mechanism defined in Section 8.2.1.2.2.

Figure 8-3. Structure of the TMU Router Configuration Capability

31						0					
I	U	T	R	T		Freq Measurement Window			Capability ID		Next Capability Pointer
D	C	S	S	D		LocalTime Low 31:0					0
E	A	N	V			LocalTime High 63:32					1
						TSPacketInterval			LocalTime 79:64		2
						TimeOffsetFromHR 31:0					3
						TimeOffsetFromHR 63:32					4
						TimeOffsetFromDFP 31:0					5
						TimeOffsetFromDFP 63:32					6
						FreqOffsetFromHR					7
						FreqOffsetFromDFP					8
						Propagation Delay 31:0					9
						Propagation Delay 63:32					10
						Computation Timestamp 31:0					11
						Computation Timestamp 63:32					12
						Reserved			Computation Timestamp 79:64		13
						TSInterDomainInterval			ErrorAvgConst		14
						OffsetAvgConst			DelayAvgConst		15
						InterDomain Computation Timestamp 31:0			FreqAvgConst		16
						InterDomain Computation Timestamp 63:32					17
I	D	N	S			Reserved			InterDomain Computation Timestamp 79:64		18
						TimeOffsetFromInterDomainHR 31:0					19
						TimeOffsetFromInterDomainHR 63:32					20
						FreqOffsetFromInterDomainHR					21
						Post Local Time 31:0					22
						Post Local Time 63:32					23
						Post Time 31:0					24
						Post Time 63:32					25

Table 8-4. TMU Router Configuration Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	TMU_RTR_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in Router Configuration Space. A Router shall set this field to 00h if the TMU Router Configuration Capability is the final Capability in the linked list of Capabilities in Router Configuration Space.	RO	Vendor Defined
		15:8	Capability ID A Router shall set this field to 03h indicating this is the start of a TMU Router Configuration Capability.	RO	03h
		26:16	Freq Measurement Window This field contains the number of Time Sync Handshakes that occur before the frequency ratio and frequency offset are computed.	R/W	800
		27	Time Disruption (TD) The Connection Manager sets this bit to 1b before any of the following time disruptions: <ul style="list-style-type: none"> • TMU mode changes (TSPacketInterval, Direction, Filters, Frequency Measurement Window) • Inter-Domain time sync is enabled • Time Posting is applied After the time disruption has passed, the Connection Manager sets this bit to 0b.	R/W	0
		28	Reserved	Rsvd	0
		29	Time Synchronization Protocol Not Supported (TSNS) This field shall indicate whether the Time Synchronization Protocol is supported. 0b – Time Synchronization Protocol is supported 1b – Time Synchronization Protocol is not supported	RO	Vendor Defined
		30	Uni-Directional Capability (UCAP) This field shall be 0b if Uni-Directional Time Sync Handshakes are not supported. This field shall be 1b if Uni-Directional Time Sync Handshakes are supported.	RO	Vendor Defined
1	TMU_RTR_CS_1	31:0	LocalTime Low This field contains the least significant 32 bits of the 80-bit LocalTime counter.	RO	0
			LocalTime Middle This field contains the middle 32 bits of the 80-bit LocalTime counter.	RO	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
3	TMU_RTR_CS_3	15:0	LocalTime High This field contains the most significant 16 bits of the 80-bit LocalTime counter.	RO	0
		31:16	TSPacketInterval This field contains the time interval between successive transmissions of the Delay Request TSNOS on a Link. The time interval is specified in units of 1 μ s with 100ppm accuracy. Three values are allowed for this register: 0: Shall disable Time Sync Handshake initiation by the Router 16: "HiFi" Mode (16 μ s) 1000 "LowRes" Mode (1 ms) Other values shall not be used. Unless specified otherwise, this field shall be ignored when Enhanced Uni-Directional Time Sync Handshakes are used. <i>Note: The Default value of this field is 0, which means that Time Sync Handshake initiation is disabled after wake up.</i>	R/W	0
4	TMU_RTR_CS_4	31:0	TimeOffsetFromHR Low This field contains the least significant 32 bits of the computed time offset between the Local Clock and the Host Router's Local Clock. A Router shall calculate the time offset as described in Equation 7_12.	RO	0
5	TMU_RTR_CS_5	31:0	TimeOffsetFromHR High This field contains the most significant 32 bits of the computed time offset between the Local Clock and the Host Router's Local Clock. A Router shall calculate the time offset as described in Equation 7_12.	RO	0
6	TMU_RTR_CS_6	31:0	TimeOffsetFromDFP Low This field contains the least significant 32 bits of the computed time offset between the Downstream Facing Port and Upstream Facing Port clocks. A Router shall calculate the time offset as described in Equation 7_10 for Bi-Directional Time Sync Handshakes or Equation 7_11 for Uni-Directional Time Sync Handshakes.	RO	0
7	TMU_RTR_CS_7	31:0	TimeOffsetFromDFP High This field contains the most significant 32 bits of the computed time offset between the Downstream Facing Port and Upstream Facing Port clocks. A Router shall calculate the time offset as described in Equation 7_10 for Bi-Directional Time Sync Handshakes or Equation 7_11 for Uni-Directional Time Sync Handshakes.	RO	0
8	TMU_RTR_CS_8	31:0	FreqOffsetFromHR This field contains the computed frequency offset between the Local Clock and the Host Router's Local Clock, represented using 2's complement format. A Router shall calculate the frequency offset as described in Equation 7_6.	RO	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
9	TMU_RTR_CS_9	31:0	FreqOffsetFromDFP This field contains the computed frequency offset between the Downstream Facing Port and the Upstream Facing Port clocks, represented using 2's complement format. A Router shall calculate the frequency offset as described in Equation 7-4.	RO	0
10	TMU_RTR_CS_10	31:0	Propagation Delay Low This field contains the least significant 32 bits of the computed time delay between the Router and its Upstream Link Partner. This field shall have the same format as the TimeOffsetFromHR register. A Router shall calculate the time delay as described in Equation 7-7.	RO	0
11	TMU_RTR_CS_11	31:0	Propagation Delay High This field contains the most significant 32 bits of the computed time delay between the Router and its Upstream Link Partner. This field shall have the same format as the TimeOffsetFromHR register. A Router shall calculate the time delay as described in Equation 7-7.	RO	0
12	TMU_RTR_CS_12	31:0	Computation Time Stamp Low This field shall contain the least significant 32 bits of the most recent value of the t_4 time stamp ($t_4[n]$).	RO	0
13	TMU_RTR_CS_13	31:0	Computation Time Stamp Middle This field shall contain the middle 32 bits of the most recent value of the t_4 time stamp ($t_4[n]$).	RO	0
14	TMU_RTR_CS_14	15:0	Computation Time Stamp High This field shall contain the most significant 16 bits of the most recent value of the t_4 time stamp ($t_4[n]$).	RO	0
		31:16	Reserved	Rsvd	0
15	TMU_RTR_CS_15	5:0	FreqAvgConst This field contains the IIR filter co-efficient that shall be used to average the frequency ratio. The IIR filter co-efficient is given by $(1/2^{\text{FreqAvgConst}})$.	R/W	8
		11:6	DelayAvgConst This field contains the IIR filter co-efficient that shall be used to average the propagation delay. The IIR filter co-efficient is given by $(1/2^{\text{DelayAvgConst}})$.	R/W	8
		17:12	OffsetAvgConst This field contains the IIR filter co-efficient that shall be used to average the time offset. The IIR filter co-efficient is given by $(1/2^{\text{OffsetAvgConst}})$.	R/W	8
		23:18	ErrorAvgConst This field contains the IIR filter co-efficient that shall be used to average the time offset averaging error. The IIR filter co-efficient is given by $(1/2^{\text{ErrorAvgConst}})$.	R/W	8
		31:24	TSInterDomainInterval This field controls the time interval between transmitting Inter-Domain Time Stamp Packets. The time interval is given in microseconds and is equal to $(\text{TSInterDomainInterval} + 1) * \text{TSPacketInterval}$. <i>Note: TSPacketInterval is used regardless of the TMU mode.</i>	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
16	TMU_RTR_CS_16	31:0	Inter-Domain Time Stamp Low For a Host Router: This field shall contain the least significant 32 bits of the value of the Inter-Domain time stamp received in the last Inter-Domain Time Stamp Packet. For Device Router: This field shall contain the least significant 32 bits of the IDTimeStamp value contained in the last received Follow-Up Packet.	RO	0
17	TMU_RTR_CS_17	31:0	Inter-Domain Time Stamp Middle For a Host Router: This field shall contain the middle 32 bits of the value of the Inter-Domain time stamp received in the last Inter-Domain Time Stamp Packet. For Device Router: This field shall contain the middle 32 bits of the IDTimeStamp value contained in the last received Follow-Up Packet.	RO	0
18	TMU_RTR_CS_18	15:0	Inter-Domain Time Stamp High For a Host Router: This field shall contain the most significant 32 bits of the value of the Inter-Domain time stamp received in the last Inter-Domain Time Stamp Packet. For Device Router: This field shall contain the most significant 32 bits of the IDTimeStamp value contained in the last received Follow-Up Packet.	RO	0
		23:16	DeltaAvgConst This field contains the IIR filter co-efficient that shall be used to average the time offset delta. The IIR filter co-efficient is given by $(1/2^{\Delta\text{DeltaAvgConst}})$.	R/W	0
		30:24	Reserved	Rsvd	0
		31	Inter-Domain Not Supported (IDNS) This field shall indicate whether a Router supports Inter-Domain Time Synchronization: 0 – Supported 1 – Not Supported A Host Router may set this field to either 1 or 0. A Device Router shall set this field to 0. <i>Note: the value of this bit is relevant only when TSNS is set to 0.</i>	RO	Host Router: Vendor Defined Device Router: 0
19	TMU_RTR_CS_19	31:0	TimeOffsetFromInterDomainHR Low For an Inter-Domain Time Initiator: This field shall contain the least significant 32 bits of the computed time offset between the local Host Router Clock and the Inter-Domain Time Source. This field shall have the same format as shown in Figure 7-3. The time offset shall be computed as described in Section 7.4.2.3. For all other Routers: This field shall contain the most recent value of the TimeOffsetFromInterDomainHR field contained in the last received Follow-Up Packet.	RO	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
20	TMU_RTR_CS_20	31:0	TimeOffsetFromInterDomainHR High For an Inter-Domain Time Initiator: This field contains the most significant 32 bits of the computed time offset between the local Host Router Clock and the Inter-Domain Time Source. The format of this register is shown in Figure 7-3. The time offset shall be computed as described in Section 7.4.2.3. For all other Routers: This field contains the most recent value of the <i>TimeOffsetFromInterDomainHR</i> field contained in the last received Follow-Up Packet.	RO	0
21	TMU_RTR_CS_21	31:0	FreqOffsetFromInterDomainHR For an Inter-Domain Time Initiator: This field shall contain the computed frequency offset between the local Host Router Clock and the Inter-Domain Time Source, represented using 2's complement format. The frequency offset shall be computed as described in Section 7.4.2.2. For all other Routers: This field shall contain the most recent value of the <i>FrequencyOffsetFromInterDomainHR</i> field contained in the last received Follow-Up Packet.	RO	0
22	TMU_RTR_CS_22	31:0	Post Local Time Low This field contains the least significant 32 bits of the Post Local Time. The Post Local Time is used to update a Router's Local Time as part of the Post Time Mechanism. See Section 7.6.3.	R/W	0
23	TMU_RTR_CS_23	31:0	Post Local Time High This field contains the most significant 32 bits of the Post Local Time. The Post Local Time is used to update a Router's Local Time as part of the Post Time Mechanism. See Section 7.6.3.	R/W	0
24	TMU_RTR_CS_24	31:0	Post Time Low This field contains the least significant 32 bits of the Post Time. The Post Time is when a Router updates its Local Time as part of the Post Time Mechanism. See Section 7.6.3. A Router shall set this field to 0 after updating its Local Time.	R/W	0
25	TMU_RTR_CS_25	31:0	Post Time High This field contains the most significant 32 bits of the Post Time. The Post Time is when a Router updates its Local Time as part of the Post Time Mechanism. See Section 7.6.3. A Router shall set this field to 0 after updating its Local Time. The Post Time Mechanism is only activated if this register is written.	R/W	0



CONNECTION MANAGER NOTE

A Connection Manager uses the following values to configure the *TSPacketInterval* field:

- *TMU_OFF* = 0.
- *HiFi* = 16.
- *LowRes* = 1000.

8.2.1.2.1 Register Locking Mechanism

Some of the fields in a TMU Router Configuration Capability span more than 1 DW. In order to keep consistent values in these fields, a Router shall update the value in the entire field (i.e. Low, Middle, and High DWs) when the Connection Manager reads the Low DW of the field. A Router shall not change the value in the Middle and High DWs until the next time the Low DW is read. For example, when a Connection Manager reads the LocalTime {Low, Medium, High} registers, it reads the LocalTime Low register first to lock in the LocalTime value. It then reads the LocalTime Medium register and the LocalTime High register, which each return the value that was locked when the LocalTime Low register was first read.

The Register Locking Mechanism shall be implemented for following registers:

- LocalTime {Low, Middle, High}.
- TimeOffsetFromHR {Low, Middle, High}.
- Inter-Domain Time Stamp {Low, Middle, High}.

**CONNECTION MANAGER NOTE**

In order to guarantee a consistent value across all registers, a Connection Manager shall read the Low DW of the following fields before reading the Medium DW and High DW:

- *LocalTime {Low, Medium, High}.*
- *TimeOffsetFromHR {Low, Medium, High}.*
- *Inter-Domain Time Stamp {Low, Medium, High}.*

8.2.1.2.2 Register Group Locking Mechanism

There are some register groups that are locked together when a particular DW is read. This DW is called the Triggering DW. The value of a locked register group shall change only when the Triggering DW is accessed.

Table 8-5 lists the register groups that shall be locked.

Table 8-5. Locked Registers Groups

Group Name	Triggering DW	Locked Registers
Time Computation Group	TimeOffsetFromHR Low	<ul style="list-style-type: none"> • TimeOffsetFromHR Low • TimeOffsetFromHR High • TimeOffsetFromDFP Low • TimeOffsetFromDFP High • FrequencyOffsetFromHR • FrequencyOffsetFromDFP • Propagation Delay Low • Propagation Delay High • Computation Time Stamp Low • Computation Time Stamp Middle • Computation Time Stamp High • Received Counter Low • Received Counter High
Inter-Domain Computation Group	Inter-Domain Time Stamp Low	<ul style="list-style-type: none"> • Inter-Domain Time Stamp Low • Inter-Domain Time Stamp Middle • Inter-Domain Time Stamp High • TimeOffsetFromInterDomainHR Low • TimeOffsetFromInterDomainHR High • FrequencyOffsetFromInterDomainHR

8.2.1.3 Vendor Specific Capability (VSC)

A Vendor Specific Capability shall have the format and fields shown in Figure 8-4. The remaining fields within the Vendor Specific Registers are vendor defined.

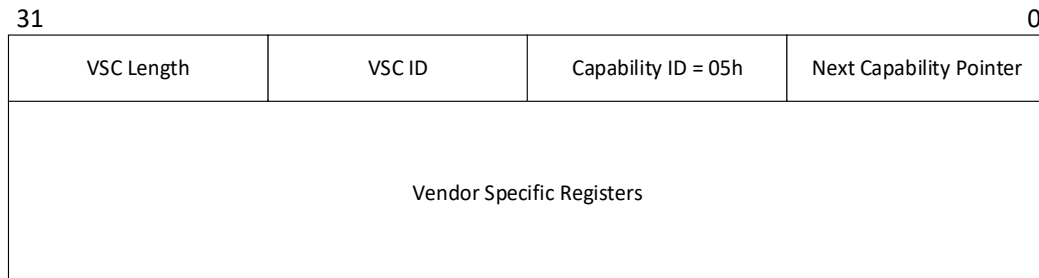
Figure 8-4. Structure of a Vendor Specific Capability

Table 8-6 describes the fields that a Vendor Specific Capability shall contain.

Table 8-6. Vendor Specific Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSC_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in Router Configuration Space. A Router shall set this field to 00h if the Vendor-Specific Capability is the final Capability in the linked list of Capabilities in Router Configuration Space.	RO	Vendor Defined
		15:8	Capability ID A Router shall set this field to 05h indicating this is the start of a Vendor-Specific Capability.	RO	05h
		23:16	VSC ID This field shall contain the vendor-defined ID number that identifies the nature and format of the VSC structure.	RO	Vendor Defined
		31:24	VSC Length This field shall contain the total number of Doublewords in the VSC structure including Doubleword 0 and the Vendor-Specific Doublewords that follow it.	RO	Vendor Defined

8.2.1.4 Vendor Specific Extended Capability (VSEC)

The Vendor Specific Extended Capability allows larger Capabilities to be defined, beyond the limitations of the Vendor Specific Capability. A Vendor Specific Extended Capability shall have the format and fields shown in Figure 8-5.

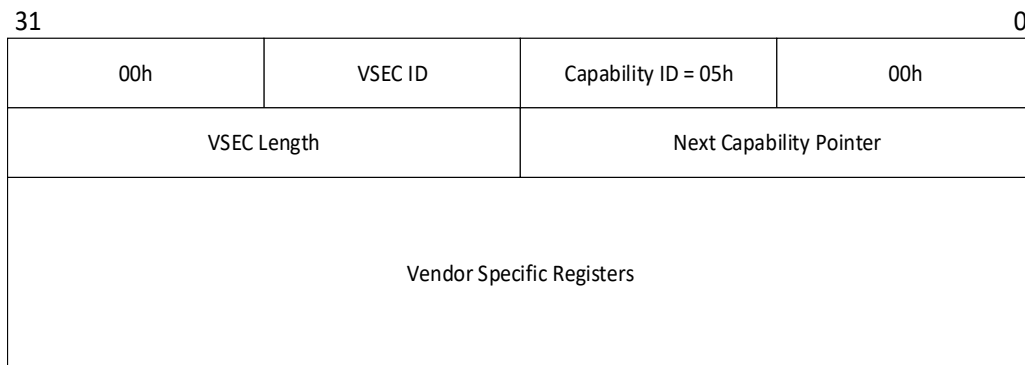
Figure 8-5. Structure of a Vendor Specific Extended Capability

Table 8-7 describes the fields that a Vendor Specific Extended Capability shall contain.

Table 8-7. Vendor Specific Extended Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_CS_0	7:0	Reserved	Rsvd	0
		15:8	Capability ID A Router shall set this field to 05h indicating this is the start of a Vendor-Specific Capability.	RO	05h
		23:16	VSEC ID This field shall contain the vendor-defined ID number that identifies the nature and format of the VSEC structure.	RO	Vendor Defined
		31:24	VSEC Header A Router shall set this field to 00h to indicate that the Capability is an Extended Capability.	RO	00h
1	VSEC_CS_1	15:0	Next Capability Pointer This field shall contains the Doubleword index of the next Capability in Router Configuration Space. A Router shall set this field to 00h if the Vendor-Specific Capability is the final Capability in the linked list of Capabilities in Router Configuration Space.	RO	Vendor Defined
		31:16	VSEC Length This field shall contain the total number of Doublewords in the VSEC structure including Doubleword 0, Doubleword 1, and the Vendor-Specific Doublewords that follow.	RO	Vendor Defined

A Vendor Specific Extended Capability may reside anywhere in the 8192 DWs that a Read or Write Request packet can address. It is recommended that the first Vendor Specific Extended Capability starts at DW address 255.

8.2.2 Adapter Configuration Space

Every Adapter (except for a Control Adapter) shall have its own Adapter Configuration Space. An Adapter Configuration Space shall have the structure depicted in Figure 8-6. The Adapter Configuration Space structure depicted in Figure 8-6 begins with a set of Doublewords describing the basic attributes of an Adapter. The rest of the space is populated with a linked list of Capabilities.

A Connection Manager reads from or writes to Adapter Configuration Space using the Read Requests and Write Requests defined in Section 6.4.2. A Router shall allow a Connection

Manager to access Adapter Configuration Space regardless of whether or not the Adapter is connected.



CONNECTION MANAGER NOTE

A Connection Manager shall not access the Adapter Configuration Capability Space of a Lane 1 Adapter in an Aggregated Link.

Figure 8-6. Structure of the Adapter Configuration Space

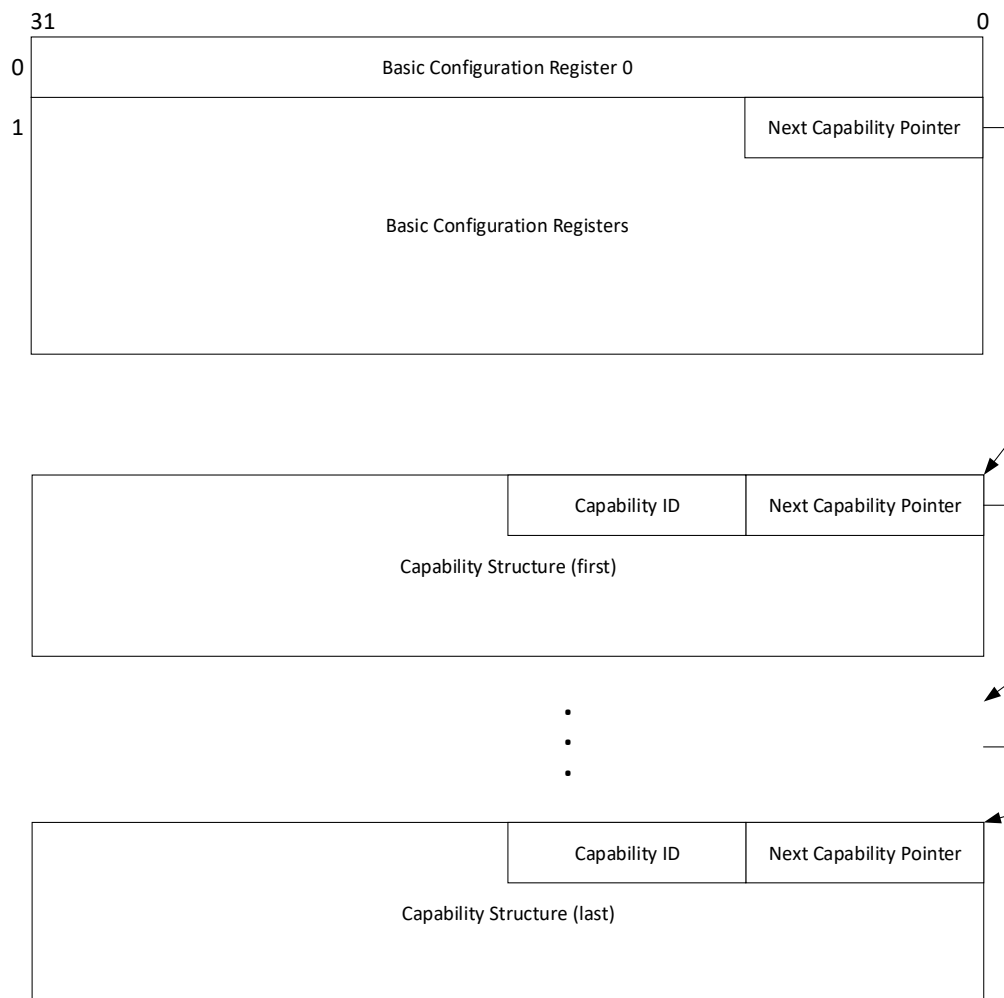


Table 8-8 lists the Configuration Capabilities supported by Adapter Configuration Space. A Capability listed as “Required” shall be present in Adapter Configuration Space. A Capability listed as “Optional” may be present in Adapter Configuration Space.

Table 8-8. List of Adapter Configuration Capabilities

Capability	Required / Optional	Capability ID
TMU Adapter Configuration	A TMU Adapter Configuration Capability is required for Lane Adapters. Shall not be present for any other Adapter.	03h
Lane Adapter Configuration	Required for Lane Adapters. Shall not be present for any other Adapter.	01h
USB4 Port Capability	Required for the Lane 0 Adapter in a USB4 Port. Shall not be present for any other Adapter.	06h

Capability	Required / Optional	Capability ID
PCIe Adapter Configuration	Required for PCIe Adapters. Shall not be present for any other Adapter.	04h
DP IN Adapter Configuration	Required for DP IN Adapters. Shall not be present for any other Adapter.	04h
DP OUT Adapter Configuration	Required for DP OUT Adapters. Shall not be present for any other Adapter.	04h
DP OUT AUX Adapter Configuration	Required for DP OUT AUX Adapters. Shall not be present for any other Adapter.	04h
USB3 Gen X Adapter Configuration	Required for USB3 Gen X Adapters. Shall not be present for any other Adapter.	04h
USB3 Gen T Adapter Configuration	Required for USB3 Gen T Adapters. Shall not be present for any other Adapter.	04h
Vendor Specific Adapter Configuration	Required for Vendor Specific Adapters.	04h
Vendor Specific	Optional.	05h

The number of Vendor Specific Capabilities and Vendor Specific Extended Capabilities is implementation specific. Section 8.2.1.3 defines the structure of the Vendor Specific Capability. Section 8.2.1.4 defines the structure of the Vendor Specific Extended Capability.

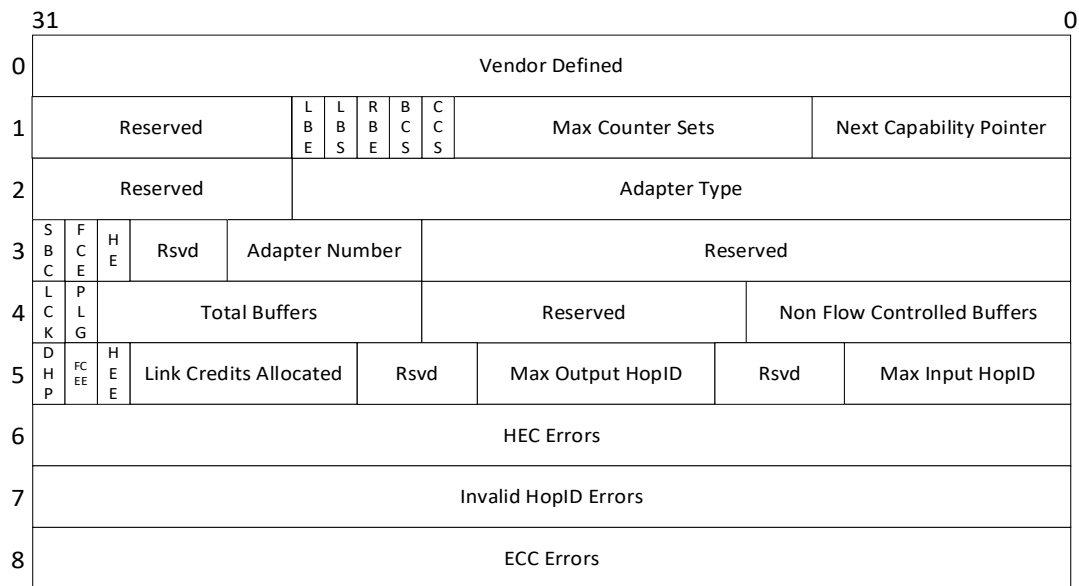
A Router's operation shall not depend on a Connection Manager's support for the Vendor Specific Capabilities and Vendor Specific Extended Capabilities.

Capabilities shall be linked in the following order:

- Required Capabilities.
- Optional Capabilities.
- Vendor Specific Capabilities.
- Vendor Specific Extended Capabilities.

8.2.2.1 Basic Configuration Registers

The first 9 Doublewords in an Adapter Configuration Space shall have the format and fields described in Figure 8-7 and Table 8-9.

Figure 8-7. Basic Configuration Registers of the Adapter Configuration Space**Table 8-9. Adapter Configuration Space Basic Attributes**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_CS_0	31:0	Vendor Defined	VD	Vendor Defined
1	ADP_CS_1	7:0	Next Capability Pointer This field shall contain the Doubleword index of the first Capability in the Adapter Configuration Space.	RO	Vendor Defined
		18:8	Max Counter Sets This field shall contain the number of counter sets provided by the Adapter in Counters Configuration Space. The value in this field shall be at least 1 if the <i>CCS Flag</i> is set to 1b. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined
		19	Counters Configuration Space (CCS) Flag An Adapter shall set this flag to 1b if it supports Counters Configuration Space. Otherwise this flag shall be set to 0b. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined
		20	Bytes Counter Supported (BCS) An Adapter shall set this flag to 1b if it supports Byte Counters. Otherwise, this flag shall be set to 0b. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		21	Received Bytes Counter Enable (RBE) When set to 0b, CNT_CS_0 and CNT_CS_1 are counting Transport Layer Packets. When set to 1b, CNT_CS_0 and CNT_CS_1 are counting bytes. This field applies to all counters for the Adapter. A Connection Manager shall not set this bit to 1b unless the <i>Bytes Counter Supported</i> bit is 1b. Writing to this bit in a Lane 1 Adapter results in undefined behavior.	R/W	0
		22	Lock Bytes Counter with TimeOffsetFromHR Low Supported (LBS) A Router uses this field to indicate whether the Lock Bytes Counter with TimeOffsetFromHR Low is supported: 0 – Not Supported 1 – Supported This field shall be set to 0b if the <i>Bytes Counter Supported</i> bit is set to 0b. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined
		23	Lock Bytes Counter with TimeOffsetFromHR Low Enable (LBE) When set to 0b, CNT_CS_0 and CNT_CS_1 reflect the current counter values. When set to 1b, the CNT_CS_0 and CNT_CS_1 values are only updated when the <i>TimeOffsetFromHR Low</i> field is read. See Section 8.2.4. A Connection Manager shall not set this bit to 1b unless the <i>Lock Bytes Counter with TimeOffsetFromHR Low Supported</i> bit is set to 1b and the <i>Received Bytes Counter Enable</i> bit is set to 1b. Writing to this bit in a Lane 1 Adapter results in undefined behavior.	RW	0
		31:24	Reserved	Rsvd	0
2	ADP_CS_2	7:0	Adapter Type Sub-type This field shall identify the Adapter sub-type using the Sub-Type encodings in Table 8-10.	RO	See Table 8-10
		15:8	Adapter Type Version This field shall identify the Adapter version using the version encodings in Table 8-10.	RO	See Table 8-10
		23:16	Adapter Type Protocol This field shall identify the Adapter protocol type using the Protocol encodings in Table 8-10.	RO	See Table 8-10
		31:24	Reserved This field shall be set to 01h.	Rsvd	01h
3	ADP_CS_3	19:0	Reserved	Rsvd	0
		25:20	Adapter Number This field shall contain the Adapter Number for the Adapter.	RO	Vendor Defined
		28:26	Reserved	Rsvd	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		29	HEC Error (HE) A Lane 0 Adapter sets this bit to 1b to indicate the reception of a Transport Layer Packet with an uncorrectable HEC error in the header. The Lane 1 Adapter shall set this bit to 0b. This field is reserved in a Protocol Adapter and shall be set to 0b.	R/Clr	0
		30	Flow Control Error (FCE) A Lane 0 Adapter sets this bit to 1b to indicate the reception of a Packet on a flow controlled Path when the appropriate buffer (dedicated or shared) has no space for the packet. The Lane 1 Adapter shall set this bit to 0b. This field is reserved in a Protocol Adapter and shall be set to 0b.	R/Clr	0
		31	Shared Buffering Capable (SBC) This bit indicates whether a USB4 Port is capable of sharing flow control buffers among flow controlled Paths. A Lane 0 Adapter shall set this bit to 1b if Shared Buffering is supported. A Lane 0 Adapter shall set this bit to 0b if Shared Buffering is not supported. The Lane 1 Adapter shall set this bit to 0b. This field is ignored in a Protocol Adapter.	RO	USB4 Hub: 1b Else: Vendor Defined
4	ADP_CS_4	9:0	Non-Flow Controlled Buffers A Connection Manager uses this field to configure the number of ingress buffers allocated for non-flow-controlled Paths in a Lane Adapter. A Connection Manager may change this field dynamically when setting up or tearing down a Path. This field is not used for a Protocol Adapter. Writing to this field in a Lane 1 Adapter results in undefined behavior.	R/W	0
		19:10	Reserved	Rsvd	0
		29:20	Total Buffers This field shall contain the total number of ingress buffers available to a Lane Adapter as defined in Section 5.3.2.1.1. <i>Note: The value in the Total Buffers field includes any buffers for Path 0.</i> This field is ignored in a Protocol Adapter. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined
		30	Plugged This field indicates whether the Adapter is plugged. 0b – Adapter is not plugged 1b – Adapter is plugged This field is reserved in a USB3 Adapter, a DP IN Adapter, a PCIe Adapter, and a Host Interface Adapter, and shall be set to 0. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		31	Lock (LCK) This bit controls whether a Connection Manager can access a Router that is downstream of a Lane Adapter. When the bit is 1b, the Adapter is “locked”, which means that Control Packets are not forwarded to the downstream Router. When the bit is 0b, the Adapter is “unlocked” and Control Packets can be forwarded to the downstream Router. An Adapter shall set this bit to 1b after the Adapter goes through a disconnect. An Adapter may ignore a write to this bit if the Adapter does not have a Router connected downstream. This bit is reserved in an Adapter in an Upstream Facing Port and shall be set to 0b. This bit is reserved in a Protocol Adapter and shall be set to 0b. Writing to this bit in a Lane 1 Adapter results in undefined behavior. See Section 6.7 for more information on the functionality of this bit.	R/W	0b
5	ADP_CS_5	6:0	Max Input HopID This field shall contain the highest HopID value the Adapter supports for incoming packets. For a Host Interface Adapter: the value in this field shall equal the number of total Paths supported by the Host Interface minus one. In a PCIe Host Interface Adapter Layer, the number of total Paths is in the <i>Total Paths</i> field in the Host Interface Capabilities Register. For a USB3 Gen T Adapter: the value of this field shall equal 8 + the value in the <i>Gen T Port Count</i> field in the USB3 Gen T Adapter Configuration Space minus one. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined
		10:7	Reserved	Rsvd	0h
		17:11	Max Output HopID This field shall contain the highest HopID value the Adapter supports for outgoing packets. For a Host Interface Adapter: the value in this field shall equal the number of total Paths supported by the Host Interface minus one. In a PCIe Host Interface Adapter Layer, the number of total Paths is in the <i>Total Paths</i> field in the Host Interface Capabilities Register. For a USB3 Gen T Adapter: the value of this field shall equal 8 + the value of the <i>Gen T Port Count</i> field in the USB3 Gen T Adapter Configuration Space minus one. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined
		21:18	Reserved	Rsvd	0h
		28:22	Link Credits Allocated A Connection Manager uses this field to configure the initial number of credits to be allocated to the Shared Flow Control Buffer used by the Ingress Lane Adapter. This field is not used for a Protocol Adapter. Writing to this field in a Lane 1 Adapter results in undefined behavior.	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		29	HEC Error Enable (HEE) A Connection Manager uses this field to enable HEC error reporting in a Lane Adapter as follows: 1b – HEC error reporting enabled 0b – HEC error reporting disabled This bit is Reserved for a Lane 1 Adapter. This field is only used for Lane Adapters. It is ignored for Protocol Adapters.	R/W	0b
		30	Flow Control Error Enable (FCEE) A Connection Manager uses this field to enable Flow Control error reporting in a Lane Adapter as follows: 1b – FCEE error reporting enabled 0b – FCEE error reporting disabled This bit is Reserved for a Lane 1 Adapter. This field is only used for Lane Adapters. It is ignored for Protocol Adapters.	R/W	0b
		31	Disable Hot Plug Events (DHP) A Connection Manager uses this bit to configure whether the Router sends a Hot Plug Event Packet as a result of a Hot Plug Event or a Hot Unplug Event on this Adapter. 1b – Hot Plug Event Packet not sent 0b – Hot Plug Event Packet is sent Only a Lane Adapter, a DP IN Adapter, or a DP OUT Adapter may optionally implement this bit. All other Adapters shall hardwire this bit to 0b. Writing to this bit in a Lane 1 Adapter results in undefined behavior.	R/W	0b
6	ADP_CS_6	31:0	HEC Errors This field shall contain the number of ingress Transport Layer Packets dropped due to HEC errors. A Lane Adapter shall increment the counter in this field from 0 and shall stop counting at FFFF FFFFh. A Protocol Adapter shall not increment the counter and shall set this field to 0. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager. Writing to this field in a Lane 1 Adapter results in undefined behavior.	W/Clr	0
7	ADP_CS_7	31:0	Invalid HopID Errors This field shall contain the number of ingress Transport Layer Packets with a HopID outside the supported range or a HopID that does not belong to an enabled Path. An Adapter shall increment the counter in this field from 0 and shall stop counting at FFFF FFFFh. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager. Writing to this field in a Lane 1 Adapter results in undefined behavior.	W/Clr	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
8	ADP_CS_8	31:0	ECC Errors This field shall contain the number of Credit Sync Packets and Credit Grant Records dropped due to ECC errors. A Lane Adapter shall increment the counter in this field from 0 and shall stop counting at FFFF FFFFh. A Protocol Adapter shall not increment the counter and shall set this field to 0. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager. Writing to this field in a Lane 1 Adapter results in undefined behavior.	W/Clr	0

Table 8-10. Adapter Types

Type	Protocol	Version	Sub-Type
Unsupported Adapter	00h	00h	00h
Lane Adapter	00h	00h	01h
Host Interface Adapter	00h	00h	02h
Downstream PCIe Adapter	10h	01h	01h
Upstream PCIe Adapter	10h	01h	02h
DP IN Adapter	0Eh	01h	01h
DP OUT Adapter	0Eh	01h	02h
DP OUT AUX Adapter	0Eh	01h	03h
Downstream USB3 Gen X Adapter	20h	01h	01h
Upstream USB3 Gen X Adapter	20h	01h	02h
Downstream USB3 Gen T Adapter	21h	01h	01h
Upstream USB3 Gen T Adapter	21h	01h	02h
Vendor Specific Adapter	FFh	Vendor Defined	Vendor Defined

**CONNECTION MANAGER NOTE**

When writing to the Adapter Configuration Space of a Protocol Adapter, a Connection Manager shall not change the value in the following fields:

- *Non-Flow Controlled Buffers.*
- *Link Credits Allocated.*

A Connection Manager shall set the Disable Hot Plug Events bit to the desired value:

- *In a Downstream Facing Port, before the Lock bit for the Port is set to 0b.*
- *In a DP IN Adapter or a DP OUT Adapter, before the AUX Enable bit or the Video Enable bit are set to 1b.*

A Connection Manager shall set the following bits to the desired value before the Counter Enable bit is set to 1b for any Path going through the Lane Adapter:

- *Received Bytes Counter Enable.*
- *Lock Bytes Counter with TimeOffsetFromHR Low Enable.*

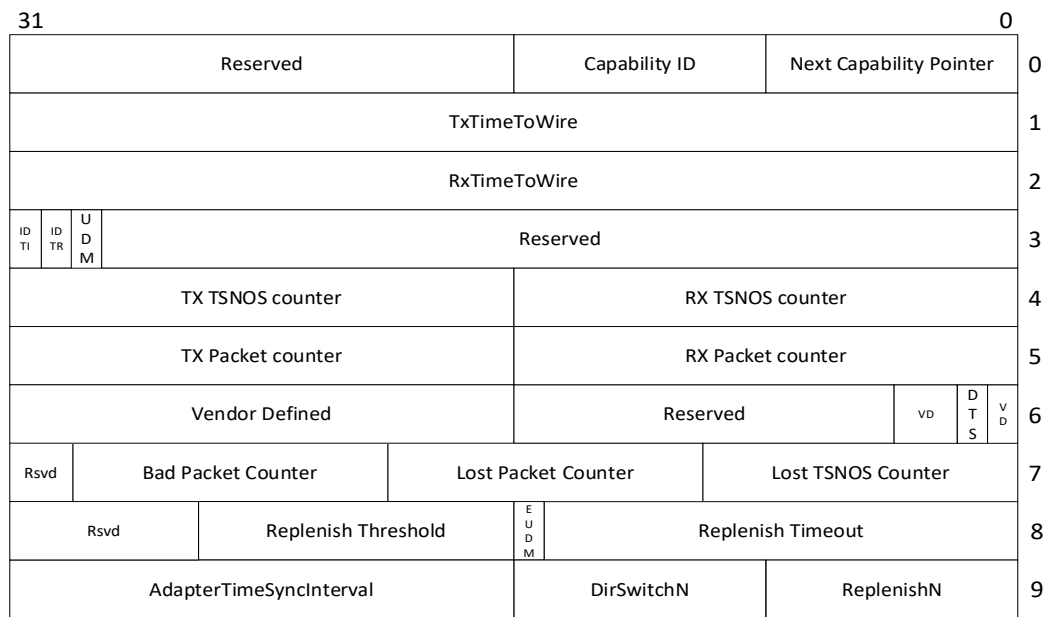
A Connection Manager shall not write to the Basic Configuration Registers of the Adapter Configuration Space in a Lane 1 Adapter.

8.2.2.2 TMU Adapter Configuration Capability

A TMU Adapter Configuration Capability shall have the structure depicted in Figure 8-8 and shall contain the fields defined in Table 8-11.

A Router that does not support the Time Synchronization Protocol may implement all the fields in this section as Read Only (RO) type.

For a USB4 Port with two enabled Lane Adapters, the values in the TMU Adapter Configuration Capability of both Adapters shall be identical. When a value in the TMU Adapter Configuration Capability of one Lane Adapter is written to, the other Lane Adapter in the USB4 Port shall update its value to match.

Figure 8-8. Structure of the TMU Adapter Configuration Capability**Table 8-11. TMU Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	TMU_ADP_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. A Router shall set this field to 00h if the TMU Adapter Configuration Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 03h indicating this is the start of a TMU Adapter Configuration Capability.	RO	03h
		31:16	Reserved	Rsvd	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	TMU_ADP_CS_1	31:0	TxTimeToWire This field shall contain the time duration from the instant the time stamp is taken at the Physical Layer to the instant when the first bit of the TSNOS is transmitted on the wire. The time shall be specified in nanoseconds multiplied by 2^{16} . For example, 2.5 ns is represented as 0000 0002 8000h. <i>Note: The value in this field may vary as Link parameters change (e.g. speed, RS-FEC on/off, number of transmitters, etc.).</i>	RO	Vendor Defined
2	TMU_ADP_CS_2	31:0	RxTimeToWire This field shall contain the time duration from the instant the first bit of the TSNOS is received at the wire to the instant when the time stamp is taken at the Physical Layer. The time shall be specified in nanoseconds multiplied by 2^{16} . For example, 2.5 ns is represented as 0000 0002 8000h. <i>Note: The value in this field may vary as Link parameters change (e.g. speed, RS-FEC on/off, number of transmitters, etc.).</i>	RO	Vendor Defined
3	TMU_ADP_CS_3	28:0	Reserved	Rsvd	0
		29	EnableUniDirectionalMode (UDM) A Connection Manager uses this bit to enable Uni-Directional Time Sync Handshakes. The TMU Adapter shall set this bit to 0b when its USB4 Port is disconnected.	R/W	0
		30	Inter-Domain Time Responder (IDTR) A Connection Manager uses this bit to configure the USB4 Port as an Inter-Domain Time Responder (i.e. the responder to Time Sync Handshakes across an Inter-Domain Link). If set to 1b, the USB4 Port shall respond to Time Sync Handshakes over the Inter-Domain Link as initiated by the ITDI Port. Otherwise this bit shall be set to 0b.	R/W	0
		31	Inter-Domain Time Initiator (IDTI) A Connection Manager uses this bit to configure the USB4 Port as an Inter-Domain Time Initiator (i.e. the initiator of Time Sync Handshakes across an Inter-Domain Link). Setting this bit to 1b in a Downstream Facing Port is optional. A Connection Manager shall only set this bit to 1b in a Downstream Facing Port if the Host Router of its Domain supports Inter-Domain Time Synchronization. If set to 1b, the USB4 Port shall Initiate Time Sync Handshakes over the Inter-Domain Link. Otherwise this bit shall be set to 0b.	R/W	0
4	TMU_ADP_CS_4	15:0	RX TSNOS Counter This field shall contain the number of TSNOS received by TMU. The counter shall not increment past FFFFh. For a Gen 4 Link, this field shall increase by 1 for each 24 Gen 4 TSNOS received.	R/Clr	0
		31:16	TX TSNOS Counter This field shall contain the number of TSNOS sent by TMU. The counter shall not increment past FFFFh. For a Gen 4 Link, this field shall increase by 1 for each 24 Gen 4 TSNOS transmitted.	R/Clr	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
5	TMU_ADP_CS_5	15:0	RX Packet Counter This field shall contain the number of Time Sync Packets received by TMU. The counter shall not increment past FFFFh.	R/Clr	0
		31:16	TX Packet Counter This field shall contain the number of Time Sync Packets sent by TMU. The counter shall not increment past on FFFFh.	R/Clr	0
6	TMU_ADP_CS_6	0	Vendor Defined	VD	Vendor Defined
		1	Disable Time Sync (DTS) A Connection Manager uses this bit to disable Time Synchronization Handshake initiation. If set to 1b, the Adapter shall not send any Delay Requests or Delay Responses. If set to 0b, the Adapter may send Delay Requests or Delay Responses.	R/W	0
		3:2	Vendor Defined	VD	Vendor Defined
		15:4	Reserved	RsvdZ	0
		31:16	Vendor Defined	VD	Vendor Defined
7	TMU_ADP_CS_7	9:0	Lost TSNOS Counter This field shall contain the number of times that a Delay Response was expected during a Time Sync Handshake but not received. The counter shall not increment past 3FFh.	R/Clr	0
		19:10	Lost Packet Counter This field shall contain the number of times that a Follow-Up Packet was expected during a Time Sync Handshake but not received. The counter shall not increment past 3FFh. <i>Note: Only an Upstream Facing Port increments this counter (a Downstream Facing Port does not receive Follow-Up Packets).</i>	R/Clr	0
		29:20	Bad Packet Counter This field shall contain the number of Follow-Up Packets and Inter-Domain Packets received with bad CRC. The counter shall not increment past 3FFh.	R/Clr	0
		31:30	Reserved	Rsvd	0
8	TMU_ADP_CS_8	14:0	Replenish Timeout This field contains the maximum of <i>Replenish Timeout</i> skipped handshakes while the Adapter is in CL1 or CL0s (TX) state. If an Adapter is in CL1 or CL0s (TX) state for more than this number of skipped handshakes (Replenish Timeout), the DFP shall assert an objection.	R/W	0
		15	Enable Enhanced Uni-Directional Mode (EUDM) When this bit is set to 1b, the USB4 Port shall use Enhanced Uni-Directional Time Sync Handshakes. <u>The TMU Adapter shall set this bit to 0b when its USB4 Port is disconnected.</u>	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
9	TMU_ADP_CS_9	25:16	Replenish Threshold This field contains the number of missed Time Sync Handshakes that requires an objection to CL1 state. If more than <i>Replenish Threshold</i> handshakes are missed, the TMU shall assert an objection to CLx until it finishes at least <i>ReplenishN</i> handshakes. Shall be set to a lower value than in the <i>Replenish Timeout</i> field.	R/W	0
		31:26	Reserved	RO	0
		7:0	ReplenishN This field contains the minimum number of successful handshakes that shall be completed after missing <i>Replenish Threshold</i> handshakes before removing the objection to CL1 state.	R/W	0
9	TMU_ADP_CS_9	15:8	DirSwitchN This field contains the number of handshakes that are required in Inversed Bi-Directional mode before the transition to Adaptive Uni-Directional mode. This field shall be greater than 1 when Enhanced Uni-Directional Time Sync Handshakes are enabled.	R/W	0
		31:16	AdapterTimeSyncInterval This field contains the time interval between successive Time Sync handshakes. The time interval is specified in units of 1 μ s with 100ppm accuracy. This field is only used when Enhanced Uni-Directional mode is enabled. There are two allowed values for this register: 0: Shall disable the initiation of Time Sync Handshake from the USB4 Port. 16: "HiFi" Mode (16 μ s). All other values are reserved.	R/W	0



CONNECTION MANAGER NOTE

A Ver. 2 Connection Manager shall set the values in the TMU Adapter Configuration Capability of an Upstream Facing Port before it sets the Configuration Valid bit of the Router to 1b.

A Connection Manager shall use the following values to configure the TMU to HiFi Accuracy when using Enhanced Uni-Directional mode:

- *Replenish Timeout = 3125*
- *Replenish Threshold = 0*
- *ReplenishN = 30*
- *DirSwitchN = 255*
- *AdapterTimeSyncInterval = 16*

8.2.2.3 Lane Adapter Configuration Capability

A Lane Adapter Configuration Capability shall have the structure depicted in Figure 8-9 and shall have the fields defined in Table 8-12.

Figure 8-9. Structure of the Lane Adapter Configuration Capability

31													0												
0	Rsvd			CLx Support		Rsvd	G4AS	SLW	Supported Link Speeds		Capability ID					Next Capability Pointer									
1	Rs vd	P MS	Adapter State			Negotiated Link Width			Current Link Speed		L B	L D	Rs vd	CLx Enable	Target Asymmetric Link	Target Link Width		Target Link Speed							
2	Reserved							Logical Layer Errors Enable				Reserved					Logical Layer Errors								

Table 8-12. Contents of the Lane Adapter Configuration Capability

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	LANE_ADP_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. An Adapter shall set this field to 00h if this Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 01h indicating this is a Lane Adapter Configuration Capability.	RO	01h
		19:16	Supported Link Speeds This field indicates which Link speed(s) are supported by the Adapter. Bit definitions within this field are: Bit [16] Rsvd Bit 17 Gen 4 Bit 18 Gen 3 Bit 19 Gen 2 For a USB4 Host or USB4 Peripheral Device: <ul style="list-style-type: none"> An Adapter shall set bit 17 to 1b if it supports Gen 4 speed, all On-Board Re-timers connected between the USB4 Port and the Type-C connector support Gen 4 speed. Otherwise, bit 17 shall be 0b. An Adapter shall set bit 18 to 1b if it supports Gen 3 speed, all On-Board Re-timers connected between the USB4 Port and the Type-C connector support Gen 3 speed. Otherwise, bit 18 shall be 0b. An Adapter shall set bit 19 to 1b to indicate support for Gen 2 speed. For a USB4 Hub: <ul style="list-style-type: none"> An Adapter shall set bit 17 to 1b if it supports Gen 4 speed, all On-Board Re-timers connected between the USB4 Port and the Type-C connector support Gen 4 speed. Otherwise, bit 17 shall be 0b. An Adapter shall set bit 18 to 1b to indicate support for Gen 3 speed. An Adapter shall set bit 19 to 1b to indicate support for Gen 2 speed. The Lane 1 Adapter in a USB4 Port shall declare the same value as the Lane 0 Adapter.	RO	Vendor Defined

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		21:20	Supported Link Widths (SLW) This field indicates which Link widths are supported by the Adapter (xN – corresponding to N Lanes). Bit definitions within this field are: Bit 20 x1 Bit 21 x2 An Adapter shall set bit 20 to 1b to indicate support for x1 operation. An Adapter shall set bit 21 to 1b to indicate support for x2 operation. Lane 1 Adapter in a USB4 Port shall declare the same value as the Lane 0 Adapter. This field is only valid for Gen 2 and Gen 3 Links.	RO	11b
		23:22	Gen 4 Asymmetric Support (G4AS) This field indicates which Asymmetric Link configurations are supported by the Adapter. Bit definitions within this field are: Bit 22 Support 3 Tx Bit 23 Support 3 Rx An Adapter shall set bit 22 to 1b if all the following are true: <ul style="list-style-type: none"> The USB4 Port supports Gen 4 speed and Asymmetric Link with three transmitters. All On-Board Re-timers connected between the USB4 Port and the Type-C connector support Gen 4 speed and Asymmetric Link with three transmitters. An Adapter shall set bit 23 to 1b if all the following are true: <ul style="list-style-type: none"> The USB4 Port supports Gen 4 speed and Asymmetric Link with three receivers. All On-Board Re-timers connected between the USB4 Port and the Type-C connector support Gen 4 speed and Asymmetric Link with three receivers. <i>Note: The method to convey the capabilities of an On-Board Re-timer to the Router is implementation specific.</i> The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined
		25:24	Reserved	RO	00b
		26	CL0s Support An Adapter shall set this field to 1b if it supports the CL0s Low Power state. Otherwise this bit shall be set to 0b. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined See Note 1
		27	CL1 Support An Adapter shall set this field to 1b if it supports the CL1 Low Power state. Otherwise this bit shall be set to 0b. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined See Note 1

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		28	CL2 Support An Adapter shall set this bit to 1b if it supports the CL2 Low Power state. Otherwise this bit shall be set to 0b. The value in this field is vendor defined in a Lane 1 Adapter and shall be ignored by the Connection Manager.	RO	Vendor Defined See Note 1
		31:29	Reserved	Rsvd	000b
1	LANE_ADAP_CS_1	3:0	Target Link Speed A Connection Manager uses this field to indicate which Link speed the Router attempts to establish for the USB4 Port. Defined encodings are: 1000b – Router shall attempt Gen 2 speed 1100b – Router shall attempt Gen 3 speed 1110b – Router shall attempt Gen 4 speed All other encodings are reserved. If the Router enters sleep state and there is no disconnect, the USB4 Port shall restore the value of this field upon exit from sleep. A Lane 1 Adapter may ignore a write to this field.	R/W	Host Router: Vendor Defined Device Router: Shall match the highest speed supported by the Lane
		5:4	Target Link Width A Connection Manager uses this field to indicate the Link width that the Router attempts to establish for the USB4 Port. Defined encodings are: 01b – Establish two Single-Lane Links 11b – Establish a Symmetric Link All other encodings are reserved. This field is only valid for Gen 2 and Gen 3 Links.	R/W	01b
		7:6	Target Asymmetric Link A Connection Manager uses this field to indicate the Asymmetric Link configuration that the Router attempts to establish for the USB4 Port. Defined encodings are: 00b – Establish Symmetric Link 01b – Establish Asymmetric Link with 3 transmitters 10b – Establish Asymmetric Link with 3 receivers All other encodings are reserved. If the Router enters sleep state and there is no disconnect, the USB4 Port shall restore the value of this field upon exit from sleep. This field is ignored for Gen 2 and Gen 3 Links. A Lane 1 Adapter may ignore a write to this field. <i>Note: This field can be changed by SET_LINK_TYPE Operation.</i>	R/W S	Vendor Defined
		9:8	Reserved	RO	00b
		10	CL0s Enable A Connection Manager uses this bit to control whether the Adapter can enter CL0s state <u>in Gen 2 and Gen 3 Links</u> . 0b – entry to CL0s state is disabled 1b – entry to CL0s state is enabled <u>This field is ignored for Gen 4 Link.</u> A Lane 1 Adapter may ignore a write to this field.	R/W	0b

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		11	CL1 Enable A Connection Manager uses this bit to control whether the Adapter can enter CL1 state. 0b – entry to CL1 state is disabled 1b – entry to CL1 state is enabled A Lane 1 Adapter may ignore a write to this field.	R/W	0b
		12	CL2 Enable A Connection Manager uses this bit to control whether the Adapter can enter CL2 state. 0b – entry to CL2 state is disabled 1b – entry to CL2 state is enabled A Lane 1 Adapter may ignore a write to this field.	R/W	0b
		13	Reserved	Rsvd	0b
		14	Lane Disable (LD) A Connection Manager sets this bit to 1b to transition the Adapter to the Disabled state. A Connection Manager sets this bit to 0b to transition the Adapter out of the Disabled state. <i>Note: Writing to this bit is immediately reflected in the value read from the bit, regardless of actual Adapter state.</i>	R/W	0
		15	Lane Bonding (LB) A Connection Manager sets this bit to 1b in either Adapter of a USB4 Port to transition the Adapters to the Lane Bonding state. Writing 0b to this bit shall have no effect. If the Adapter is already in the Lane Bonding state when this bit is set to 1b, the Adapter may reenter the Lane Bonding state after Lane Bonding is complete but is not required to do so. For a Gen 4 Link, when this bit is set to 1b, the Adapter shall clear it to 0b. A Lane 1 Adapter may ignore a write to this field.	R/W SC	0
		19:16	Current Link Speed This field shall indicate the negotiated Link speed. Defined encodings are: 1000b Gen 2 0100b Gen 3 0010b Gen 4 All other encodings are reserved. The Lane 1 Adapter in a USB4 Port shall contain the same value as the Lane 0 Adapter. This field is only valid when the Link is in the Active state.	RO	Vendor Defined

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		25:20	Negotiated Link Width This field shall indicate the negotiated Link width. Defined encodings are: 000001b Single-Lane Link (x1) 000010b Symmetric Link (x2) 000100b Asymmetric Link with 3 transmitters 001000b Asymmetric Link with 3 receivers All other encodings are reserved. The Lane 1 Adapter in a USB4 Port shall contain the same value as the Lane 0 Adapter. This field is only valid when the Link is in the Active state.	RO	Vendor Defined
		29:26	Adapter State This field shall indicate the current Adapter state. Defined encodings are: 0000b: Disabled state 0001b: Training or Lane Bonding state 0010b: CL0 state 0011b: Transmitter in CL0s state 0100b: Receiver in CL0s state 0101b: CL1 state 0110b: CL2 state 0111b: CLd state All other encodings are reserved.	RO	7h
		30	PM Secondary (PMS) A Connection Manager uses this field to indicate whether the Adapter is a PM Secondary Adapter. 0b – Adapter is not a PM Secondary Adapter 1b – Adapter is a PM Secondary Adapter A Lane 1 Adapter may ignore a write to this field.	R/W	1b
		31	Reserved	RsvdZ	0b
2	LANE_ADP_CS_2	6:0	Logical Layer Errors An Adapter uses this field to indicate the occurrence of a Logical Layer Error. See Section 4.4.2. Bit 0 – Aligner Lock Error (ALE) Bit 1 – Order Set Error (OSE) Bit 2 – Timing Error (TE) Bit 3 – Elastic Buffer Error (EBE) Bit 4 – De-Skew Buffer Error (DBE) Bit 5 – RS-FEC Decoder Error (RDE) Bit 6 – RX Sync Timeout (RST) For an Aggregated Link, this field is not valid in the Lane 1 Adapter.	R/Clr	00h
		15:7	Reserved	Rsvd	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		22:16	Logical Layer Errors Enable A Connection Manager uses this field to enable Logical Layer error reporting. See Section 4.4.2. When a bit is set to 1b, the corresponding error is reported by a Notification Packet: Bit 0 – Alignment Lock Error (ALE) Bit 1 – Order Set Error (OSE) Bit 2 – Timing Error (TE) Bit 3 – Elastic Buffer Error (EBE) Bit 4 – De-Skew Buffer Error (DBE) Bit 5 – RS-FEC Decoder Error (RDE) Bit 6 – RX Sync Timeout (RST) For an Aggregated Link, writing to this field in the Lane 1 Adapter results in undefined behavior.	R/W	00h
		31:23	Reserved	Rsvd	0
Notes: 1. The <i>CL0s Support</i> , <i>CL1 Support</i> , and <i>CL2 Support</i> bits may change according to the negotiated Link Speed.					



CONNECTION MANAGER NOTE

A Connection Manager shall only write to DW1 in a Lane 1 Adapter to disable or enable the Lane. When writing to DW1 in a Lane 1 Adapter, a Connection Manager shall write to any R/W field other than the Lane Disable bit the same value written to the Lane 0 Adapter of the same USB4 Port.

A Connection Manager shall not write to DW2 in the Lane 1 Adapter of an Aggregated Link.

8.2.2.4 USB4 Port Capability

A USB4 Port Capability shall have the structure depicted in Figure 8-10 and shall have the fields defined in Table 8-13.

Figure 8-10. Structure of USB4 Port Capability

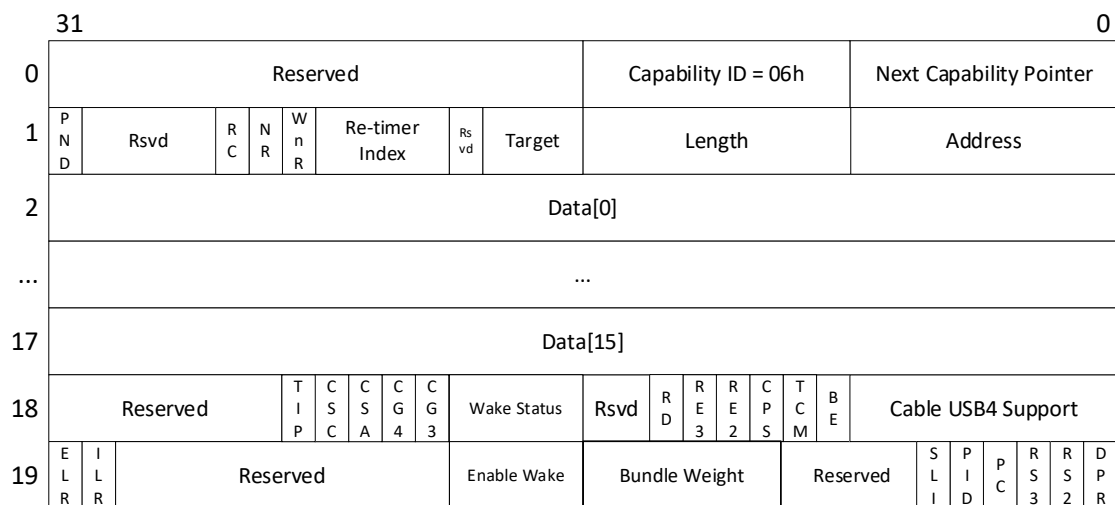


Table 8-13. USB4 Port Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	PORT_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. An Adapter shall set this field to 00h if the Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 06h indicating this is USB4 Port Capability.	RO	06h
		31:16	Reserved	Rsvd	0
1	PORT_CS_1	7:0	Address A Connection Manager uses this field when it initiates a read or write to SB Register Space. This field indicates the 8-bit address of the register in the SB Register Space that is the target of the read/write.	R/W	0
		15:8	Length A Connection Manager uses this field when it initiates a read or write to SB Register Space. This field indicates the number of bytes to read/write. After executing a read or write to the SB Register Space, a Router shall set this field to the value of the <i>LEN</i> field in the AT Response, the RT Response, or the local access.	R/W	0
		18:16	Target A Connection Manager uses this field when it initiates a read or write to SB Register Space. This field defines which SB Register Space to access: 000b – Router (via local access) 001b – Link Partner (via AT Transaction) 010b – Re-timer (via RT Transaction) All other encodings are reserved.	R/W	0
		19	Reserved	Rsvd	0
		23:20	Re-timer Index A Connection Manager uses this field when it initiates a read or write to SB Register Space. When the <i>Target</i> field is 010b, this field contains the Re-timer Index of the target Re-timer. Otherwise, this field is reserved and set to 0.	R/W	0
		24	WnR A Connection Manager uses this field to indicate whether it is initiating a read or a write: 0b – Read 1b – Write	R/W	0b
		25	No Response (NR) A Router uses this field when a Connection Manager initiates a read or write to SB Register Space. A Router shall set this bit to 1b if it did not receive a response for the read/write (including after any retransmissions), otherwise it shall be set to 0. This field is only valid when the <i>Pending</i> bit is set to 0b.	R/W	0b

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		26	Result Code (RC) A Router uses this field when a Connection Manager initiates a read or write to SB Register Space. For a Read operation: A Router shall set this bit to 0b if the <i>LEN</i> field in the AT Response or the RT Response is greater than zero, or if a local access completes successfully. A Router shall set this bit to 1b if the <i>LEN</i> field in the AT Response or the RT Response is 0, or if a local access completes unsuccessfully. For a Write operation: A Router shall set this bit to the value of the Result Code in the AT Response or the RT Response. For a local access, a Router shall set this bit to 0b if the access completes successfully. A Router shall set this bit to 1b if the access completes unsuccessfully. This field is only valid when the <i>Pending</i> bit is set to 0b.	R/W	0b
		30:27	Reserved	Rsvd	0
		31	Pending (PND) A Connection Manager sets this bit to 1b to initiate a read or write to SB Register Space. A Router shall set this bit to 0b after it finishes the SB Register Space read/write.	R/W	0b
17:2	PORT_CS_17 – PORT_CS_2	31:0	Data [15:0] A Router uses these fields when a Connection Manager initiates a read or write to SB Register Space. For a write: The Connection Manager sets these fields to contain the Doublewords to be written to the SB Register Space. For a read: The Router shall set these fields to contain the Doublewords read from the SB Register Space. Doublewords shall be arranged in increasing address order, starting at DW2 of the USB4 Port Capability and ending with the last Doubleword written/read.	R/W	0
18	PORT_CS_18	7:0	Cable USB4 Support This field shall identify whether the USB Type-C® cable connected to the Port supports USB4. Allocated values: 0Xh –Cable does not support USB4 10h –Cable supports USB4 Note: all USB Full-Featured Type-C® cables other than a TBT3 Active cable support USB4 for the purposes of this field. All other encodings are reserved. The value in this field is only valid when a USB Type-C® cable connected to the Port.	RO	10h
		8	Bonding Enabled (BE) An Adapter shall set this bit to 1b when the conditions for Lane bonding are met (See Section 4.1.2.3). Otherwise, this bit shall be set to 0b. This bit shall be set to 1b for a Gen 4 Link.	RO	0
		9	TBT3-Compatible Mode (TCM) An Adapter shall set this bit to 1b when the Link is operating in TBT3-Compatible Mode. This bit is set to 0b otherwise.	RO	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		10	CLx Protocol Support (CPS) This bit indicates that the Router and connected Cable support the Low Power protocol. When a Router supports the Low Power protocol, it either accepts or rejects entry to a Low Power (CLx) state as defined in Section 4.2.1.6. A Router shall set this bit to 0b if a Cable that does not support CLx states is connected to the Port. Otherwise, Router shall set this bit to 1b. The value of this bit is applicable when the Adapter is not in CLd nor Disabled state.	RO	Vendor Defined
		11	RS-FEC Enabled (Gen 2) (RE2) An Adapter shall set this bit to 1b when the USB4 Port operates in Gen 2 and RS-FEC is enabled. This bit shall be set to 0b otherwise.	RO	0
		12	RS-FEC Enabled (Gen 3) (RE3) An Adapter shall set this bit to 1b when the USB4 Port operates in Gen 3 and RS-FEC is enabled. This bit shall be set to 0b otherwise.	RO	0
		13	Router Detected (RD) An Adapter shall set this bit to 1b when the USB4 Port detects a connected Router (see Section 4.1.2.2) An Adapter shall set this bit to 0b upon a disconnect.	RO	0
		15:14	Reserved	Rsvd	0
		16	Wake on Connect Status An Adapter shall set this bit to 1b after a wake event is generated by the USB4 Port as a result of a connect to the USB4 Port. This bit shall not be set to 1b unless the <i>Enable Wake on Connect</i> bit is 1b. This bit shall be set to 0b on entry to sleep.	RO	0
		17	Wake on Disconnect Status An Adapter shall set this bit to 1b after a wake event is generated by the USB4 Port as a result of a disconnect from the USB4 Port. This bit shall not be set to 1b unless the <i>Enable Wake on Disconnect</i> bit is 1b. This bit shall be set to 0b on entry to sleep.	RO	0
		18	Wake on USB4 Wake Status An Adapter shall set this bit to 1b after a wake event is generated by the USB4 Port as a result of a USB4 Wake. This bit shall not be set to 1b unless the <i>Enable Wake on USB4 Wake</i> bit is 1b. This bit shall be set to 0b on entry to sleep.	RO	0
		19	Wake on Inter-Domain Status An Adapter shall set this bit to 1b after a wake event is generated by the USB4 Port as a result of an Inter-Domain Wake. This bit shall not be set to 1b unless the <i>Enable Wake on Inter-Domain</i> bit is 1b. This bit shall be set to 0b on entry to sleep.	RO	0
		20	Cable Gen 3 Support (CG3) An Adapter shall set this bit to 1b if its USB4 Port is connected to a Cable that supports Gen 3 Speed.	RO	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		21	Cable Gen 4 Support (CG4) An Adapter shall set this bit to 1b if its USB4 Port is connected to a Cable that supports Gen 4 Speed.	RO	0
		22	Cable Asymmetric Support (CSA) An Adapter shall set this bit to 1b if its USB4 Port is connected to a Cable that supports an Asymmetric Link.	RO	0
		23	Cable CLx Support (CSC) An Adapter shall set this bit to 1b if its USB4 Port is connected to a Cable that supports the Low Power (CLx) states.	RO	0
		24	AsymmetricTransitionInProgress (TIP) A USB4 Port sets this bit to 1b when it sends UNBOND Ordered Sets. A USB4 Port sets this bit to 0b after finishing the transition.	RO	0
		31:25	Reserved	Rsvd	0
19	PORT_CS_19	0	Downstream Port Reset (DPR) A Connection Manager uses this bit to reset a Downstream Facing Port. A Downstream Facing Port shall initiate a Downstream Port Reset when this bit is set to 1b. Setting this bit to 0b shall transition the Adapters in the Downstream Facing Port out of the CLd state. An Adapter in an Upstream Facing Port shall ignore this bit and may hardwire the bit to 0b.	R/W	0b
		1	Request RS-FEC Gen 2 (RS2) A Connection Manager uses this bit to request enabling of RS-FEC encoding at Gen 2 speeds. If a Link is Active, the Link shall be re-initialized before RS-FEC can be enabled. If this bit is set to 0b, the USB4 Port shall disable RS-FEC at Gen 2 speeds during the next Lane Initialization. If this bit is set to 1b, then the Link Partner response determines whether RS-FEC is enabled at Gen 2 speeds.	R/W	1b
		2	Request RS-FEC Gen 3 (RS3) A Connection Manager uses this bit to request enabling of RS-FEC encoding at Gen 3 speeds. If a Link is Active, the Link shall be re-initialized before RS-FEC can be enabled. If this bit is set to 0b, the USB4 Port shall disable RS-FEC at Gen 3 speeds during the next Lane Initialization. If this bit is set to 1b, then the Link Partner response determines whether RS-FEC is enabled at Gen 3 speeds.	R/W	1b
		3	USB4 Port is Configured (PC) A Connection Manager sets this bit as follows: 1b – Router connected to the USB4 Port is configured and therefore supports sleep state 0b – Router connected to the USB4 Port is not configured and therefore does not support sleep	R/W	0b
		4	USB4 Port is Inter-Domain (PID) A Connection Manager sets this bit as follows: 1b – USB4 Port is part of an Inter-Domain Link 0b – USB4 Port is not part of an Inter-Domain Link	R/W	0b
		7:5	Reserved	Rsvd	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		15:8	Bundle Weight This field is set by the Connection Manager as the total weight for all the enabled Gen T Paths that goes through this USB4 Port. This field only applies to a USB4 Port in a Host Router that has the <i>Gen T Bundle Weight Mode</i> bit set to 1b.	R/W	0
		16	Enable Wake on Connect A Connection Manager uses this bit to configure whether a connection on the USB Type-C connector attached to this USB4 Port causes the Router to exit the sleep state. 1b – Connection causes exit from sleep 0b – Connection does not cause exit from sleep	R/W	0
		17	Enable Wake on Disconnect A Connection Manager uses this bit to configure whether a disconnect on the USB Type-C connector attached to this USB4 Port causes the Router to exit sleep state. 1b – Disconnect causes exit from sleep 0b – Disconnect does not cause exit from sleep	R/W	0
		18	Enable Wake on USB4 Wake A Connection Manager uses this bit to configure whether a USB4 Wake causes the Router to exit the sleep state. 1b – USB4 Wake causes exit from sleep 0b – USB4 Wake does not cause exit from sleep	R/W	1
		19	Enable Wake on Inter-Domain A Connection Manager uses this bit to configure whether an Inter-Domain Wake causes the Router to exit the sleep state. 1b – Inter-Domain Wake causes exit from sleep 0b – Inter-Domain Wake does not cause exit from sleep	R/W	0
		20:23	Reserved	Rsvd	0
		24	StartAsymmetricFlow A Connection Manager uses this field to initiate a transition either from Symmetric Link to Asymmetric Link or a transition from Asymmetric Link to a Symmetric Link. A USB4 Port sets this bit to 0b when Asymmetric Transition is initiated.	R/W SC	0
		29:25	Reserved	Rsvd	0
		30	Initiate Gen 4 Link Recovery (ILR) A Connection Manager uses this bit to trigger Link Recovery for Gen 4 Links. This bit is self-cleared. This bit is not applicable for Gen 2 and Gen 3 Links.	W/Clr	0
		31	Enable Gen 4 Link Recovery (ELR) A Connection Manager uses this bit to enable Link Recovery for Gen 4 Links. This bit is not applicable for Gen 2 and Gen 3 Links.	R/W	0

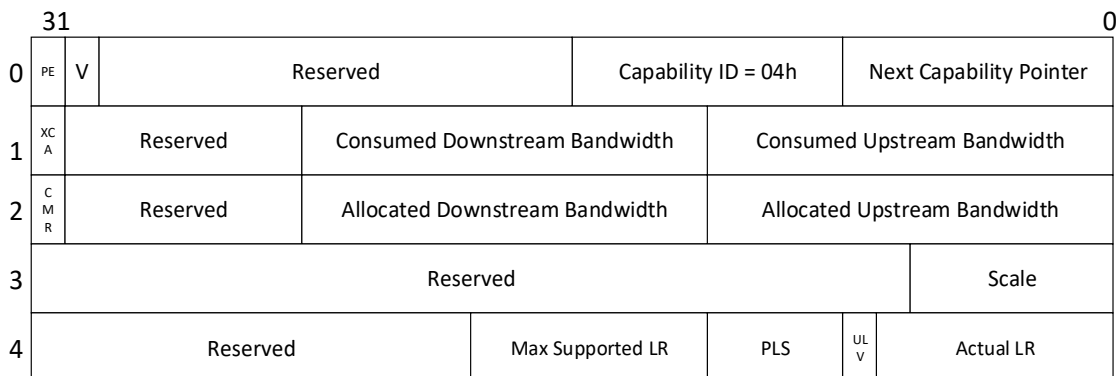
**CONNECTION MANAGER NOTE**

When writing to a USB4 Port Capability, a Connection Manager shall abide by the following rules:

- The Target Link Speed field in the Lane Adapters of a USB4 Port shall be set to the same value.
- The Target Link Width field in the Lane Adapters of a USB4 Port shall be set to the same value.
- A Connection Manager shall not write to any of DW1 through DW17 (inclusive) of the USB4 Port Capability (PORT_CS_1) when the Pending bit is 1b.
- A Connection Manager shall not set the Length field to a value greater than 64.
- When the Target field is 010b, the Connection Manager shall set the Re-timer Index field to the index of the target Re-timer. When the Target field is not 010b, the Connection Manager shall set the Re-timer Index field to 0.
- The Connection Manager shall not write USB4 Port Capability Register 19 while StartAsymmetricFlow is 1b.

8.2.2.5 USB3 Adapter Configuration Capabilities**8.2.2.5.1 USB3 Gen X Configuration Capability**

A USB3 Gen X Adapter Configuration Capability shall have the structure depicted in Figure 8-11 and shall have the fields defined in Table 8-14.

Figure 8-11. Structure of USB3 Gen X Adapter Configuration Capability**Table 8-14. USB3 Gen X Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_USB3_GX_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. An Adapter shall set this field to 00h if the Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 04h indicating this is a Protocol Adapter Configuration Capability.	RO	04h
		29:16	Reserved	Rsvd	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		30	Valid (V) A Connection Manager sets this bit to 1b when the value of the <i>Path Enable</i> bit is valid. When this bit is set to 0b, the value of the <i>Path Enable</i> bit is not valid.	R/W	0b
		31	Path Enable (PE) A Connection Manager uses this bit to enable transmission and reception of Tunneled Packets. When set to 1b, the Adapter may send and receive Tunneled Packets. When set to 0b, the Adapter shall not send or receive Tunneled Packets.	R/W	0b
1	ADP_USB3_GX_CS_1	11:0	Consumed Upstream Bandwidth This field shall contain the amount of upstream bandwidth consumed for periodic USB3 traffic. The upstream bandwidth is given as the maximal number of bytes consumed within each USB3 frame of 1 ms in multiple of $(512 * 2^{\text{Scale}})$ bytes. A Router shall not update this field when the <i>Host Controller Ack</i> bit is set to 1b. This field shall be hardwired to 0 for a Device Router.	RO	0
		23:12	Consumed Downstream Bandwidth This field shall contain the amount of downstream bandwidth consumed for periodic USB3 traffic. The downstream bandwidth is given as the maximal the number of bytes consumed within each USB3 frame of 1 ms in multiple of $(512 * 2^{\text{Scale}})$ bytes. A Router shall not update this field when the <i>Host Controller Ack</i> bit is set to 1b. This field shall be hardwired to 0 for a Device Router.	RO	0
		30:24	Reserved	Rsvd	0
		31	Host Controller Ack (HCA) A Router shall set this bit to 1b when a Connection Manager is allowed to read the <i>Consumed Upstream Bandwidth</i> and <i>Consumed Downstream Bandwidth</i> fields or update the <i>Allocated Upstream Bandwidth</i> or <i>Allocated Downstream Bandwidth</i> fields. Otherwise, this bit shall be set to 0b. This bit shall be hardwired to 0b for a Device Router.	RO	0b
2	ADP_USB3_GX_CS_2	11:0	Allocated Upstream Bandwidth This field shall contain the amount of upstream bandwidth allocated for periodic USB3 traffic. The upstream bandwidth is given as the maximal number of available bytes within each USB3 frame of 1 ms in multiple of $512 * 2^{\text{Scale}}$ bytes. This field shall be hardwired to 0 for a Device Router. A Connection Manager shall not set this field to a higher bandwidth than the Maximum Supported Link Rate	R/W	0
		23:12	Allocated Downstream Bandwidth This field shall contain the amount of downstream bandwidth allocated for periodic USB3 traffic. The downstream bandwidth is given as the maximal number of available bytes within each USB3 frame of 1 ms in multiple of $512 * 2^{\text{Scale}}$ bytes. This field shall be hardwired to 0 for a Device Router. A Connection Manager shall not set this field to a higher bandwidth than the Maximum Supported Link Rate	R/W	0

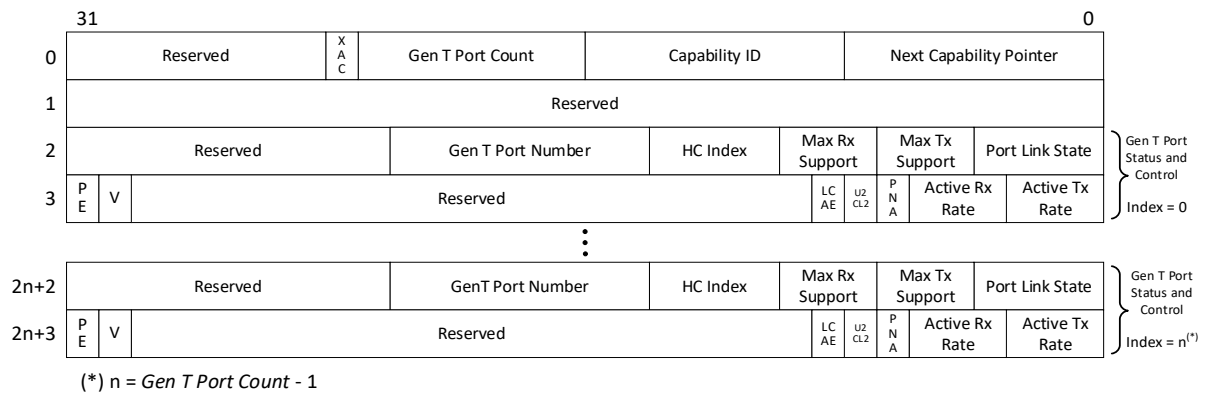
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DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		30:24	Reserved	Rsvd	0
		31	Connection Manager Request (CMR) The Connection Manager sets this bit to 1b to request permission to read the <i>Consumed Upstream Bandwidth</i> and <i>Consumed Downstream Bandwidth</i> fields or update the <i>Allocated Upstream Bandwidth</i> or <i>Allocated Downstream Bandwidth</i> fields. The Connection Manager sets this bit to 0b after it has completed the read/update. The Connection Manager set this bit to 0 when the Internal USB3 Host Controller is not enabled in the Router.	R/W	0b
3	ADP_USB3_GX_CS_3	5:0	Scale A Connection Manager uses this field to set the granularity of bandwidth negotiated in the <i>Consumed Upstream Bandwidth</i> field, the <i>Consumed Downstream Bandwidth</i> field, the <i>Allocated Upstream Bandwidth</i> field, and the <i>Allocated Downstream Bandwidth</i> field. A Device Router shall hardwire this field to 0. A Connection Manager shall set this field to 0 if the Maximum Supported Link Rate equals to 0.	R/W	0
		31:6	Reserved	Rsvd	0
4	ADP_USB3_GX_CS_4	6:0	Actual Link Rate 0h: 10 Gbps (Gen 2 – Single-Lane) 1h: 20 Gbps (Gen 2 – Aggregated) 7Fh – 2h: Reserved	RO	0
		7	USB3 Link Valid (ULV) 0: <i>Actual Link Rate</i> field is not valid 1: <i>Actual Link Rate</i> field is valid	RO	0
		11:8	Port Link State (PLS) This field shall indicate the port link state of the USB3 Gen X Port connected to the USB3 Gen X Adapter Layer: 0h: U0 state 1h: Reserved 2h: U2 state 3h: U3 state 4h: Disabled state 5h: RxDetect state 6h: Inactive state 7h: Polling state 8h: Recovery state 9h: Hot Reset state Ah – Eh: Reserved Fh: Resume state	RO	Vendor Defined
		18:12	Maximum Supported Link Rate 0h: 10 Gbps (Gen 2 – Single-Lane) 1h: 20 Gbps (Gen 2 – Aggregated) 7Fh – 2h: Reserved	RO	Vendor Defined
		31:19	Reserved	Rsvd	0

8.2.2.5.2 USB3 Gen T Configuration Capability

A USB3 Gen T Adapter Configuration Capability consists of two DWs of Adapter status and control fields followed by a series of Gen T Port entries. Each Gen T Port entry contains two DW. A USB3 Gen T Adapter Configuration Capability contains one Gen T Port entry for each Gen T Port that interfaces to the Adapter.

A USB3 Gen T Adapter Configuration Capability shall have the structure depicted in Figure 8-12 and shall have the fields defined in Table 8-15. The Gen T Port entries are addressed using the 6 Gen T Index (index) as shown in Figure 8-12.

Figure 8-12. Structure of USB3 Gen T Adapter Configuration Capability**Table 8-15. USB3 Gen T Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_USB3_GT_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. An Adapter shall set this field to 00h if the Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 04h indicating this is a Protocol Adapter Configuration Capability.	RO	04h
		22:16	Gen T Port Count Number of Gen T Ports supported by the Adapter. <i>Note: The size of the USB3 Gen T Adapter Configuration Capability in DW is (Gen T Port Count) x 2 + 2.</i>	RO	Vendor Defined
		23	Gen X Adapter Coupled (XAC) This bit shall be set to 1b if the Gen T Ports of this Adapter and a Gen X Port are associated with the same USB3 device controller. Otherwise, this bit shall be set to 0b. For example, a USB3 device controller for an embedded storage that needs either Gen T or Gen X operation, but not both at the same time, would set this bit to 1b. If this field is set to 1b, a Connection Manager shall not enable Gen X and Gen T operation in the Device Router at the same time. This field only applies to Upstream USB3 Gen T Adapters.	RO	Upstream Adapter: Vendor Defined Else: 0

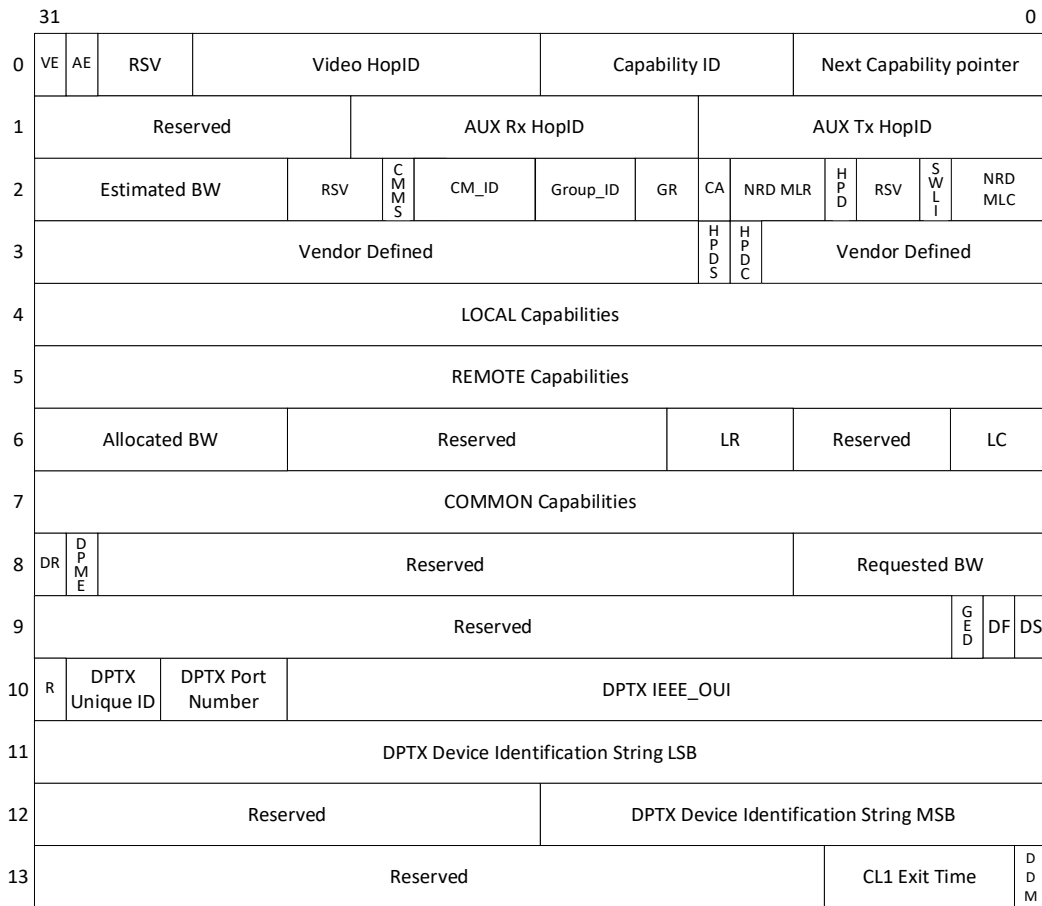
DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		31:24	Reserved	Rsvd	0
1	ADP_USB3_GT_CS_1	31:0	Reserved	Rsvd	0
2+2n	ADP_USB3_GT_PORT_CS_0	3:0	Port Link State (PLS) This field shall indicate the port link state of the USB3 Gen T Port connected to the USB3 Gen T Adapter 0h: U0 state 1h: Reserved 2h: U2 state 3h: U3.DEFAULT 4h: Disabled state 5h: DISCONNECT.ENTRY 6h: Error State 7h: DISCONNECT.EXIT 8h: Reserved 9h: Port Reset state Ah-Eh: Reserved Fh: DFP Only: U3.RECEIVED_U3Resume	RO	5
		6:4	Maximum Tx Supported Link Rate 0-1h: Reserved 2h: 40Gbps 3h: 80Gbps 4h: 120Gbps 5-7h: Reserved	RO	Vendor Defined
		9:7	Maximum Rx Supported Link Rate 0-1h: Reserved 2h: 40Gbps 3h: 80Gbps 4h: 120Gbps 5-7h: Reserved	RO	Vendor Defined
		13:10	USB3 Host Controller Index This field contains the hardware-defined index of the USB3 Host Controller that the USB3 Gen T Port is associated with. This field only applies to Downstream USB3 Gen T Adapters	RO	Vendor Defined
		21:14	Gen T Port Number This field contains the Port Number of the Gen T port associated with this Adapter. The Gen T Port Number is assigned by the USB3 Host Controller. This field only applies to Downstream USB3 Gen T Adapters.	RO	Vendor Defined
		31:22	Reserved	Rsvd	0
3+2n	ADP_USB3_GT_PORT_CS_1	2:0	Active Tx Link Rate This field indicates the current Tx speed: 0h: 10Gbps 1h: 20Gbps 2h: 40Gbps 3h: 80Gbps 4h: 120Gbps 5-7h: Reserved This field is set by the Connection Manager based on the capabilities of the Gen T Link Partner and any intermediate Routers and cables.	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		5:3	Active Rx Link Rate This field indicates the current Rx speed: 0h: 10Gbps 1h: 20Gbps 2h: 40Gbps 3h: 80Gbps 4h: 120Gbps 5-7h: Reserved This field is set by the Connection Manager based on the capabilities of the Gen T Link Partner and any intermediate Routers and cables.	R/W	0
		6	Gen T Port Not Available (PNA) A Connection Manager sets this bit to 1b when there are no Gen T Ports available in the Host Gen T Adapter. This field only applies to the Upstream USB3 Gen T Adapter in a Device Router.	R/W	0
		7	U2CL2 Enable (U2CL2) A Connection Manager sets this bit to 1b to indicate that, when the Gen T Port enters U2, the objection for CL2 for that Gen T Port may be dropped. This field may be set to 1b after Path was enabled.	R/W	0
		8	Link Commands Aggregation Enable (LCAE) This bit indicates whether the Link Commands Aggregation feature is enabled: 0b: Disabled 1b: Enabled A Connection Manager shall set this bit to the same value in the USB3 Gen T Ports on each end of a Path. A Connection Manager shall set this bit to the desired value before the Path is enabled.	R/W	0
		29:9	Reserved	Rsvd	0
		30	Valid (V) A Connection Manager sets this bit to 1b when the value of the <i>Path Enable</i> bit is valid. When this bit is set to 0b, the value of the <i>Path Enable</i> bit is not valid.	R/W	0b
		31	Path Enable (PE) A Connection Manager uses this bit to enable transmission and reception of Tunneled Packets. When set to 1b, the Adapter may send and receive Tunneled Packets. When set to 0b, the Adapter shall not send Tunneled Packets and discard any received Tunneled Packets. When the <i>Valid</i> bit is set to 0b, a Router ignores a change in the value of this field.	R/W	0b

8.2.2.6 DP Adapter Configuration Capabilities

8.2.2.6.1 DP IN Adapter Configuration Capability

A DP IN Adapter Configuration Capability shall have the structure depicted in Figure 8-13 and shall have the fields defined in Table 8-16.

Figure 8-13. Structure of DP IN Adapter Configuration Capability**Table 8-16. DP IN Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_DP_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. An Adapter shall set this field to 00h if the Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 04h indicating this is a Protocol Adapter Configuration Capability.	RO	04h
		22:16	Video HopID An Adapter shall set this field to 9.	RO	9
		29:23	Reserved	Rsvd	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		30	AUX Enable (AE) A Connection Manager uses this bit to control when the DP IN Adapter can send and receive packets on the AUX Path. When set to 1, the Adapter may send and receive packets on the AUX Path. When set to 0, the Adapter shall not send or receive packets on the AUX Path and shall set Adapter Configuration Space to its default values as defined in Section 10.2.2.	R/W	0
		31	Video Enable (VE) A Connection Manager uses this bit to control when the DP IN Adapter can send and receive packets on the Video Path. When set to 1, the Adapter may send packets on the Video Path. When set to 0, the Adapter shall not send packets on the Video Path and shall set Adapter Configuration Space to its default values as defined in Section 10.2.2.	R/W	0
1	ADP_DP_CS_1	6:0	AUX Tx HopID An Adapter shall set this field to 8.	RO	8
		10:7	Reserved	Rsvd	0
		17:11	AUX Rx HopID An Adapter shall set this field to 8.	RO	8
		31:18	Reserved	Rsvd	0
2	ADP_DP_CS_2	2:0	NRD Max Lane Count (NRD MLC) 0: 1 lane 1: 2 lanes 2: 4 lanes 3 – 7: Reserved The Non-Reduced Max Lane Count is set by a Connection Manager to reflect the highest common Max Lane Count between the two DP Adapters, regardless of bandwidth availability.	R/W	0
		3	SW Link Init (SWLI) A Connection Manager uses this bit to initiate Link-Initialization. When this bit transitions from 0 to 1, the Adapter shall initiate Link-Init as described in Section 10.4.13.	R/W	0
		5:4	Reserved	RsvdZ	0
		6	HPD Status This field shall contain the HPD value received from the DP OUT Adapter.	RO	0
		9:7	NRD Max Link Rate (NRD MLR) 0h: 1.62 Gbps/lane 1h: 2.7 Gbps/lane 2h: 5.4 Gbps/lane 3h: 8.1 Gbps/lane 4h – Fh: Reserved The Non-Reduced Max Link Rate is set by a Connection Manager to reflect the highest common Max Link Rate between the two DP Adapters, regardless of bandwidth availability.	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		10	CM Ack (CA) A Connection Manager sets this field to 1b to indicate that it completed the bandwidth allocation process. A Connection Manager sets this bit to 0b after the DP IN Adapter sets <i>DPTX Req</i> field to 0b.	R/W	0
		12:11	Granularity (GR) A Connection Manager sets this field to indicate the bandwidth granularity for the <i>Requested BW</i> , <i>Allocated BW</i> and <i>Estimated BW</i> : 0: 0.25 1: 0.5 2: 1.0 3: Reserved The units are in Gbps.	R/W	0
		15:13	Group_ID A Connection Manager uses this field to indicate the group this Path is associated with: 0h – The Path is not associated to any group. 1-7h – The group number the Path is associated with.	R/W	0
		19:16	CM_ID A Connection Manager uses this field to indicate its own index, in case there are multiple CMs in the Host system.	R/W	0
		20	CM BW Allocation Mode Support (CMMS) This bit indicates whether the Connection Manager supports DP BW Allocation Mode: 0: Not supported 1: Supported A Connection Manager shall set this bit to the desired value before a Path is enabled.	R/W	0
		23:21	Reserved	RsvdZ	0
		31:24	Estimated BW A Connection Manager uses this field to indicate the estimated available bandwidth for the DP IN Adapter.	R/W	0
3	ADP_DP_CS_3	8:0	Vendor Defined	VD	Vendor Defined
		9	HPD Output Clear (HPDC) A Connection Manager uses this field to clear the HPD output. When this bit is 1b, an Adapter shall drive HPD low to cause a single event of HPD output clear.	R/W	0
		10	HPD Output Set (HPDS) A Connection Manager uses this field to set the HPD output. When this bit is 1b, a Port shall drive HPD high to cause a single event of HPD output set.	R/W	0
		31:11	Vendor Defined	VD	Vendor Defined

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
DP_LOCAL_CAP Register reflects the static local capabilities of the DP IN Adapter per connection. For example, Connecting a DP IN Adapter as DP ALT-Mode in Multi-Function operation limits the <i>Maximal Lane Count</i> field in this register.					
4	DP_LOCAL_CAP	3:0	Protocol Adapter Version This field shall identify which version of the USB4 Specification the Adapter supports. 0h – 2h: Reserved 3h: Reserved for TBT3 4h: Version 1.0 5h: Version 2.0 6h – Fh: Reserved	RO	5h
		7:4	Maximal DPCD Rev 0h: DPCD r1.1 1h: DPCD r1.2 2h: DPCD r1.3 3h: DPCD r1.4a 4h – Fh: Reserved	RO	3
		11:8	8b10b Maximal Link Rate 0h: 1.62 Gbps/lane 1h: 2.7 Gbps/lane 2h: 5.4 Gbps/lane 3h: 8.1 Gbps/lane 4h – Fh: Reserved	RO	Vendor Defined
		14:12	Maximal Lane Count 0: 1 lane 1: 2 lanes 2: 4 lanes 3 – 7: Reserved If the DP IN Adapter was connected as part of MFDP, this field shall not indicate 4 lanes.	RO	Vendor Defined
		15	8b10b MST Capability 0: Not supported 1: Supported	RO	Vendor Defined
		16	Panel Replay Tunneling Optimization Support 0: Not supported 1: Supported	RO	Vendor Defined
		17	128b/132b Link Layer & 10Gbps/Lane Support Link rate associated with UHBR10. 0: Not supported 1: Supported A DP Adapter that supports the 128b/132b Link Layer shall support this link rate.	RO	Vendor Defined
		18	20Gbps/Lane Support Link rate associated with UHBR20. 0: Not supported 1: Supported Highest link rate available. A DP Adapter may optionally support this link rate.	RO	Vendor Defined

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		19	13.5Gbps/Lane Support Link rate associated with UHBR13.5 0: Not supported 1: Supported A DP Adapter may optionally support this link rate. <i>Note: Support for 13.5Gbps/lane is optional, even for a DP Adapter that supports 20Gbps/lane.</i>	RO	Vendor Defined
		20	ALPM Support 0: Not supported 1: Supported	RO	Vendor Defined
		21	Reserved	Rsvd	0
		22	8b10b TPS3 Capability 0: Not supported 1: Supported	RO	Vendor Defined
		23	Reserved	Rsvd	1
		24	8b10b TPS4 Capability 0: Not supported 1: Supported	RO	Vendor Defined
		25	8b10b FEC Not Supported 0: Supported 1: Not supported A DP IN Adapter shall set this bit to 0b if it sets the <i>DSC Not Supported</i> bit to 0b or it sets the <i>Panel Replay Tunneling Optimization Support</i> bit to 1b.	RO	Vendor Defined
		26	Secondary Split Capability 0: Not Supported 1: Supported A DP IN Adapter shall set this bit to 1b unless it is integrated with a DPTX which doesn't support SDP Split.	RO	Vendor Defined
		27	LTTPR Not Supported 0: Supported 1: Not supported A DP IN Adapter shall set this bit to 0b.	RO	0
		28	DP IN BW Allocation Mode Support 0: Not supported 1: Supported A DP IN Adapter shall set this bit to 1b.	RO	1
		29	DSC Not Supported 0: Supported 1: Not supported A DP IN Adapter shall set this bit to 0b if it sets the <i>128b/132b Link Layer & 10Gbps/Lane Support</i> bit to 1b.	RO	Vendor Defined
		31:30	Reserved	Rsvd	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
The DP_REMOTE_CAP register reflects the local capabilities of the paired DP OUT Adapter. The Values in this register are set by the Connection Manager during Path Configuration. A DP IN Adapter shall reset the fields in this register to their default values when the DP OUT Adapter is unpaired.					
5	DP_REMOTE_CAP	3:0	Protocol Adapter Version Identifies what version of the USB4 Specification is supported by the paired DP OUT Adapter 0h – 2h: Reserved 3h: Reserved for TBT3 4h: Version 1.0 5h: Version 2.0 6h – Fh: Reserved	R/W	0
		7:4	Maximal DPCD Rev 0h: DPCD r1.1 1h: DPCD r1.2 2h: DPCD r1.3 3h: DPCD r1.4a 4h – Fh: Reserved	R/W	0
		11:8	8b10b Maximal Link Rate 0h: 1.62 Gbps/lane 1h: 2.7 Gbps/lane 2h: 5.4 Gbps/lane 3h: 8.1 Gbps/lane 4h – Fh: Reserved	R/W	0
		14:12	Maximal Lane Count 0: 1 lane 1: 2 lanes 2: 4 lanes 3 – 7: Reserved	R/W	0
		15	8b10b MST Capability 0: Not supported 1: Supported	R/W	0
		16	Panel Replay Tunneling Optimization Support 0: Not supported 1: Supported	R/W	0
		17	128b/132b Link Layer & 10Gbps/Lane Support Link rate associated with UHBR10. 0: Not supported 1: Supported	R/W	0
		18	20Gbps/Lane Support Link rate associated with UHBR20. 0: Not supported 1: Supported	R/W	0
		19	13.5Gbps/Lane Support Link rate associated with UHBR13.5. 0: Not supported 1: Supported	R/W	0
		20	ALPM Support 0: Not supported 1: Supported	R/W	0
		21	Reserved	RsvdZ	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		22	8b10b TPS3 Capability 0: Not supported 1: Supported	R/W	0
		23	Vendor Defined	VD	Vendor Defined
		24	8b10b TPS4 Capability 0: Not supported 1: Supported	R/W	0
		25	8b10b FEC Not Supported 0: Supported 1: Not supported	R/W	0
		26	Secondary Split Capability 0: Not supported 1: Supported	R/W	0
		27	LTTPR Not Supported 0: Supported 1: Not Supported	R/W	0
		28	Reserved	RsvdZ	0
		29	DSC Not Supported 0: Supported 1: Not supported	R/W	0
		31:30	Reserved	RsvdZ	0
The <i>Lane Count</i> and <i>Link Rate</i> fields are only valid after the DP Link is established.					
6	DP_STATUS	2:0	Lane Count 1: 1 lane 2: 2 lanes 4: 4 lanes 0; 3; 5 – 7: Reserved	RO	0
		7:3	Reserved	Rsvd	0
		11:8	Link Rate 0h: 1.62 Gbps/lane 1h: 2.7 Gbps/lane 2h: 5.4 Gbps/lane 3h: 8.1 Gbps/lane 4h: 10.0 Gbps/lane 5h: 20.0 Gbps/lane 6h: 13.5 Gbps/lane 7h – Fh: Reserved	RO	0
		16:12	Reserved	Rsvd	0
		23:17	Reserved	RsvdZ	0
		31:24	Allocated BW A Connection Manager uses this field to indicate the allocated bandwidth for the DP IN Adapter.	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
DP_COMMON_CAP fields reflects the lowest common capability between DP_LOCAL_CAP fields and DP_REMOTE_CAP fields. The DP_COMMON_CAP fields shall be updated any time the DP_REMOTE_CAP fields are updated.					
7	DP_COMMON_CAP	3:0	Protocol Adapter Version This field shall identify the highest common version of the USB4 Specification that is supported by both the DP IN Adapter and the DP OUT Adapter. 0h – 2h: Reserved 3h: Reserved for TBT3 4h: Version 1.0 5h: Version 2.0 6h – Fh: Reserved	RO	0
		7:4	Maximal DPCD Rev 0h: DPCD r1.1 1h: DPCD r1.2 2h: DPCD r1.3 3h: DPCD r1.4a 4h – Fh: Reserved	RO	0
		11:8	8b10b Maximal Link Rate 0h: 1.62 Gbps/lane 1h: 2.7 Gbps/lane 2h: 5.4 Gbps/lane 3h: 8.1 Gbps/lane 4h – Fh: Reserved	RO	0
		14:12	Maximal Lane Count 0: 1 lane 1: 2 lanes 2: 4 lanes 3 – 7: Reserved	RO	0
		15	8b10b MST Capability 0: Not supported 1: Supported	RO	0
		16	Panel Replay Tunneling Optimization Support 0: Not supported 1: Supported	RO	0
		17	128b/132b Link Layer & 10Gbps/Lane Support Link rate associated with UHBR10. 0: Not supported 1: Supported	RO	0
		18	20Gbps/Lane Support Link rate associated with UHBR20. 0: Not supported 1: Supported	RO	0
		19	13.5Gbps/Lane Support Link rate associated with UHBR13.5. 0: Not supported 1: Supported	RO	0
		20	ALPM Support 0: Not supported 1: Supported	RO	0
		21	Reserved	Rsvd	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		22	8b10b TPS3 Capability 0: Not supported 1: Supported	RO	0
		23	Vendor Defined	VD	0
		24	8b10b TPS4 Capability 0: Not supported 1: Supported	RO	0
		25	8b10b FEC Not Supported 0: Supported 1: Not supported	RO	0
		26	Secondary Split Capability 0: Not supported 1: Supported	RO	0
		27	LTTPR Not Supported 0: Supported 1: Not Supported	RO	0
		28	Reserved	Rsvd	0
		29	DSC Not Supported 0: Supported 1: Not supported	RO	0
		30	Reserved	Rsvd	0
		31	DPRX Capabilities Read Done 0: Not Done 1: Done A DP Adapter shall set the value of this field after DPCD addresses 00001h and 00002h are read. See Section 10.4.6.2.	RO	0
8	ADP_DP_CS_8	7:0	Requested BW A DP IN Adapter uses this field to reflect the requested bandwidth by the DPTX to the Connection Manager.	RO	0
		29:8	Reserved	Rsvd	0
		30	DPTX BW Allocation Mode Enable (DPME) 0: Disabled (default) 1: Enabled	RO	0
		31	DPTX Req(DR) A DP IN Adapter sets this field to 1b when DPTX writes to the REQUESTED_BW register. A DP IN Adapter sets this field to 0b after the Connection Manager sets the <i>CM Ack</i> bit to 1b.	RO	0
9	ADP_DP_CS_9	0	Discovery Success (DS) A DP IN Adapter sets this bit to 1b if the DPTX Discovery process ends successfully, as defined in Section 10.8.2. Otherwise, this bit shall be set to 0b.	RO	0
		1	Discovery Failure (DF) A DP IN Adapter sets this bit to 1b if the DPTX Discovery process ends unsuccessfully, as defined in Section 10.8.2. Otherwise, this bit shall be set to 0b.	RO	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		2	Grant Extended Delay (GED) A DP IN Adapter sets this bit according to the value set by the DPTX in the DPCD <i>USB4 CL1 Granted through ALPM</i> field (Address E0032h, bit 0).	RO	0
		31:3	Reserved	Rsvd	0
10	ADP_DP_CS_10	23:0	DPTX IEEE_OUI A DP IN Adapter sets this field to the value written by the DPTX to DPCD registers 00300h-00302h.	RO	0
		27:24	DPTX Port Number A DP IN Adapter sets this field to the value written by the DPTX to DPCD <i>DPTX_DISCOVERY_CONTROL.DPTX_Port_number</i> (E0033h, bits[3:0]).	RO	0
		30:28	DPTX Unique_ID A DP IN Adapter sets this field to the value written by the DPTX to DPCD <i>DPTX_DISCOVERY_CONTROL.DPTX_UNIQUE_ID</i> (E0033h, bits[6:4]).	RO	0
		31	Reserved	Rsvd	0
11	ADP_DP_CS_11	31:0	DPTX Device Identification String LSB A DP IN Adapter sets this field to the value written by the DPTX to DPCD registers 00303h-00306h.	RO	0
12	ADP_DP_CS_12	15:0	DPTX Device Identification String MSB A DP IN Adapter sets this field to the value written by the DPTX to DPCD registers 00307h-00308h.	RO	0
		31:16	Reserved	Rsvd	0
13	ADP_DP_CS_13	0	DPTX Discovery Mode (DDM) This field causes a DP IN Adapter to enter or exit the DPTX Discovery state, as defined in Section 10.8.2. 0: Exit DPTX Discovery state 1: Enter DPTX Discovery state A Connection Manager shall not set this bit to 1b if the <i>DPTX Discovery Support</i> bit is 0b.	R/W	0
		6:1	CL1 Exit Time This field indicates the time it takes the USB4 Links, that the DP Path traverses through, to exit CL1state. A DP IN Adapter shall reflect the same written value in this field to the DPCD <i>USB4_CL1Exit_Time</i> field (Address E002Ah, bits [5:0]). The time in this field is specified in units of 10 μ s. A value of 0h indicates that CL1 is not enabled on any of the USB4 Link that the DP Path traverses through. A Connection Manager shall set this field during Path Setup.	R/W	0
		31:7	Reserved	Rsvd	0

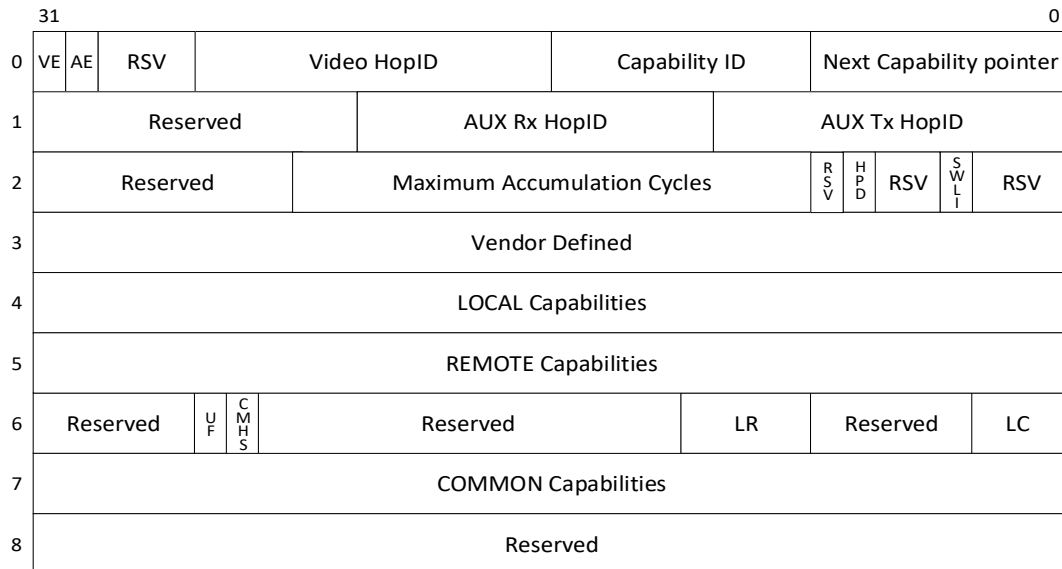


CONNECTION MANAGER NOTE

A Connection Manager shall set the values in the DP IN Adapter Configuration Capability before it sets the Video Enable bit or the Aux Enable bit in the Adapter to 1b. However, the Connection Manager may set the Bandwidth Management fields (i.e., CM Ack, Granularity, Estimated BW, and Allocated BW) at any time after the DP resource is allocated via an Allocate DP Resource Router Operation.

8.2.2.6.2 DP OUT Adapter Configuration Capability

A DP OUT Adapter Configuration Capability shall have the structure depicted in Figure 8-14 and shall have the fields defined in Table 8-17.

Figure 8-14. Structure of DP OUT Adapter Configuration Capability**Table 8-17. DP OUT Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_DP_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. An Adapter shall set this field to 00h if the Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 04h indicating this is a Protocol Adapter Configuration Capability.	RO	04h
		22:16	Video HopID An Adapter shall set this bit to 9.	RO	9
		29:23	Reserved	Rsvd	0
		30	AUX Enable (AE) A Connection Manager uses this bit to control when the DP OUT Adapter can send and receive packets on the AUX Path. When set to 1, the Adapter may send and receive packets on the AUX Path. When set to 0, the Adapter shall not send or receive packets on the AUX Path and shall set Adapter Configuration Space to its default values as defined in Section 10.2.2.	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		31	Video Enable (VE) A Connection Manager uses this bit to control when the DP OUT Adapter can receive packets on the Video Path. When set to 1, the Adapter may receive packets on the Video Path. When set to 0, the Adapter shall not receive packets on the Video Path and shall set Adapter Configuration Space to its default values as defined in Section 10.2.2.	R/W	0
1	ADP_DP_CS_1	6:0	AUX Tx HopID An Adapter shall set this field to 8.	RO	8
		10:7	Reserved	Rsvd	0
		17:11	AUX Rx HopID An Adapter shall set this field to 8.	RO	8
		31:18	Reserved	Rsvd	0
2	ADP_DP_CS_2	2:0	Reserved	Rsvd	0
		3	SW Link Init (SWLI) A Connection Manager uses this bit to initiate Link-Initialization. When this bit transitions from 0 to 1, the Adapter shall initiate Link-Init as described in Section 10.4.13.	R/W	0
		5:4	Reserved	Rsvd	0
		6	HPD Status This field shall contain the HPD value sent to DP IN Adapter.	RO	0
		7	Reserved	Rsvd	0
		23:8	Maximum Accumulation Cycles The number of DP Link clock cycles that a DP OUT Adapter accumulates Main-Link Data when operating at the highest supported DP Link Rate.	RO	Vendor Defined
		31:24	Reserved	Rsvd	0
3	ADP_DP_CS_3	31:0	Vendor Defined	VD	Vendor Defined
DP_LOCAL_CAP register reflects the static local capabilities of the DP OUT Adapter per connection. For example, Connecting a DP OUT Adapter as DP ALT-Mode in Multi-Function operation limits the Maximal Lane Count in this register.					
4	DP_LOCAL_CAP	3:0	Protocol Adapter Version This field shall identify which version of the USB4 Specification the DP OUT Adapter supports 0h – 2h: Reserved 3h: Reserved for TBT3 4h: Version 1.0 5h: Version 2.0 6h – Fh: Reserved	RO	5h
		7:4	Maximal DPCD Rev 0h: DPCD r1.1 1h: DPCD r1.2 2h: DPCD r1.3 3h: DPCD r1.4a 4h – Fh: Reserved	RO	3

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
4	DP_LOCAL_CAP	11:8	8b10b Maximal Link Rate 0h: 1.62 Gbps/lane 1h: 2.7 Gbps/lane 2h: 5.4 Gbps/lane 3h: 8.1 Gbps/lane 4h – Fh: Reserved	RO	Vendor Defined
		14:12	Maximal Lane Count 0: 1 lane 1: 2 lanes 2: 4 lanes 3 – 7: Reserved If the DP OUT Adapter was connected as part of MFDP, this field shall not indicate 4 lanes.	RO	Vendor Defined
		15	8b10b MST Capability 0: Not supported 1: Supported	RO	Vendor Defined
		16	Panel Replay Tunneling Optimization Support 0: Not supported 1: Supported	RO	Vendor Defined
		17	128b/132b Link Layer & 10Gbps/Lane Support Link rate associated with UHBR10. 0: Not supported 1: Supported A DP Adapter that supports a 128b/132b Link Layer shall support this link rate.	RO	Vendor Defined
		18	20Gbps/Lane Support Link rate associated with UHBR20. 0: Not supported 1: Supported Highest link rate available. A DP Adapter may optionally support this link rate.	RO	Vendor Defined
		19	13.5Gbps/Lane Support Link rate associated with UHBR13.5. 0: Not supported 1: Supported A DP Adapter may optionally support this link rate. <i>Note: Support for 13.5Gbps/lane is optional, even for a DP Adapter that supports 20Gbps/lane.</i>	RO	Vendor Defined
		20	ALPM Support 0: Not supported 1: Supported	RO	Vendor Defined
		21	Reserved	Rsvd	0
		22	8b10b TPS3 Capability 0: Not supported 1: Supported	RO	Vendor Defined
		23	Reserved	Rsvd	1
		24	8b10b TPS4 Capability 0: Not supported 1: Supported	RO	Vendor Defined

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		25	8b10b FEC Not Supported 0: Supported 1: Not supported A DP OUT Adapter shall set this bit to 0b if it sets the <i>DSC Not Supported</i> bit to 0b or it sets the <i>Panel Replay Tunneling Optimization Support</i> bit to 1b.	RO	Vendor Defined
		26	Secondary Split Capability 0: Not supported 1: Supported A DP OUT Adapter shall set this bit to 1b.	RO	1
		27	LTTPR Not Supported 0: Supported 1: Not supported A DP OUT Adapter shall set this bit to 0b.	RO	0
		28	Reserved	Rsvd	0
		29	DSC Not Supported 0: Supported 1: Not supported A DP OUT Adapter shall set this bit to 0b if it sets the <i>128b/132b Link Layer & 10Gbps/Lane Support</i> bit to 1b.	RO	Vendor Defined
		31:30	Reserved	Rsvd	0
DP_REMOTE_CAP register reflects the local capabilities of the paired DP IN Adapter. The Values in this register are set by the Connection Manager during Path Configuration. A DP OUT Adapter shall reset the fields in this register to their default values when the DP IN Adapter is unpaired.					
5	DP_REMOTE_CAP	3:0	Protocol Adapter Version Identifies what version of the USB4 Specification is supported by the paired DP IN Adapter 0h – 2h: Reserved 3h: Reserved for TBT3 4h: Version 1.0 5h: Version 2.0 6h – Fh: Reserved	R/W	0
5	DP_REMOTE_CAP	7:4	Maximal DPCD Rev 0h: DPCD r1.1 1h: DPCD r1.2 2h: DPCD r1.3 3h: DPCD r1.4a 4h – Fh: Reserved	R/W	0
		11:8	8b10b Maximal Link Rate 0h: 1.62 Gbps/lane 1h: 2.7 Gbps/lane 2h: 5.4 Gbps/lane 3h: 8.1 Gbps/lane 4h – Fh: Reserved	R/W	0
		14:12	Maximal Lane Count 0: 1 lane 1: 2 lanes 2: 4 lanes 3 – 7: Reserved	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		15	8b10b MST Capability 0: Not supported 1: Supported	R/W	0
		16	Panel Replay Tunneling Optimization Support 0: Not supported 1: Supported	R/W	0
		17	128b/132b Link Layer & 10Gbps/Lane Support Link rate associated with UHBR10. 0: Not supported 1: Supported	R/W	0
		18	20Gbps/Lane Support Link rate associated with UHBR20. 0: Not supported 1: Supported	R/W	0
		19	13.5Gbps/Lane Support Link rate associated with UHBR13.5. 0: Not supported 1: Supported	R/W	0
		20	ALPM Support 0: Not supported 1: Supported	R/W	0
		21	Reserved	RsvdZ	0
		22	8b10b TPS3 Capability 0: Not supported 1: Supported	R/W	0
		23	Vendor Defined	VD	Vendor Defined
		24	8b10b TPS4 Capability 0: Not supported 1: Supported	R/W	0
		25	8b10b FEC Not Supported 0: Supported 1: Not supported	R/W	0
		26	Secondary Split Capability 0: Not supported 1: Supported	R/W	0
		27	LTPR Not Supported 0: Supported 1: Not supported	R/W	0
		28	Reserved	RsvdZ	0
		29	DSC Not Supported 0: Supported 1: Not supported	R/W	0
		31:30	Reserved	RsvdZ	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
6	DP_STATUS_CTRL	2:0	Lane Count 0: DP Main Link is not Active 1: 1 Lane 2: 2 Lanes 4: 4 Lanes 3; 5 – 7: Reserved	RO	0
		7:3	Reserved	Rsvd	0
		11:8	Link Rate 0h: 1.62 Gbps/lane 1h: 2.7 Gbps/lane 2h: 5.4 Gbps/lane 3h: 8.1 Gbps/lane 4h: 10.0 Gbps/lane 5h: 20.0 Gbps/lane 6h: 13.5 Gbps/lane 7h – Fh: Reserved	RO	0
		16:12	Reserved	Rsvd	0
		24:17	Reserved	RsvdZ	0
		25	CM Handshake (CMHS) A Connection Manager uses this bit for the handshake defined in Section 10.4.2.1.	R/W	0
		26	DP IN Adapter USB4 Flag (UF) A Connection Manager uses this bit to indicate whether the DP IN Adapter is a USB4 DP IN Adapter or a TBT3 DP IN Adapter. 0: TBT3 1: USB4	R/W	0
		31:27	Reserved	RsvdZ	0
		This register reflects the lowest common capability between DP_LOCAL_CAP fields and DP_REMOTE_CAP fields. The DP_COMMON_CAP fields shall be updated any time the DP_REMOTE_CAP fields are updated.			
7	DP_COMMON_CAP	3:0	Protocol Adapter Version This field shall identify the highest common version of the USB4 Specification that is supported by both the DP OUT Adapter and the DP IN Adapter 0h – 2h: Reserved 3h: Reserved for TBT3 4h: Version 1.0 5h: Version 2.0 6h – Fh: Reserved	RO	0
		7:4	Maximal DPCD Rev 0h: DPCD r1.1 1h: DPCD r1.2 2h: DPCD r1.3 3h: DPCD r1.4a 4h – Fh: Reserved	RO	0
		11:8	8b10b Maximal Link Rate 0h: 1.62 Gbps/lane 1h: 2.7 Gbps/lane 2h: 5.4 Gbps/lane 3h: 8.1 Gbps/lane 4h – Fh: Reserved	RO	0

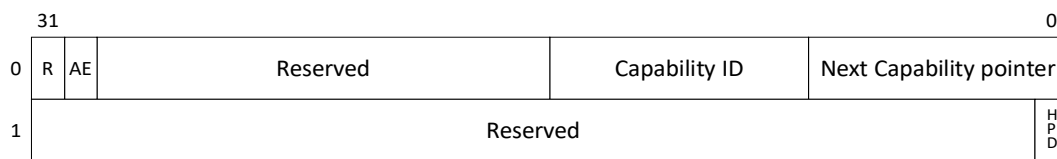
DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		14:12	Maximal Lane Count 0: 1 lane 1: 2 lanes 2: 4 lanes 3 – 7: Reserved	RO	0
		15	8b10b MST Capability 0: Not supported 1: Supported	RO	0
		16	Panel Replay Tunneling Optimization Support 0: Not supported 1: Supported	RO	0
		17	128b/132b Link Layer & 10Gbps/Lane Support Link rate associated with UHBR10. 0: Not supported 1: Supported	RO	0
		18	20Gbps/Lane Support Link rate associated with UHBR20. 0: Not supported 1: Supported	RO	0
		19	13.5Gbps/Lane Support Link rate associated with UHBR13.5. 0: Not supported 1: Supported	RO	0
		20	ALPM Support 0: Not supported 1: Supported	RO	0
		21	Reserved	Rsvd	0
		22	8b10b TPS3 Capability 0: Not supported 1: Supported	RO	0
		23	Vendor Defined	VD	0
7	DP_COMMON_CAP	24	8b10b TPS4 Capability 0: Not supported 1: Supported	RO	0
		25	8b10b FEC Not Supported 0: Supported 1: Not supported	RO	0
		26	Secondary Split Capability 0: Not supported 1: Supported	RO	0
		27	LTTPR Not Supported 0: Supported 1: Not supported	RO	0
		28	Reserved	Rsvd	0
		29	DSC Not Supported 0: Supported 1: Not supported	RO	0
		31:30	Reserved	Rsvd	0
8	ADP_DP_CS_8	31:0	Reserved	Rsvd	0

**CONNECTION MANAGER NOTE**

A Connection Manager shall set the values in the DP OUT Adapter Configuration Capability after it receives a Hot Plug Event Packet with the UPG bit set to 0b from the Adapter, and before it sets the Video Enable bit or the Aux Enable bit in the Adapter to 1b.

8.2.2.6.3 DP OUT AUX Adapter Configuration Capability

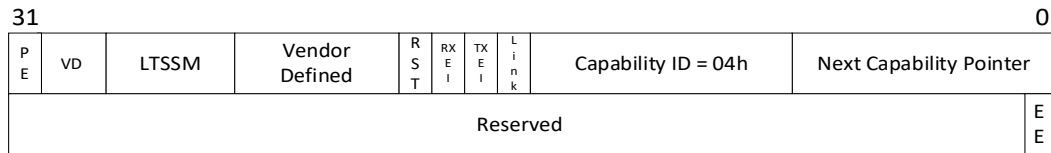
A DP OUT AUX Adapter Configuration Capability shall have the structure depicted in Figure 8-15 and shall have the fields defined in Table 8-18.

Figure 8-15. Structure of DP OUT AUX Adapter Configuration Capability**Table 8-18. DP OUT AUX Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_DP_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. An Adapter shall set this field to 00h if the Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 04h indicating this is a Protocol Adapter Configuration Capability.	RO	04h
		29:16	Reserved	Rsvd	0
		30	AUX Enable (AE) A Connection Manager uses this bit to control when the DP OUT AUX Adapter can send and receive packets on the AUX Path. When set to 1, the Adapter may send and receive packets on the AUX Path. When set to 0, the Adapter shall not send packets on the AUX Path and shall set Adapter Configuration Space to its default values as defined in Section 10.2.2.	R/W	0
		31	Reserved	Rsvd	0
1	ADP_DP_CS_1	0	HPD Status This field shall contain the HPD value of the connector that is connected to the DP OUT AUX Adapter. If no connector is connected to the Adapter, this field shall be set to 0b.	RO	0
		31:1	Reserved	Rsvd	0

8.2.2.7 PCIe Adapter Configuration Capability

A PCIe Adapter Configuration Capability shall have the structure depicted in Figure 8-16 and shall have the fields defined in Table 8-19.

Figure 8-16. Structure of PCIe Adapter Configuration Capability**Table 8-19. PCIe Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_PCIE_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. An Adapter shall set this field to 00h if the Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 04h indicating this is a Protocol Adapter Configuration Capability.	RO	04h
		16	Link An Adapter shall set this bit to indicate the LinkUp state of the PCIe Physical Layer Logical Sub-block above the PCIe Adapter: 0: Link is down 1: Link is up	RO	0b
		17	TX EI An Adapter shall set this bit to indicate whether the PCIe Physical Layer Logical Sub-block above the PCIe Adapter is in Electrical Idle state for its transmitter: 0b: Transmitter is not in Electrical Idle state 1b: Transmitter is in Electrical Idle state	RO	1b
		18	RX EI An Adapter shall set this bit to indicate whether the PCIe Physical Layer Logical Sub-block above the PCIe Adapter is in Electrical Idle state for its receiver: 0b: Receiver is not in Electrical Idle state 1b: Receiver is in Electrical Idle state	RO	1b
		19	RST An Adapter shall set this bit to indicate whether the attached Internal PCIe Port is in reset due to assertion of PERST# to the respective internal PCIe Port: 0b: Internal PCIe Port is not in reset 1b: Internal PCIe Port is in reset	RO	1b
		24:20	Vendor Defined	VD	Vendor Defined

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		28:25	LTSSM An Adapter shall set this bit to indicate the LTSSM state in the PCIe Physical Layer Logical Sub-block above the PCIe Adapter: 0h: Detect state 1h: Polling state 2h: Configuration state 3h: Configuration.Idle state 4h: Recovery state 5h: Recovery.idle state 6h: L0 state 7h: L1 state 8h: L2 state 9h: Disabled state Ah: Hot Reset state Bh – Fh: Reserved	RO	0h
		30:29	Vendor Defined	VD	Vendor Defined
		31	Path Enable (PE) A Connection Manager uses this bit to control when a PCIe Adapter can send and receive PCIe Tunneled Packets across the USB4 Fabric. It also controls the in-band presence indication to the internal PCIe Switch: 0b: PCIe Packets shall not be sent. In-band presence is set to 0b 1b: PCIe Tunneled Packets may be sent. In-band presence is set to 1b	RW	0b
1	ADP_PCIE_CS_1	0	Extended Encapsulation (EE) A Connection Manager uses this field to enable extended encapsulation (see Section 11.1.1.1.3). 0b – Disabled 1b – Enabled	R/W	0
		31:1	Reserved	Rsvd	0

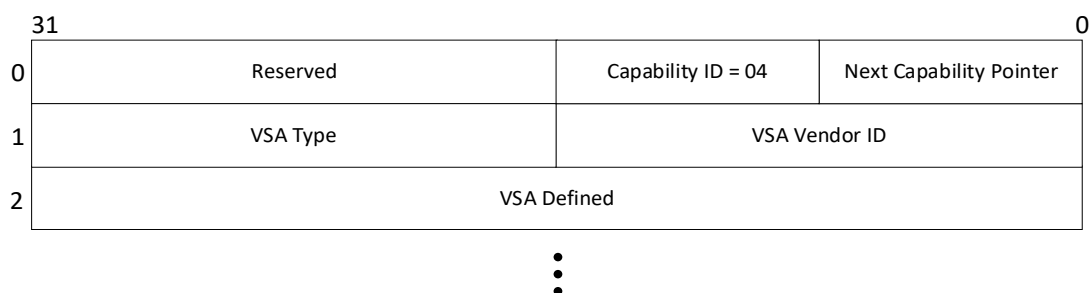


CONNECTION MANAGER NOTE

A Connection Manager shall set the Extended Encapsulation bit to the desired value before it sets the Path Enable bit in the Adapter to 1b.

8.2.2.8 Vendor Specific Adapter Configuration Capability

A Vendor Specific Adapter Configuration Capability shall have the structure depicted in Figure 8-17 and shall have the fields defined in Table 8-20.

Figure 8-17. Structure of Vendor Specific Adapter Configuration Capability**Table 8-20. Vendor Specific Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_VS_CS_0	7:0	Next Capability Pointer This field shall contain the Doubleword index of the next Capability in the Adapter Configuration Space. An Adapter shall set this field to 00h if the Capability is the final Capability in the linked list of Capabilities in the Adapter Configuration Space.	RO	Vendor Defined
		15:8	Capability ID An Adapter shall set this field to 04h indicating this is a Protocol Adapter Configuration Capability.	RO	04h
		31:16	Reserved	Rsvd	0h
1	ADP_VS_CS_1	15:0	VSA Vendor ID This field shall contain the Vendor ID, assigned by USB-IF, of the vendor that defined this Vendor Specific Adapter.	RO	Vendor Defined
		31:16	VSA Type This field defines the type of the Vendor Specific Adapter. This field is assigned by the vendor that defined this Vendor Specific Adapter.	RO	Vendor Defined
2:n	ADP_VS_CS_2... ADP_VS_CS_n	31:0	VSA Defined The definition of the rest of the Configuration Capability fields are according to the definition of this specific Vendor Specific Adapter.	VD	Vendor Defined

**IMPLEMENTATION NOTE**

It is recommended that a Vendor Specific Adapter implement a QoS scheme such as the ones defined for USB3 Gen X, USB3 Gen T, PCIe or DisplayPort.

**CONNECTION MANAGER NOTE**

The Connection Manager will skip the Vendor Specific Adapter if it does not recognize it. The association between an application and a Vendor Specific Adapter is made based on the values of the Adapter Type Sub-type, Adapter Type Version, VSA Type and VSA Vendor ID (which is unique per application regardless to the value of Vendor ID (ROUTER_CS_0)). A Connection Manager that recognizes a Vendor Specific Adapter should be able to establish Paths between two Vendor Specific Adapters of the same type and configure any applicable QoS parameters.

**CONNECTION MANAGER NOTE**

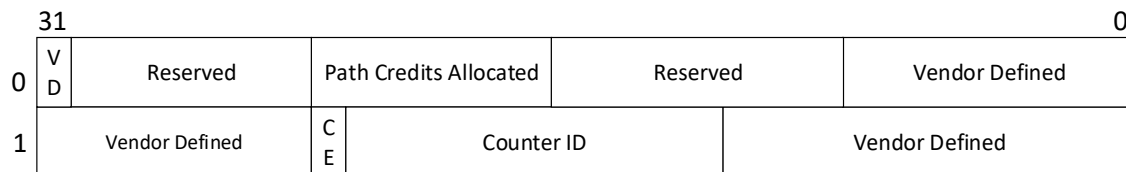
A Connection Manager may configure Paths between the Vendor Specific Adapter in a USB4 Host and the Vendor Specific Adapter in a USB4 Device. The Connection Manager shall not configure any Paths between the Vendor Specific Adapters in two USB4 Devices.

8.2.3 Path Configuration Space

The Path Configuration Space in an Adapter contains a 2-Doubleword entry for each Path supported by the Adapter. Section 8.2.3.1 defines entry for Path 0. Section 8.2.3.2 defines the Path entries for a Lane Adapter. Section 8.2.3.3 defines the Path entries for a Protocol Adapter.

8.2.3.1 Path 0 Entry

A Lane Adapter and a Host Interface Adapter shall support a Path for HopID 0 (referred to as “Path 0”). Figure 8-18 shows the Path Configuration Space entry for Path 0. Table 8-21 defines the fields for Path 0.

Figure 8-18. Structure of Path 0 Entry Configuration Space**Table 8-21. Contents of Path 0 Entry**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	PATH_CS_0	5:0	Vendor Defined	VD	Vendor Defined
		16:6	Reserved	Rsvd	0h
		23:17	Path Credits Allocated This field shall contain the initial value of the <i>Path Credits Allocated</i> state variable for the Ingress Adapter of the Path.	RO	Vendor Defined (Minimum 2h)
		30:24	Reserved	Rsvd	0
		31	Vendor Defined	VD	Vendor Defined
1	PATH_CS_1	11:0	Vendor Defined	VD	Vendor Defined
		22:12	Counter ID A Connection Manager uses this field to set the ID number of the counter set that is used to collect statistics for the Path. The Counter ID shall be less than the <i>Max Counter Sets</i> field for the Adapter. This field is valid only when the <i>Counter Enable (CE)</i> bit is set to 1b.	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		23	Counter Enable (CE) A Connection Manager uses this bit to enable the counters in Counter Configuration Space for the Path. 1b: Counter set for Path is enabled 0b: Counter set for Path is disabled When this bit is 1b, the Adapter shall increment the counter set for the Path as defined in Table 8-24.	R/W	0
		31:24	Vendor Defined	VD	Vendor Defined

8.2.3.2 Lane Adapters

A Lane Adapter shall support Paths from HopID 8 to Max Input HopID (inclusive). Each entry shall be formatted as shown in Figure 8-19. Table 8-22 defines the fields for a Path entry. The entries for the Paths with HopIDs 1 through 7 are undefined and the space is reserved.

When a Path is configured to route Tunneled Packets from a USB4 Port to a Protocol Adapter the following Path entry fields shall be ignored by the Router:

- *Weight.*
- *Egress Flow Control Flag.*
- *Egress Shared Buffering Enable Flag.*

Figure 8-19. Structure of Path Entry ‘n’ in the Path Configuration Space of a Lane Adapter

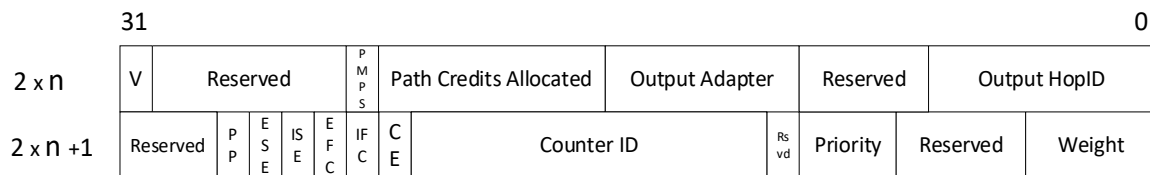


Table 8-22. Contents of Path Entry in the Path Configuration Space of a Lane Adapter

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	PATH_CS_0	6:0	Output HopID A Connection Manager uses this field to set the Egress HopID for the Path.	R/W	00h
		10:7	Reserved	Rsvd	0h
		16:11	Output Adapter A Connection Manager uses this field to set the Adapter Number of the Egress Adapter for the Path.	R/W	00h
		23:17	Path Credits Allocated A Connection Manager uses this field to set the initial value of the Path Credits Allocated state variable for the Ingress Adapter of the Path.	R/W	0
		24	PM Packet Support (PMPS) A Connection Manager uses this bit to indicate whether this Path objects to CLx if the last packet transmitted through it was not a PM Packet.	R/W	0
		30:25	Reserved	Rsvd	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		31	Valid A Connection Manager uses this field to enable or disable the Path. 1b: The contents of this Path entry are valid. 0b: The contents of this Path entry are not valid.	R/W	0b
1	PATH_CS_1	3:0	Weight A Connection Manager uses this field to set the WRR scheduler weight for the Path.	R/W	0h
		7:4	Reserved	Rsvd	0h
		10:8	Priority A Connection Manager uses this field to set the Priority Group for the Path.	R/W	0h
		11	Reserved	Rsvd	0b
		22:12	Counter ID A Connection Manager uses this field to set the ID number of the counter set that is used to collect statistics for the Path. The Counter ID shall be less than the <i>Max Counter Sets</i> field for the Adapter. This field is valid only when the <i>Counter Enable (CE)</i> bit is set to 1b.	R/W	0
		23	Counter Enable (CE) A Connection Manager uses this bit to enable the counters in Counter Configuration Space for the Path. 1b: Counter set for Path is enabled 0b: Counter set for Path is disabled When this bit is 1b, the Adapter shall increment the counter set for the Path as defined in Table 8-24.	R/W	0
		24	Ingress Flow Control (IFC) Flag A Connection Manager uses this bit in combination with the ISE Flag to configure the Ingress Flow Control scheme. See Table 5-13.	R/W	0b
		25	Egress Flow Control (EFC) Flag A Connection Manager uses this bit in combination with the ESE Flag to configure the Egress Flow Control scheme. See Table 5-15.	R/W	0b
		26	Ingress Shared Buffering Enable (ISE) Flag A Connection Manager uses this bit in combination with the IFC Flag to configure the Ingress Flow Control scheme. See Table 5-13.	R/W	0b
		27	Egress Shared Buffering Enable (ESE) Flag A Connection Manager uses this bit in combination with the EFC Flag to configure the Egress Flow Control scheme. See Table 5-15.	R/W	0b
		28	Pending Packets (PP) An Adapter shall set this field to 1b when one or more packets that belong to the Path are waiting to be dequeued. Otherwise it shall be set to zero.	RO	0b
		29	Reserved	RsvdZ	0b
		31:30	Reserved	Rsvd	00b

8.2.3.3 Protocol Adapters

A Host Interface Adapter shall support Paths from HopID 1 to Max Input HopID (Inclusive). A USB3/PCIe/DP Adapter shall support Paths from HopID 8 to Max Input HopID (Inclusive). Each entry shall be formatted as shown in Figure 8-20. Table 8-23 defines the fields for a Path entry.

Figure 8-20. Structure of Path Entry ‘n’ in the Path Configuration Space of a Protocol Adapter

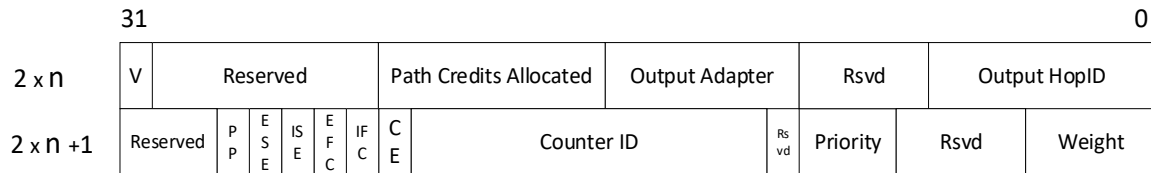


Table 8-23. Contents of Path Entry in the Path Configuration Space of a Protocol Adapter

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	PATH_CS_0	6:0	Output HopID A Connection Manager uses this field to set the Egress HopID for the Path.	R/W	00h
		10:7	Reserved	Rsvd	0h
		16:11	Output Adapter A Connection Manager uses this field to set the Adapter Number of the Egress Adapter for the Path.	R/W	00h
		23:17	Path Credits Allocated It is recommended that a Router set this field to 0b	VD	Vendor Defined
		30:24	Reserved	Rsvd	0
		31	Valid A Connection Manager uses this field to enable or disable the Path. 1b: The contents of this Path entry are valid. 0b: The contents of this Path entry are not valid.	R/W	0b
1	PATH_CS_1	3:0	Weight A Connection Manager uses this field to set the WRR scheduler weight for the Path.	R/W	0h
		7:4	Reserved	Rsvd	0h
		10:8	Priority A Connection Manager uses this field to set the Priority Group for the Path.	R/W	0h
		11	Reserved	Rsvd	0b
		22:12	Counter ID A Connection Manager uses this field to set the ID number of the counter set that is used to collect statistics for the Path. The Counter ID shall be less than the <i>Max Counter Sets</i> field for the Adapter. This field is valid only when the <i>Counter Enable (CE)</i> bit is set to 1b.	R/W	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		23	Counter Enable (CE) A Connection Manager uses this bit to enable the counters in Counter Configuration Space for the Path. 1b: Counter set for Path is enabled 0b: Counter set for Path is disabled When this bit is 1b, the Adapter shall increment the counter set for the Path as defined in Table 8-24.	R/W	0
		24	Ingress Flow Control (IFC) Flag It is recommended that an Adapter set this field to 0b.	VD	Vendor Defined
		25	Egress Flow Control Flag (EFC) Flag A Connection Manager uses this bit in combination with the ESE Flag to configure the Egress Flow Control scheme. See Table 5-13.	R/W	0b
		26	Ingress Shared Buffering Enable (ISE) Flag It is recommended that an Adapter set this field to 0b.	VD	Vendor Defined
		27	Egress Shared Buffering Enable (ESE) Flag A Connection Manager uses this bit in combination with the EFC Flag to configure the Egress Flow Control scheme. See Table 5-13.	R/W	0b
		28	Pending Packets (PP) An Adapter shall set this field to 1b when one or more packets that belong to the Path are waiting to be dequeued. Otherwise it shall be set to zero.	RO	0b
		29	Reserved	RsvdZ	0b
		31:30	Reserved	Rsvd	00b



CONNECTION MANAGER NOTE

When writing to the Path Configuration Space of a Lane Adapter or Protocol Adapter, a Connection Manager shall abide by the following rules:

- *The Connection Manager needs to read a Path Configuration Space register before writing to it. The Connection Manager shall not change the value of any fields that are defined as RsvdZ or VD. See Section 8-1 for more information.*
- *The Weight field for a Path cannot be 0 if the Valid bit is 1b.*
- *The Priority field for a Path needs to be set to a value between 1 and 7 (inclusive).*
- *The Output Adapter field for a Path needs to be set to an Adapter that has a Path Configuration Space.*

8.2.3.4 Path Configuration Space Access

When a Connection Manager configures a Path, within a Router, from Ingress Adapter N, HopID 'n' to Egress Adapter M, it issues the following single write access:

- The *Adapter Num* field shall be equal to N.
- The *Address* field shall be equal to 2 x 'n'.
- The *Length* field shall be equal to 2.

Note: To configure the above Path, no access is issued to Adapter M.

**CONNECTION MANAGER NOTE**

When a Connection Manager reads from a Path, it shall issue a single Read Request that reads both doublewords of the Path.

When a Connection Manager writes to a Path, it shall issue a single Write Request that writes to both doublewords of the Path.

**CONNECTION MANAGER NOTE**

A Version 1 Connection Manager may Tear down a Path by writing only the first doubleword of the Path.

**CONNECTION MANAGER NOTE**

A Connection Manager can access registers for multiple contiguous Paths by increasing the read/write Length in a Read or Write Request. For example, a Read Request targeting the entries for the Paths with Ingress HopIDs 8 and 9 would contain values of 16 in the Address field and 4 in the Length field.

A Connection Manager shall not send a Read or a Write Request that targets a Path Configuration Space entry that is either reserved or does not exist.

**CONNECTION MANAGER NOTE**

The only fields in the Path Configuration Space entry for Path 0 that a Connection Manager can change are the Counter ID field and the Counter Enable bit. In order to avoid changing the value of the other fields, it is recommended that a Connection Manager first read the Path Configuration Space entry for Path 0, make the necessary changes to the Counter ID field and the Counter Enable bit, then write the results back to Path Configuration Space.

**CONNECTION MANAGER NOTE**

After setting the Valid bit to 1b in a Path Configuration Space, a Connection Manager shall not modify any fields except the Weight field and the Valid bit.

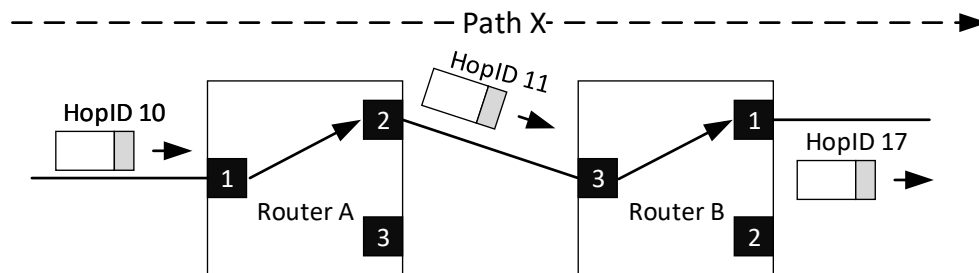
8.2.3.4.1 Path Configuration Example

The entry for a Path contains fields that apply to the Ingress Adapter of the Path and fields that apply to the Egress Adapter of the Path, however, all parameters are written to the Ingress Adapter. In the example shown in Figure 8-21, configuring the Routers along Path X requires one configuration per Router:

- Router A: Single Path access to Path 10 at Adapter Number 1.
- Router B: Single Path access to Path 11 at Adapter Number 3.

Note: The Path Configuration Spaces of Adapter 2 in Router A and Adapter 1 in Router B are independent of Path X and therefore do not reflect any of the above configuration.

Figure 8-21. Configuration of a Path

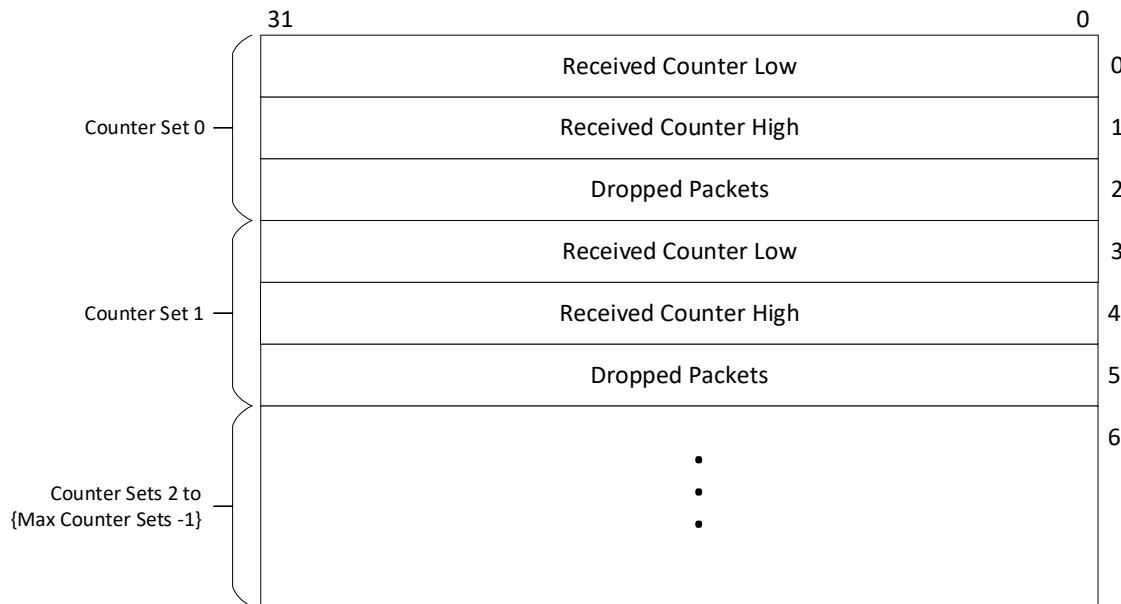


8.2.4 Counters Configuration Space

An Adapter with the CCS Flag in the Adapter Configuration Space set to 1b shall implement the Counters Configuration Space depicted in Figure 8-22.

A Counter Configuration Space shall contain the number of counter sets specified in the *Max Counter Sets* field from the Adapter Configuration Space. Each counter set shall consist of the three counters described in Table 8-24.

A Path is associated with a counter set through the *Counter ID* field in the Path Configuration Space. A Path can only be associated with one counter set. However a single counter set may count Transport Layer Packets or bytes for more than one Path.

Figure 8-22. Structure of the Counters Configuration Space**Table 8-24. Counter Set Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	CNT_CS_0	31:0	Received Counter Low This field shall contain the lower 32 bits of a 64-bit Received Counter value. If the <i>Received Bytes Counter Enable</i> field is set to 0b: An Ingress Adapter shall increment the Received Counter value by 1 each time it receives a Transport Layer Packet on a Path that uses this counter set. If the <i>Received Bytes Counter Enable</i> field is set to 1b: An Ingress Adapter shall increment the Received Counter value by the Transport Layer Packet payload length, as provided in the <i>Length</i> field of the received Transport Layer Packets being routed to the subject Path. The Received Counter shall increment from 0 and shall stop counting at FFFF FFFF FFFF FFFFh.	W/Clr	0
1	CNT_CS_1	31:0	Received Counter High This field contains the upper 32 bits of a 64-bit Received Counter. An Ingress Adapter shall increment the Received Counter by 1 each time the Received Counter Low is overflowed. The counter shall increment from 0 and shall stop counting at FFFF FFFF FFFF FFFFh.	W/Clr	0
2	CNT_CS_2	31:0	Dropped Packets This field contains a 32-bit dropped packets counter. An Ingress Adapter shall increment the dropped packets counter by 1 for every packet that is dropped due to insufficient buffer space for a Path that uses this counter set. The counter shall increment from 0 and shall stop counting at FFFF FFFFh.	W/Clr	0

**CONNECTION MANAGER NOTE**

It is recommended that a Connection Manager read the Received Packets Low field and the Received Packets High field in a single Read Request in order to guarantee that the received packets counter values are from the same counter snapshot.

**CONNECTION MANAGER NOTE**

It is recommended that a Connection Manager read the Received Counter Low field and the Received Counters High field in a single Read Request to guarantee that the received bytes counter values are from the same counter snapshot. Alternatively, Connection Manager can use the Lock Bytes Counter with TimeOffsetFromHR Low field to ensure that the values are from the same counter snapshot and use Host Router's Local Clock for accurate bandwidth calculation.

8.3 Operations

A Router supports a Router-level interface and a Port-level interface that allow a Connection Manager to initiate various Operations.

The Router-level interface initiates Router Operations, which perform Router-wide tasks such as NVM read/write and DisplayPort™ resource management. Section 8.3.1 defines Router Operations.

The Port-level interface initiates Port Operations, which can be used to initiate Port-level tasks such as compliance tests, NVM access, and receiver Lane margining tests. Section 8.3.2 defines Port Operations.

A Router shall handle Router Operations and Port Operations concurrently.

Unless otherwise specified, fields and values marked “Reserved” shall be handled as described in Table 8-25.

Table 8-25. Reserved Value and Field Handling

Type	Handling
Reserved value	<p>A value that is marked as “Reserved” shall not be used when initiating or completing an Operation.</p> <p>The target of a Router Operation shall respond to an Operation that has any of its defined fields set to a Reserved value by setting the <i>Status</i> field in the completion with a value of 1h.</p> <p>The target of a Port Operation shall respond to an Operation that has any of its defined fields set to a Reserved value by setting the <i>Opcode</i> register to a FourCC value of “ERR ” (20525245h).</p>
Reserved field	<p>When writing to a field that is marked “Reserved”, the value shall be set to zero.</p> <p>When reading from a field that is marked “Reserved”, the value shall be ignored.</p>

8.3.1 Router Operations

A Connection Manager writes to the ROUTER_CS_9 through ROUTER_CS_26 registers in Router Configuration Space to initiate a Router Operation.

A Router shall process a Router Operation when the *Operation Valid* bit changes from 0b to 1b. The Router shall execute the specific Router Operation indicated by the *Opcode* field as defined in the sections below.

When a Router Operation is defined to include metadata information, the Router shall fetch the information from the *Metadata* field in Router Configuration Space.

When a Router Operation is defined to include additional information, the Router shall fetch the information from the *Data* DWs in Router Configuration Space.

Once the Router Operation is complete, the Router shall:

1. If the Router Operation returns completion metadata information, write the metadata information to the *Metadata* field in Router Configuration Space.
2. If the Router Operation returns additional completion information, write the additional information to the *Data* DWs in Router Configuration Space.
3. Set the *Operation Not Supported* bit to 0b if the Router supports the Operation. Set the *Operation Not Supported* bit to 1b if the Router does not support the Operation.
4. If the *Operation Not Supported* bit is 0b, update the *Status* field with the results of the Router Operation.
 - If the Operation is supported by the Router but is not executed for any reason, set the *Status* field to 1h.

Note: The Status field is only applicable when the Operation Not Supported bit is set to 0b.

5. Set the *Operation Valid* bit to 0b.
6. Send the Connection Manager a Notification Packet with Event Code = ROP_CMPLT and the *Event Info* field set to 00h. See Section 6.4.2.7 for more information on Notification Packets.



CONNECTION MANAGER NOTE

If an Operation does not write to the Metadata field, then a Connection Manager shall set it to 0 when issuing the Operation.

If an Operation does not write to a Data DW, then a Connection Manager shall set that DW to 0 when issuing the Operation.

A Connection Manager shall not issue a new Router Operation until the previous Router Operation has completed.

Table 8-26 lists the Router Operations defined for a Router.

Table 8-26. List of Router Operations

Router Operation	Opcode	Operation		Completion		Reference
		Metadata DW	Data DWs	Metadata DW	Data DWs	
Reserved	00h – 0Fh	--	--	--	--	none
Query DP Resource Availability	10h	1	0	1	0	Section 8.3.1.1.1
Allocate DP Resource	11h	1	0	1	0	Section 8.3.1.1.2
De-allocate DP Resource	12h	1	0	1	0	Section 8.3.1.1.3
Connect DP OUT Adapter	13h	1	0	1	0	Section 8.3.1.1.4
Reserved	14h – 1Fh	--	--	--	--	none
NVM Write	20h	0	1 to 16	0	0	Section 8.3.1.2.2
NVM Authenticate Write	21h	0	0	0	0	Section 8.3.1.2.3
NVM Read	22h	1	0	1	1 to 16	Section 8.3.1.2.4
NVM Set Offset	23h	1	0	1	0	Section 8.3.1.2.1
DROM Read	24h	1	0	1	1 to 16	Section 8.3.1.2.5
Get NVM Sector Size	25h	0	0	1	0	Section 8.3.1.2.6
Reserved	26h – 2Fh	--	--	--	--	none
Get PCIe Downstream Entry Mapping	30h	0	0	1	2	Section 8.3.1.3.1
Get Capabilities	31h	1	0	1	1 to 16	Section 8.3.1.3.2
Set Capabilities	32h	1	0 to 16	0	0	Section 8.3.1.3.2.2
Buffer Allocation Request	33h	1	0	1	1 to 5	Section 8.3.1.3.4
Block Sideband Port Operations	34h	0	0	0	0	Section 8.3.1.4.1
Unblock Sideband Port Operations	35h	0	0	0	0	Section 8.3.1.4.2
Get Container-ID	36h	0	0	0	4	Section 8.3.1.3.5
Get Connectors Information	37h	0	0	1	3	Section 8.3.1.3.6
Reserved	38h – 7FFFh	--	--	--	--	none
Vendor Specific Router Operations	8000h – FFFFh	--	--	--	--	none

8.3.1.1 DP Tunneling Operations**8.3.1.1.1 Query DP Resource Availability (Conditional)**

A Router shall support the Query DP Resource Availability Router Operation if it has one or more DP IN Adapters. This Router Operation is not applicable for Routers that do not have a DP IN Adapter.

Operation Initiation

Table 8-27 defines the contents of the *Metadata* field for a Query DP Resource Availability Router Operation.

Table 8-27. Query DP Resource Availability Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	31:0	DisplayPort Number This field contains the DP IN Adapter Number queried by the Router Operation.

This Router Operation does not write to the *Data* DWs.

Operation Completion

A Router shall return the *Metadata* and *Status* fields defined in Table 8-28.

Table 8-28. Query DP Resource Availability Completion Metadata and Status

Field	Bit(s)	Description
<i>Metadata</i>	31:0	DisplayPort Number This field contains the <i>DisplayPort Number</i> value from the Operation Metadata.
<i>Status</i>	29:24	Status 0h: A DP Source is detected and a resource is available to be allocated to the DP IN Adapter 1h: No DP Source is detected and/or a resource is not available to be allocated to the DP IN Adapter 2h – Fh: Reserved

This Operation does not return any *Data* DWs.

8.3.1.1.2 Allocate DP Resource (Conditional)

A Router shall support the Allocate DP Resource Availability Router Operation if it has one or more DP IN Adapters. This Router Operation is not applicable for Routers that do not have a DP IN Adapter.

Operation Initiation

Table 8-29 defines the contents of the *Metadata* field for an Allocate DP Resource Router Operation.

Table 8-29. Allocate DP Resource Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	31:0	DisplayPort Number This field contains the Adapter Number of the DP IN Adapter that is the recipient of the allocated DP stream resource.

This Router Operation does not write to the *Data* DWs.

Operation Completion

A Router shall return the *Metadata* and *Status* fields defined in Table 8-30.

Table 8-30. Allocate DP Resource Completion Metadata and Status

Field	Bit(s)	Description
<i>Metadata</i>	31:0	DisplayPort Number This field contains the <i>DisplayPort Number</i> value from the Operation Metadata.
<i>Status</i>	29:24	Status 0h: Resource was allocated 1h: Resource was not allocated 2h – Fh: Reserved If a resource was already allocated to this DP IN Adapter by a previous Allocate DP Resource Operation, then a Router shall respond with <i>Status</i> = 0h.

This Operation does not return any *Data* DWs.

8.3.1.1.3 De-allocate DP Resource (Conditional)

A Router shall support the De-Allocate DP Resource Availability Router Operation if it has one or more DP IN Adapters. This Router Operation is not applicable for Routers that do not have a DP IN Adapter.

Operation Initiation

Table 8-31 defines the contents of the *Metadata* field for a De-allocate DP Resource Router Operation.

Table 8-31. De-Allocate DP Resource Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	31:0	DisplayPort Number This field contains the Adapter Number of the DP IN Adapter that is the recipient of the DP stream resource that is being de-allocated.

This Router Operation does not write to the *Data* DWs.

Operation Completion

A Router shall return the *Metadata* and *Status* fields defined in Table 8-32.

Table 8-32. De-Allocate DP Resource Completion Metadata and Status

Field	Bit(s)	Description
<i>Metadata</i>	31:0	DisplayPort Number This field contains the <i>DisplayPort Number</i> value from the Operation Metadata.
<i>Status</i>	29:24	Status 0h: Resource was de-allocated 1h: Resource was not de-allocated 2h – Fh: Reserved If no resource is allocated to this DP IN Adapter, then a Router shall respond with <i>Status</i> = 0h.

This Router Operation does not return any *Data* DWs.

8.3.1.1.4 Connect DP OUT Adapter (Conditional)

A Connection Manager uses this Operation to either connect or disconnect a Connector and a DP OUT Adapter or a DP OUT AUX Adapter.

A Device Router shall support this Router Operation if it supports DPRX Discovery through the Partial Implementation option. This Router Operation is not applicable for a Host Router. This Router Operation is not applicable for a Device Router that supports DPRX Discovery through the Full Implementation option.

Operation Initiation

Table 8-33 defines the contents of the *Metadata* field for a Connect DP OUT Adapter Router Operation.

Table 8-33. Connect DP OUT Adapter Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	5:0	Adapter Number This field contains either the DP OUT Adapter Number or the DP OUT AUX Adapter Number to be connected to or disconnected from the Connector.
	6	Reserved
	7	Connect 0 – A Router shall disconnect the Adapter that corresponds to the <i>Adapter Number</i> field from the Connector that corresponds to the <i>Connector Number</i> field. 1 – A Router shall connect the Adapter that corresponds to the <i>Adapter Number</i> field to the Connector that corresponds to the <i>Connector Number</i> field.
	11:8	Connector Number This field contains the Connector number to be connected or disconnected from the DP OUT Adapter or the DP OUT AUX Adapter.
	31:12	Reserved

This Router Operation does not write to the *Data* DWs.

Operation Completion

A Router shall return the *Metadata* and *Status* fields defined in Table 8-34.

Table 8-34. Connect DP OUT Adapter Completion Metadata and Status

Field	Bit(s)	Description
<i>Metadata</i>	5:0	Adapter Number This field contains the <i>Adapter Number</i> value from the Operation Metadata.
	6	Reserved
	7	Connect This field contains the <i>Connect</i> value from the Operation Metadata.
	11:8	Connector Number This field contains the <i>Connector Number</i> value from the Operation Metadata.
	31:12	Reserved
<i>Status</i>	29:24	Status 0h: (Successful) Connectivity is set according to the operation. 1h: (Failure) Connectivity is not set according to the operation. 2h – Fh: Reserved. If the connectivity is the same as previously set by the Connection Manager, then a Router shall respond with Status = 0h.

This Router Operation does not return any *Data* DWs.

8.3.1.2 NVM Operations

NVM Operations are used to read from and write to the Non Volatile Memory (NVM) in a USB4 product. The following is an example of a Router Operation sequence used by software to update the NVM of a Router:

1. Software issues a Get NVM Sector Size Operation to read the sector size of the NVM.
2. Software issues an NVM Set Offset Operation, which sets the first location in NVM to be written by the following NVM Write Operation.
3. Software issues a sequence of NVM Write Operations, each writing a 64B block of data to NVM.
 - Following an NVM Write Operation, if the value of the *Status* field in the completion status is 1h, software repeats all previous NVM Write Operations. The first Router Operation to be issued is an NVM Set Offset Operation that sets the location in NVM of the first block to be rewritten.
4. Software issues an NVM Authenticate Write Operation to indicate to the target that all data was sent to the target. After receiving the NVM Authenticate Write Operation, the target performs an authentication check over the data written.

The following is an example of a Router Operation sequence used by software to validate the results of the NVM update:

1. Software then waits for at least 5 seconds from the completion of the NVM Authenticate Write Operation.
2. Software reads the results of the NVM Authenticate Write Operation. If the *Status* field in the Completion Metadata is 0h, the update ended successfully. If the *Status* field is not 0h, then software repeats all previous NVM Write Operations. The first Router Operation issued is an NVM Set Offset Operation that sets the location in NVM of the first block to be rewritten, followed by re-issuing one or more NVM Write Operations.

8.3.1.2.1 NVM Set Offset (Conditional)

A ~~Device~~Router may optionally ~~shall~~ support the NVM Set Offset Router Operation. ~~A Host Router may optionally support this Router Operation.~~

The NVM Set Offset Router Operation sets the first location in NVM to be written by the following NVM Write Router Operation.

Operation Initiation

Table 8-35 defines the contents of the *Metadata* field for an NVM Set Offset Router Operation.

Table 8-35. NVM Set Offset Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	1:0	Reserved
	23:2	NVM Offset This field contains the first address to be written relative to the base address of the region being written to. NVM Offset is specified in DWs.
	31:24	Reserved

This Router Operation does not write to the *Data* DWs.

Operation Completion

A Router shall return the *Metadata* and *Status* fields defined in Table 8-36.

Table 8-36. NVM Set Offset Completion Metadata and Status

Field	Bit(s)	Description
<i>Metadata</i>	1:0	Reserved
	23:2	NVM Offset This field contains the NVM Offset value from the Operation.
	31:24	Reserved
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h: NVM is not implemented 3h – 3Fh: Reserved

This Router Operation does not return any *Data* DWs.

8.3.1.2.2 NVM Write (Conditional)

A ~~Device~~ Router ~~may optionally shall~~ support the NVM Write Router Operation. ~~A Host Router may optionally support this Router Operation.~~

The NVM Write Router Operation writes 64 bytes to NVM, starting at the address equal to the NVM Offset. A Router shall increment its NVM Offset value by 16 after executing an NVM Write Router Operation.

Operation Initiation

This Operation does not write to the *Metadata* field. Table 8-37 defines the contents of the *Data* DWs.

Table 8-37. NVM Write Operation Data

DW	Bit(s)	Description
0	31:0	DW0 The first Doubleword, to be written into NVM at <i>NVM Offset</i> address.
1	31:0	DW1 The second Doubleword, to be written into NVM at the next NVM Offset.
...	31:0	...
15	31:0	DW15 The last Doubleword of this Router Operation, to be written into NVM at the next NVM Offset.

Operation Completion

A Router shall return the *Status* field defined in Table 8-38.

Table 8-38. NVM Write Completion Status

Field	Bit(s)	Description
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h – 3Fh: Reserved

This Router Operation does not return any *Metadata* or *Data* DWs.

8.3.1.2.3 NVM Authenticate Write (Conditional)

A ~~Device~~ Router may optionally~~shall~~ support the NVM Authenticate Write Router Operation. ~~A Host Router may optionally support this Router Operation.~~

The NVM Authenticate Write Router Operation indicates to the target that all data was sent to the target. After receiving an NVM Authenticate Write Router Operation, the target performs an authentication check over the data written. The authentication check is implementation specific and outside the scope of this specification.

Operation Initiation

This Router Operation does not write to the *Metadata* field. It does not write to the *Data* DWs.

Operation Completion

A Router shall return the *Status* field defined in Table 8-39.

Table 8-39. NVM Authenticate Write Completion Status

Field	Bit(s)	Description
<i>Status</i>	29:24	Status 0h: Authentication completed successfully 1h: Authentication Failed 2h: Retry NVM write 3h: NVM is not implemented 4h – 3Fh: Reserved

If the *Status* field is 2h, then software writes the last blocks of data again, starting with the block whose offset is the beginning of a sector-aligned page that contains the last successful offset written minus the sector size. The first Router Operation to be issued is an NVM Set Offset Router Operation that sets the location in NVM of the first block to be rewritten, followed by issuing an NVM Authenticate Write Router Operation again.

This Router Operation does not return any *Metadata* or *Data* DWs.

8.3.1.2.4 NVM Read (Conditional)

A ~~Device~~ Router may optionally~~shall~~ support the NVM Read Router Operation. ~~A Host Router may optionally support this Router Operation.~~

The NVM Read Router Operation reads up to 64 bytes from NVM.

Operation Initiation

Table 8-40 defines the contents of the *Metadata* field for an NVM Read Router Operation.

Table 8-40. NVM Read Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	1:0	Reserved
	23:2	NVM Offset This field contains the first address to be read relative to the base address of the region being read. NVM Offset is specified in DWs.
	27:24	Length Number of Doublewords that shall be read starting from the <i>NVM Offset</i> field value. If this field is zero, then 16 DWs are read.
	31:28	Reserved

This Router Operation does not write to the *Data* DWs.

Operation Completion

A Router shall return the *Metadata* and *Status* fields defined in Table 8-41.

Table 8-41. NVM Read Router Completion Metadata

Field	Bit(s)	Description
<i>Metadata</i>	1:0	Reserved
	23:2	NVM Offset This field contains the <i>NVM Offset</i> value from the Operation Metadata.
	27:24	Length This field contains the <i>Length</i> value from the Operation Metadata.
	31:28	Reserved
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h – 3Fh: Reserved

If this Operation is completed successfully, the Router returns Length number of Doublewords of Data as shown in Table 8-42.

Table 8-42. NVM Read Router Completion Data

DW	Bit(s)	Description
0	31:0	DW0 The first Doubleword read from NVM at <i>NVM Offset</i> address.
1	31:0	DW1 The second Doubleword read from NVM at the next NVM Offset.
...	31:0	...
15	31:0	DW15 The last Doubleword read from NVM at the next NVM Offset.

8.3.1.2.5 DROM Read (Conditional)

A Device Router shall support the DROM Read Router Operation. A Standalone AIC Host Router shall support this Router Operation. A Platform Integrated Host Router may optionally support this Router Operation.

The DROM Read Router Operation reads up to 64 bytes from DROM.

Operation Initiation

Table 8-43 defines the contents of the *Metadata* field for a DROM Read Router Operation.

Table 8-43. DROM Read Router Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	1:0	Reserved
	14:2	Address DW address in DROM relative to DROM first address. Address = 0 targets the first DW in DROM.
	19:15	Read Size Number of Doublewords that shall be read starting from the <i>Address</i> field value. The <i>Read Size</i> field shall be greater than 0 and less than or equal to 16.
	31:20	Reserved

This Router Operation does not write to the *Data* DWs.

Operation Completion

A Router shall return the *Metadata* and *Status* fields defined in Table 8-44.

Table 8-44. DROM Read Router Completion Metadata and Status

Field	Bit(s)	Description
<i>Metadata</i>	1:0	Reserved
	14:2	Address This field contains the <i>Address</i> value from the Operation Metadata.
	19:15	Read Size This field contains the <i>Read Size</i> value from the Operation.
	31:20	Reserved
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h – 3Fh: Reserved

If this Operation is completed successfully, the Router returns *Read Size* number of Doublewords of Data as shown in Table 8-45.

Table 8-45. DROM Read Router Completion Data

DW	Bit(s)	Description
0	31:0	DW0 The first Doubleword read from DROM at <i>Address</i> .
1	31:0	DW1 The second Doubleword read from DROM at the next address.
...	31:0	...
15	31:0	DW15 The last Doubleword read from DROM at the next address.

8.3.1.2.6 Get NVM Sector Size (Conditional)

Software uses the Get NVM Sector Size Operation to determine the sector size of the Router NVM.

A ~~Device~~ Router ~~may optionally~~shall support the NVM Sector Size Router Operation. ~~A Host Router may optionally support this Router Operation.~~

Operation Initiation

This Router Operation does not write to the *Metadata* field or *Data* DWs.

Operation Completion

A Router shall return the *Metadata* and *Status* fields defined in Table 8-46.

Table 8-46. Get NVM Sector Size Completion Metadata and Status

Field	Bit(s)	Description
<i>Metadata</i>	23:0	Sector Size Equals the sector size of the NVM in bytes. For example, a value of 1000h indicates a sector size of 4KB.
	31:24	Reserved
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h: NVM is not implemented 3h – 3Fh: Reserved

This Router Operation does not return any *Data* DWs.

8.3.1.3 Router Discovery Operations**8.3.1.3.1 Get PCIe Downstream Entry Mapping (Conditional)**

A Connection Manager uses this Operation to retrieve information about the mapping of a PCIe downstream facing port. The mapping information is returned in an entry, where there is one entry per PCIe downstream facing port. Each execution of this Operation retrieves the entry for one PCIe downstream facing port. Entries are returned in increasing order of their Entry Index.

A ~~Device~~ Router shall support the Get PCIe Downstream Entry Mapping Router Operation if it supports PCIe Tunneling. ~~A Host Router may optionally support this Router Operation if it supports PCIe Tunneling.~~ This Router Operation is not applicable for a Router that does not support PCIe tunneling.

Operation Initiation

This Router Operation does not write to the *Metadata* field or *Data* DWs.

Operation Completion

If a Router supports the Get PCIe Downstream Entry Mapping Router Operation, it shall return the *Metadata* and *Status* fields defined in Table 8-47.

Table 8-47. Get PCIe Downstream Entry Mapping Completion Metadata and Status

Field	Bit(s)	Field Name and Description
<i>Metadata</i>	7:0	Total Number of Entries This field indicates the total number of entries. A Host Router that supports PCIe tunneling shall have one entry per Downstream PCIe Adapter. A Device Router that supports PCIe tunneling shall have one entry per PCIe downstream facing port.
	15:8	Entry Index This field indicates the current entry index. The values of this field shall be zero to <i>Total Number of Entries</i> – 1.
	31:16	Reserved
<i>Status</i>	29:24	Status 0h: Operation completed successfully 1h: Operation failed to execute 2h – Fh: Reserved

The first time this Operation is executed after transition to the Enumerated state, a Router shall respond with the entry for Entry Index = 0h. On each subsequent execution of the Operation, the Router shall respond with the next entry (*Entry Index* = 01h, *Entry Index* = 02h, etc.). After the last entry is retrieved, the Router shall restart at the first entry (*Entry Index* = 0h) the next time the Operation is executed.

A Router shall return the entry for a PCIe Downstream mapping in *Data* DW0 and DW1 as defined in Table 8-48.

Table 8-48. Get PCIe Downstream Entry Mapping Completion Data

DW	Bit(s)	Field Name and Description
0	0	Native PCIe Link 0 – Entry is for a PCIe downstream facing port connected to a Downstream PCIe Adapter 1 – Entry is for a PCIe downstream facing port connected through a native PCIe link
	6:1	PCIe Adapter Number If <i>Native PCIe Link</i> is set to 0, this field shall indicate the Adapter Number of the Downstream PCIe Adapter. Otherwise it shall be set to 0.
	14 31:7	Reserved
	<u>15</u>	<u>PCIE Segment ID Valid</u> <u>When set – the PCIE Segment ID field is valid. When not set – the PCIE Segment ID is not used or is set by implementation -specific means.</u>
	<u>23:16</u>	<u>PCIE Segment ID [7:0]</u> <u>The least significant byte of the Segment ID assigned to the PCIe downstream facing port.</u> <u>This field is valid in case the PCIE Segment ID Valid is set to 1. Otherwise this field shall be set to 0.</u>
	<u>31:24</u>	<u>PCIE Segment ID [15:8]</u> <u>This field contains the most significant byte of the Segment ID in case PCIE Segment ID Valid is set and the Segment ID size is 16-bits. Otherwise this field shall be set to 0.</u>
1	15:0	Non-FPB Routing ID The Routing ID value assigned to this PCIe downstream facing port according to the non-FPB addressing scheme. A value of 0 indicates that the non-FPB addressing scheme is not used through this PCIe downstream facing port ,unless both the <i>Non-FPB Routing ID</i> and <i>FPB Routing ID</i> fields are set to zero, which indicates that the non-FPB addressing scheme is used.
	31:16	FPB Routing ID The Routing ID value assigned to this PCIe downstream facing port according to the FPB addressing scheme. A value of 0 indicates that the FPB addressing scheme is not used through this PCIe downstream facing port.
2-15	31:0	Reserved

8.3.1.3.2 Get Capabilities (Conditional)

A Connection Manager uses this Operation to retrieve information about certain Router capabilities. Every execution of this Operation retrieves information about a single capability.

A Router shall support the Get Capabilities Router Operation if it supports any of the capabilities listed in Table 8-51. A Router that supports this Operation shall also support the Set Capabilities Router Operation.

Upon transitioning to the Uninitialized state, a Router shall set any capabilities it reports via the Get Capabilities Operation to their default state as defined in Table 8-51.

Operation Initiation

Table 8-49 defines the contents of the *Metadata* field for a Get Capabilities Router Operation.

Table 8-49. Get Capabilities Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	7:0	Capability Index This field indicates the capability to be read. The value in this field shall not exceed the <i>Max Capability Index</i> .
	31:8	Reserved

This Router Operation does not write to the *Data DWs*.

Operation Completion

A Router that supports the Get Capabilities Operation shall return the *Metadata* field and the *Status* field defined in Table 8-50.

Table 8-50. Get Capabilities Operation Completion Metadata and Status

Field	Bit(s)	Description
<i>Metadata</i>	7:0	Max Capability Index This field indicates the highest Capability Index supported by the Router.
	15:8	Capability Index This field contains the <i>Capability Index</i> value from the Get Capabilities Operation.
	29:16	Reserved
	30	Capability Supported 0b – Capability is not supported 1b – Capability is supported This bit shall be set to 0b for <i>Capability Index</i> = 0.
	31	Capability Enabled 0b – Capability is disabled 1b – Capability is enabled This bit shall be set to 0b for <i>Capability Index</i> = 0.
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h – 3Fh: Reserved

When a Router receives a Get Capabilities Operation with *Capability Index* = 0, it shall return a list of the capabilities that the Router supports and indicate which capabilities are enabled. Capability information is returned in a series of 2-bit entries, where each entry represents a different capability. Each 2-bit entry consists of the following:

- *Capability Supported (SUP)* bit – The entry for capability *n* (*n* = 0 to *Max Capability Index*) to is located in DW $\lfloor n / 16 \rfloor$, bit $2 * [n - 16 * \lfloor n / 16 \rfloor]$. The entry for *Capability Index* = 0 is reserved.
 - The *Capability Supported* bit shall be set to 0b when the capability is not supported.
 - The *Capability Supported* bit shall be set to 1b when the capability is supported.
- *Capability Enabled (ENA)* bit – The entry for capability *n* (*n* = 0 to *Max Capability Index*) to is located in DW $\lfloor n / 16 \rfloor$, bit $\{2 * [n - 16 * \lfloor n / 16 \rfloor] + 1\}$. The entry for *Capability Index* = 0 is reserved.

- The *Capability Enabled* bit shall be set to 0b when the capability is disabled.
- The *Capability Enabled* bit shall be set to 1b when the capability is enabled.

The 2-bit entries are organized as a packed array of Doublewords. The last Doubleword may not necessarily be fully populated. The list of capabilities is returned in the *Data* field and shall be formatted as shown in Figure 8-23.

Figure 8-23. Get Capabilities Operation Data Response for Capability Index 0

[illegible]

The contents of the *Data* DWs returned by the Get Capability Operation for *Capability Index* > 0 are specific to each capability. Table 8-51 lists the capabilities and the number of *Data* DWs returned by each capability.

Table 8-51. List of Capabilities

Capability Index	Capability Name	# of Data DWs returned	Default State	Reference
01h	Hot Plug Failure Indication	0	Disabled	Section 8.3.1.3.2.1
02h	Sequence bit in Notification Packet	0	Disabled	Section 8.3.1.3.2.2
03h	Buffer Allocation Per USB4 Port	0	Disabled	Section 8.3.1.3.2.3
04h	Notification Retry Limit	1	Disabled	Section 8.3.1.3.2.4
05h	CLx Latency Tolerance	0	Disabled	Section 8.3.1.3.2.5
06h – FFh	Reserved	--	--	N/A

8.3.1.3.2.1 Hot Plug Failure Indication

This capability allows a Router to inform the Connection Manager when a Hot Plug Event is detected on a Downstream Facing Port, but none of the Adapters in that USB4 Port succeeds to establish a Link (see Section 6.8.1.1).

This capability does not return any Data DWs.

8.3.1.3.2.2 Sequence Bit in Notification Packet

This capability enables the usage of a Sequence bit in a Notification Packet (see Section 6.4.2.7) and the usage of the Enhanced Notification Acknowledgment Packet (see Section 6.4.2.9).

This capability does not return any Data DWs.

8.3.1.3.2.3 Buffer Allocation Per USB4 Port

This capability allows a Router to request a different buffer allocation per USB4 Port (see Section 5.3.2.1.1).

This capability does not return any *Data DWs*.

8.3.1.3.2.4 Notification Retry Limit

This capability enables to limit the number of retry attempts for Notification Packets and Hot Plug Event Packets that require an Acknowledgement.

This Capability returns a single Data DW as described in the table below:

Table 8-52. Notification Retry Limit Operation Completion (Get) and Data DW (Set)

Field	Bit(s)	Description
<u>Notification Retry Limit</u>	<u>7:0</u>	<u>The value in this field represents the number of retry attempts performed for Notification Packets that require an Acknowledgment.</u> <u>The value of 0 is used for having no retry attempts.</u> <u>Note: Disabling this Capability results in infinite retry attempts.</u>
<u>Reserved</u>	<u>31:8</u>	

8.3.1.3.2.5 CLx Latency Tolerance

This capability allows USB4 Ports to use longer CL0S and CL1 exit times than defined in the standard.

This capability does not return any Data DWs.

8.3.1.3.3 Set Capabilities (Conditional)

A Connection Manager uses this Operation to configure a Router's capabilities. Every execution of this Operation configures a single capability.

A Router shall support the Set Capabilities Router Operation if it supports the Get Capabilities Router Operation. Otherwise, a Router shall not support this Router Operation.

Operation Initiation

Table 8-53 defines the contents of the *Metadata* field for a Set Capabilities Router Operation.

Table 8-538-52. Set Capabilities Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	7:0	Capability Index This field indicates the capability to be written. The values of this field shall not exceed the <i>Max Capability Index</i> .
	8	Enable Capability This bit is used to request that a Capability be enabled or disabled 0b – Router shall disable the Capability 1b – Router shall enable the Capability
	31:9	Reserved

A Router shall enable a capability when all the following conditions are true:

- The Router supports the Get Capabilities Operation and the Set Capabilities Operation.
- The Router supports the capability.
- The Router receives a Set Capabilities Operation with *Capability Index* equal to the index of the capability and *Enable Capability* = 1b.

The *Data DWs* for the Set Capability Operation are specific to each capability. Table 8-54 lists the capabilities and the number of *Data DWs* written by each capability.

Table 8-548-53. List of Capabilities

Capability Index	Capability Name	# of Data DWs written	Reference
01h	Hot Plug Failure Indication	0	Section 8.3.1.3.2.1
02h	Sequence bit in Notification Packet	0	Section 8.3.1.3.2.2
03h	Buffer Allocation Per USB4 Port	0	Section 8.3.1.3.2.3
04h	Notification Retry Limit	1	Section 8.3.1.3.2.4
05h	CLx Latency Tolerance	0	Section 8.3.1.3.2.5
065h – FFh	Reserved	--	N/A

Operation Completion

A Router that supports this Operation shall return the *Status* field defined in Table 8-55.

Table 8-558-54. Set Capabilities Operation Completion Status

Field	Bit(s)	Field Name and Description
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h – 3Fh: Reserved

This Operation does not return any Metadata.

This Operation does not return any *Data DWs*.

8.3.1.3.4 Buffer Allocation Request (Required)

A Router shall support this Router Operation.

The Buffer Allocation Request Router Operation reads the Router's preferences for buffer allocation per Path type.

Operation Initiation

Table 8-56 defines the contents of the *Metadata* field for a Buffer Allocation Request Router Operation.

Table 8-56-55. Buffer Allocation Request Operation Metadata

Field	Bit(s)	Description
<i>Metadata</i>	5:0	Lane Adapter Number If the <i>Buffer Allocation Per USB4 Port</i> capability is enabled, this field contains the Lane 0 Adapter Number queried by the Router Operation. Otherwise this field shall be ignored by the Router.
	31:6	Reserved

This Router Operation does not write to the *Data* DWs.

Operation Completion

A Router shall return *Metadata* and *Status* fields defined in Table 8-57.

Table 8-57-56. Buffer Allocation Request Router Completion Status and Metadata

Field	Bit(s)	Description
<i>Metadata</i>	7:0	Length This field shall be equal to the number of buffer allocation parameters the Router reports. Buffer allocation parameters are defined in Table 8-58.
	13:8	Lane Adapter Number If the <i>Buffer Allocation Per USB4 Port</i> capability is enabled, this field contains the <i>Lane Adapter Number</i> queried by the Router Operation. Otherwise this field shall be set to 0.
	31:14	Reserved
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h – 3Fh: Reserved

If this Operation is completed successfully, the Router returns *Length* Doublewords of Data where each DW has the structure shown in Table 8-58. If the *Buffer Allocation Per USB4 Port* capability is enabled, the return *Data* DWs shall correspond to the queried *Lane Adapter Number* which was set in the *Metadata* when the Router Operation was initiated. If the *Buffer Allocation Per USB4 Port* capability is disabled, the return *Data* DWs shall correspond to all Lane Adapters.

Table 8_588-57. Buffer Allocation Request Router Completion Data DW Structure

Bit(s)	Description
15:0	Parameter Index 0h: Reserved 1h: baMaxUSB3GenX 2h: baMinDPaux 3h: baMinDPmain 4h: baMaxPCIE 5h: baMaxHI 6h: baMaxUSB3GenT 7h-FFFFh: Reserved
31:16	Requested Buffer Allocation This field contains the number of buffers requested for the corresponding buffer allocation parameter indicated by the <i>Parameter Index</i> field.

8.3.1.3.5 Get Container-ID (Conditional)

A USB4 Hub shall support this Router Operation. A USB4 Peripheral Device with an Internal USB3 Hub shall support this Router Operation. A USB4 Peripheral Device that does not contain an Internal USB3 Hub may optionally support this Router Operation. This Router Operation is not applicable for USB4 Hosts. The Get Container-ID Router Operation reads the Container-ID value which allows software to associate a Router with its internal USB SuperSpeed Plus hub. The return value for the Container-ID shall be identical to the Container-ID read from the internal USB SuperSpeed Plus hub.

Operation Initiation

This Router Operation does not write to the *Metadata* field. It does not write to the *Data* DWs.

Operation Completion

This Router Operation does not return Metadata.

A Router that supports this operation shall return *Status* field defined in Table 8_59.

Table 8_598-58. Get Container-ID Router Completion Status

Field	Bit(s)	Description
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h – 3Fh: Reserved

If this Operation is completed successfully, the Router returns four Doublewords of Data as shown in Table 8_60.

Table 8_608-59. Get Container-ID Router Completion Data DW Structure

DW	Bit(s)	Description
0	31:0	Container-ID[31:0]
1	31:0	Container-ID[63:32]
2	31:0	Container-ID[95:64]
3	31:0	Container-ID[127:96]
4-15	31:0	Reserved

8.3.1.3.6 Get Connectors Information (Conditional)

A Connection Manager uses this Operation to retrieve information about the Downstream facing USB Type-C ports and native DP connectors (referred to collectively as “Connectors”) that are capable of being connected to a DP OUT Adapter. The information is returned as a set of one or more entries, where the Router contains one entry per Connector.

A Device Router shall support this Router Operation if it supports DPRX Discovery through the Partial Implementation option. This Router Operation is not applicable for a Host Router. A Device Router that supports DPRX Discovery through the Full Implementation option may optionally support this Router Operation.

Operation Initiation

This Router Operation does not write to the *Metadata* field or *Data* DWs.

Operation Completion

If a Router supports the Get Connectors Information Router Operation, it shall return the *Metadata* and *Status* fields defined in Table 8-61.

Table 8-61~~8-60~~. Get Connectors Information Completion Metadata and Status

Field	Bit(s)	Field Name and Description
<i>Metadata</i>	7:0	Total Number of Entries This field indicates the total number of entries.
	15:8	Entry Index This field indicates the current entry index. The values of this field shall be zero to <i>Total Number of Entries</i> – 1.
	31:16	Reserved
<i>Status</i>	29:24	Status 0h: Operation completed successfully 1h: Operation failed to execute 2h – Fh: Reserved

The first time this Operation is executed after transition to the Enumerated state, a Router shall respond with the entry for Entry Index = 0h. On each subsequent execution of the Operation, the Router shall respond with the next entry (*Entry Index* = 01h, *Entry Index* = 02h, etc.). After the last entry is retrieved, the Router shall restart at the first entry (*Entry Index* = 0h) the next time the Operation is executed.

A Router shall return the entry for a connector in *Data* DW0 through DW2 as defined in Table 8-62.

Table 8-628-61. Get Connectors Information Completion Data

DW	Bit(s)	Field Name and Description
0	3:0	Connector Number This field shall be set to the Connector number that this entry describes.
	5:4	Reserved
	6	Connected This field shall be set to indicate the connection status of this Connector: 0 – The Connector is not connected to an Adapter 1 – The Connector is connected to a DP OUT Adapter or a DP OUT AUX Adapter
	7	HPD Status This field shall be set to indicate the status of the HPD: 0 – HPD is low 1 – HPD is high (Monitor is connected)
	8	USB4 Capable This field shall be set to indicate if the Connector supports USB4 0 – Not supported 1 – Supported
	15:9	Reserved
	21:16	Adapter Number This field shall be set to the Adapter Number of the Adapter that is connected to the Connector. This field shall be set to 0h if the <i>Connected</i> bit is set to 0b.
	31:22	Reserved
1-2	63:0	Connectivity This field represents the possible connectivity for this Connector. When a bit in this field is set to 1b, it indicates that the DP OUT Adapter or DP OUT AUX Adapter with the same index as the bit can be connected to this Connector. When a bit is set to 0b, it indicates that the DP OUT Adapter or DP OUT AUX Adapter cannot be connected to this Connector.
3-15	31:0	Reserved

8.3.1.4 Port Control Operations**8.3.1.4.1 Block Sideband Port Operations (Optional)**

A Router may optionally support the Block Sideband Port Operations Router Operation.

The Block Sideband Port Operations Router Operation disables Port Operations when initiated by Transactions over the Sideband Channel. After receiving a Block Sideband Port Operations Router Operation, a Router shall change the access type for SB Registers 8, 9 and 18 in all its Ports from RW to RO when accessed by Sideband Transactions. Note that these registers are still RW for local accesses done by Connection Manager as described in Section 4.1.1.3.2.

Operation Initiation

This Router Operation does not write to the *Metadata* field. It does not write to the Data DWs.

Operation Completion

A Router that supports this Operation shall return the *Status* field defined in Table 8-63.

Table 8-63~~8-62~~. Block Sideband Port Operation Completion Status

Field	Bit(s)	Description
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h – Fh: Reserved

8.3.1.4.2 Unblock Sideband Port Operation (Conditional)

A Router may optionally support the Unblock Sideband Port Operation Router Operation. If a Router supports the Block Sideband Port Operations Router Operation, it shall support this Router Operation.

The Unblock Sideband Port Operation Router Operation enables Port Operations when initiated by Transactions over the Sideband Channel. After receiving an Unblock Sideband Port Operations Router Operation, the Router shall change the access type for SB Registers 8, 9 and 18 from RO to RW when accessed by Sideband Transactions.

Operation Initiation

This Router Operation does not write to the *Metadata* field. It does not write to the Data DWs.

Operation Completion

A Router that supports this Operation shall return the *Status* field defined in Table 8-64.

Table 8-64~~8-63~~. Unblock Sideband Port Operation Completion Status

Field	Bit(s)	Description
<i>Status</i>	29:24	Status 0h: Router Operation completed successfully 1h: Router Operation failed to execute 2h – Fh: Reserved

8.3.2 Port Operations

A Connection Manager uses registers 8 (Opcode), 9 (Metadata), and 18 (Data) in the SB Register Space of a USB4 Port to initiate a Port Operation. Section 4.1.1.3.2 describes how a Connection Manager writes to SB Register Space. A Connection Manager uses the following flow to issue a Port Operation:

1. The Connection Manager writes to the Metadata register in the SB Register Space of the target USB4 Port.
2. The Connection Manager writes to the Data register in the SB Register Space of the target USB4 Port.
3. The Connection Manager writes to the Opcode register in the SB Register Space of the target USB4 Port.

**CONNECTION MANAGER NOTE**

If an Operation does not write to the Metadata register in the SB Register Space, then a Connection Manager shall set it to 0 when issuing the Operation.

If an Operation does not write to any bytes in the Data register in the SB Register Space, then a Connection Manager shall write 0 to these bytes when issuing the Operation.

A Connection Manager shall verify the successful completion of a write to the SB Register Space of the target USB4 Port before proceeding with the next write to SB Register Space. A Connection Manager verifies the results of a Port Operation by issuing a read to the Opcode register in the SB Register Space of the target USB4 Port. The Connection Manager also reads any Completion Metadata and Completion Data. If the Opcode Register = “!CMD” or “ERR ” the contents of the Metadata and Data registers are invalid and shall be ignored.

8.3.2.1 Port Operation Completion

When the Opcode register in SB Register Space is written, a USB4 Port shall execute the Port Operation associated with the Opcode register using the information in the Metadata and Data registers.

After executing the Port Operation, the USB4 Port updates the Opcode, Metadata, and Data register as follows:

- If the USB4 Port successfully completed the Port Operation, it shall set the Opcode register to 0. The USB4 Port shall update the Metadata register with completion metadata (if the Port Operation is defined to return metadata), and the Data register with completion data (if the Port Operation is defined to return data).
- Else, if the Port Operation is not supported, the USB4 Port shall set the Opcode register to a FourCC value of “!CMD” (444D4321h). The USB4 Port may update the Metadata and Data registers. However, any updates will be ignored by the Connection Manager.
- Else, the USB4 Port shall set the Opcode register to a FourCC value of “ERR ” (20525245h) to indicate that the Port Operation is supported, but could not be completed. The USB4 Port may update the Metadata and Data registers. However, any updates will be ignored by the Connection Manager.
- The Router shall send the Connection Manager a Notification Packet with *Event Code* = POP_CMPLT. See Section 6.4.2.7 for more information on Notification Packets.

A Ver. 2 Re-timer sends an ELT_OpDone Transaction after it completes a Port Operation (see Section 4.1.1.2.2). When a Router receives an ELT_OpDone Transaction, it shall send the Connection Manager a Notification Packet with *Event Code* = POP_CMPLT.

**CONNECTION MANAGER NOTE**

A Connection Manager verifies the results of a Port Operation by issuing a read to the Opcode register in the SB Register Space of the target Port. The Connection Manager also reads any Completion Metadata and Completion Data.

A Connection Manager shall only issue a Port Operation to a USB4 Port after the previous Port Operation for that USB4 Port completes execution.

Table 8-65 lists the Port Operations defined for a USB4 Port. A USB4 Port may also support vendor specific Opcodes. The second byte (Opcode 1) of a vendor specific Opcode shall have a value between 61h and 7Ah (inclusive) to distinguish from Opcodes defined in this specification. All unused Opcodes (except for vendor specific Opcodes) are reserved and shall not be used.

Table 8-658-64. List of Port Operations

Port Operation	Opcode ¹	Operation		Completion		Reference
		Metadata DW	Data DWs	Metadata DW	Data DWs	
SET_TX_COMPLIANCE	TXCM (4D435854h)	1	0	0	0	Section 8.3.2.2.1
SET_RX_COMPLIANCE	RXCM (4D435852h)	1	0	0	0/1	Section 8.3.2.2.2
START_BER_TEST	SBER (52454253h)	1	0	0	0	Section 8.3.2.2.3
END_BER_TEST	EBER (52454245h)	1	0	0	2	Section 8.3.2.2.4
END_BURST_TEST	BBER (52454242h)	1	0	0	3	Section 8.3.2.2.5
READ_BURST_TEST	RBER (52454252h)	1	0	0	3	Section 8.3.2.2.6
ENTER_EI_TEST	EEIT (54494545h)	1	0	0	0	Section 8.3.2.2.7
LFPS_TEST	LFPT (5450464Ch)	1	0	0	0	Section 8.3.2.2.8
SET_LINK_TYPE	LNKT (544B4E4Ch)	1	0	0	0	Section 8.3.2.2.9
ROUTER_OFFLINE_MODE	LSEN (4E45534Ch)	1	0	0	0	Section 8.3.2.3.1
ENUMERATE_RE-TIMERS	ENUM (4D554E45h)	0	0	0	0	Section 8.3.2.3.2
FEC_ERRORS_STAT	FERS (53524546h)	1	0	0	7	Section 8.3.2.3.3
READ_LANE_MARGIN_CAP	RDCP (50434452h)	0	0	0	3	Section 8.3.2.4.1
RUN_HW_LANE_MARGINING	RHMG (474D4852h)	1	0	0	2	Section 8.3.2.4.2
RUN_SW_LANE_MARGINING	RSMG (474D5352h)	1	0	0	1	Section 8.3.2.4.3
READ_SW_MARGIN_ERR	RDSW (57534452h)	0	0	1	0	Section 8.3.2.4.4
<u>QUERY CLX LATENCY TOL</u>	<u>SCLT</u>	<u>1</u>	<u>0</u>	<u>0</u>	<u>0</u>	<u>Section 8.3.2.5</u>
<u>SET CLX LATENCY TOL</u>	<u>QCLT</u>	<u>0</u>	<u>0</u>	<u>4</u>	<u>0</u>	<u>Section 8.3.2.6</u>
Notes:						
1. Byte 0 of the Opcode is the rightmost byte of the hexadecimal representation.						

8.3.2.2 Compliance Port Operations

The Port Operations defined in the subsections below are used to bring transmitters and receivers into compliance mode and to execute bit error tests, burst error rate tests, clock switch tests, TxFFE equalization tests, Electrical Idle tests, and Return Loss tests.

The following is an example Port Operation sequence used for compliance testing. It assumes that compliance software interfaces with test equipment that includes a PD controller (or its equivalent) and a Sideband Channel controller (or its equivalent).

Note: In some Compliance test flows the compliance software may send several Port Operations without a Disconnect between them.

For Gen 2 and Gen 3 transmitter compliance testing:

1. Compliance software disconnects the Link to be tested (via the PD Controller embedded in the test equipment).
2. Compliance software sets a USB4 Link or TBT3-Compatible Link (to the PD controller).
3. Compliance software disables AT Transactions in the USB4 Port at the test equipment side in order to delay Lane Initialization (see step 8 below).
4. Compliance software connects the Link to be tested (via the PD Controller).
5. The PD Controller sets a USB4 Link or TBT3-Compatible Link.
6. Compliance software issues a SET_TX_COMPLIANCE Port Operation to the Router and to each On-Board Re-timer in the Router Assembly under test to set the transmit parameters.
7. Compliance software sets the USB4 Port at the test equipment side to either support Gen 3 or to not support Gen 3.
8. Compliance software enables AT Transactions in the USB4 Port at the test equipment side in order to proceed with Lane Initialization.
 - Compliance software disabled RS-FEC during compliance testing.
9. Compliance software performs TxFFE equalization tests with the component next to the USB Type-C connector.
 - Compliance software selects the Preset values for the receiver at the test equipment side.
 - Compliance software determines when to complete the test by setting the *Rx Lock* bit to 1b at the test equipment side.
10. Compliance software performs clock switch test with the On-Board Re-timer next to the USB Type-C connector.
 - Compliance software sets the *Clock Switch Done* bit to 1b at the test equipment side to initiate a clock switch by the Re-timer.
11. Once the Lane under test is up, compliance software performs checks on the pattern received from the Router Assembly under test.
12. Once the transmitter compliance test is done, compliance software disconnects the Link under test.

For Gen 4 transmitter compliance testing:

1. Compliance software disconnects the Link to be tested (via the PD Controller embedded in the test equipment).
2. Compliance software sets a USB4 Link (to the PD controller).
3. Compliance software disables AT Transactions in the USB4 Port at the test equipment side in order to delay Lane Initialization (see Step 8 below).
4. Compliance software connects the USB4 Link to be tested (via the PD Controller).

5. The PD Controller sets a USB4 Link.
6. If the Router Assembly supports an Asymmetric Link with 3 transmitters, the compliance software issues a SET_LINK_TYPE Port Operation to the Router to set a Link with 3 transmitters.
7. Compliance software issues a SET_TX_COMPLIANCE Port Operation to the Router or to the On-Board Re-timer adjacent to the USB Type-C Connector in the Router Assembly under test to set the transmit parameters:
 - Each transmitter receives a different Port Operation with a different Pattern.
 - The transmitters in the Router receive Port Operations with the *SSC* bit set to 1b.
 - The transmitters in the Re-timers receive Port Operations with *Forward* bit set to 0b.
8. Compliance software enables AT Transactions in the USB4 Port at the test equipment side in order to proceed with Lane Initialization.
9. Compliance software performs TxFFE equalization tests with the component next to the USB Type-C connector:
 - Compliance software selects the Preset values for the receiver at the test equipment side.
10. Once the Lane under test is up, compliance software performs checks on the pattern received from the Router Assembly under test.
11. Once the transmitter compliance test is done, compliance software disconnects the Link under test.

For Gen 2 or Gen 3 receiver compliance testing:

1. Compliance software disconnects the Link to be tested (via the PD Controller embedded in the test equipment).
2. Compliance software sets a USB4 Link or TBT3-Compatible Link (to the PD controller).
3. Compliance software disables AT Transactions in the USB4 Port at the test equipment side in order to delay Lane Initialization (see step 8 below).
4. Compliance software connects the Link to be tested (via the PD Controller).
5. The PD Controller sets a USB4 Link or TBT3-Compatible Link.
6. Compliance software issues a SET_RX_COMPLIANCE Port Operation to the Router under test.
7. Compliance software sets the USB4 Port at the test equipment side to either support Gen 3 or to not support Gen 3.
8. Compliance software enables AT Transactions in the USB4 Port at the test equipment side in order to proceed with Lane Initialization.
 - Compliance software disabled RS-FEC during compliance testing.
9. Compliance software performs TxFFE equalization test with the component next to the USB Type-C connector.
10. Compliance software waits for completion of Lane Initialization.

- Compliance software performs a bit error rate test, a burst error rate test, or a clock switch test as described below.

For Gen 4 receiver compliance testing:

1. Compliance software disconnects the Link to be tested (via the PD Controller embedded in the test equipment).
2. Compliance software sets a USB4 Link (to the PD controller).
3. Compliance software disables AT Transactions in the USB4 Port at the test equipment side in order to delay Lane Initialization (see Step 9 below).
4. Compliance software connects the Link to be tested (via the PD Controller).
5. The PD Controller sets a USB4 Link.
6. If the Router Assembly supports an Asymmetric Link with 3 receivers, the compliance software issues a SET_LINK_TYPE Port Operation to the Router to set a Link with 3 receivers.
7. Compliance equipment starts sending PRBS11 to the receiver under test and issues a SET_RX_COMPLIANCE Port Operation with the *Transmitter State* field set to 000b to the component next to the USB Type-C connector.
8. Compliance software enables AT Transactions in the USB4 Port at the test equipment side in order to proceed with Lane Initialization.
9. Compliance software performs TxFFE equalization flow with the receiver under test in the component next to the USB Type-C connector.
10. Compliance software periodically issues a SET_RX_COMPLIANCE Port Operation with *Transmitter State* field set to 000b to the component next to the USB Type-C connector. When the *Receiver State* field in the Port Operation Completion is set to 001b, continue to the next step.
11. Compliance equipment starts sending PRTS7 to the receiver under test and issues a SET_RX_COMPLIANCE Port Operation with the *Transmitter State* field set to 010b to the component next to the USB Type-C connector.
12. Compliance software continues performing the TxFFE equalization flow with the receiver under test in the component next to the USB Type-C connector.
13. If there are Re-timers on the Router Assembly:
 - a. Compliance software periodically issues a SET_RX_COMPLIANCE Port Operation with the *Transmitter State* field set to 010b to the component next to the USB Type-C connector. When the *Receiver State* field in the Port Operation Completion is set to 010b, continue to next step.
 - b. Compliance software issues a SET_RX_COMPLIANCE Port Operation with the *Clock Switch* field set to 1b, first to the Re-timer adjacent to the USB Type-C Connector and later to an internal Re-timer (if present).
14. Compliance software periodically issues a SET_RX_COMPLIANCE Port Operation with the *Transmitter State* field set to 010b to the Router. When the *Receiver State* field in the Port Operation Completion is set to 010b, continue to the next step.

15. Compliance equipment starts sending Pre-Coded PRTS19 to the receiver under test and issues a SET_RX_COMPLIANCE Port Operation with the *Transmitter State* field set to 011b

Note: The receivers within a USB4 Port are tested one at a time. Therefore, if an Asymmetric Link with 3 receivers is supported by the Router Assembly, then Rx2 is tested without having a signal present at the inputs of Rx0 and Rx1.

For bit error rate test:

1. Compliance software issues a START_BER_TEST Port Operation to start a receiver compliance test using the chosen BER test pattern. The Operation may be issued to a Router, an On-Board Re-timer, or to multiple components.
2. Compliance software issues an END_BER_TEST Port Operation to stop a running receiver BER test pattern and retrieve the results of the test. The Operation may be issued to a Router, an On-Board Re-timer, or to multiple components.
3. Once the test is completed, compliance software disconnects the Link under test.

For Gen 2/3 Link burst error rate test:

1. Compliance software issues a START_BER_TEST Port Operation to start a receiver compliance test using the chosen BER test pattern. The Operation may be issued to a Router, an On-Board Re-timer, or to multiple components.
2. Compliance software may issue a READ_BURST_TEST Port Operation to read the counters involved in the test. The Operation may be issued multiple times. The Operation may be issued to a Router, an On-Board Re-timer, or to multiple components.
3. Compliance software issues an END_BURST_TEST Port Operation to stop a running receiver burst error rate test pattern and retrieve the results of the test. The Operation may be issued to a Router, an On-Board Re-timer, or to multiple components.
4. Once the test is completed, compliance software disconnects the Link under test.

For clock switch test:

1. Compliance software issues a START_BER_TEST Port Operation to the Adapter in the component next to the USB Type-C connector.
2. Compliance software sets the appropriate test conditions such as emulating a clock switch. For a Gen 4 Link, the compliance equipment will send either TS2.clksw (if supported) or PRTS7.
3. Compliance software issues an END_BER_TEST Port Operation to the component next to the USB Type-C connector.
4. Once the test is completed, compliance software disconnects the Link under test.
5. Software transitions the Router to the Uninitialized state.

For transmitter electrical idle test:

1. Compliance software disconnects the Link to be tested (via the PD Controller embedded in the test equipment).
2. Compliance software connects the Link to be tested (via the PD Controller).
3. Compliance software waits for completion of Lane Initialization.

4. Compliance software issues an ENTER_EI_TEST Port Operation to the component next to the USB Type-C connector.
5. Once the test is completed, compliance software disconnects the Link under test.

For receiver return loss test:

1. Compliance software disconnects the Link to be tested (via the PD Controller embedded in the test equipment).
2. Compliance software sets a USB4 Link or TBT3 compatible Link (to the PD controller).
3. Compliance software connects the Link to be tested (via the PD Controller).
4. The PD Controller sets a USB4 Link or TBT3-compatible Link.
5. Compliance software sets the USB4 Port at the test equipment side to either support Gen 3 or to not support Gen 3.
6. Compliance software enables AT Transactions in the USB4 Port at the test equipment side in order to proceed with Lane Initialization.
7. Compliance software polls the *Rx Enable* bit in the Lane under test. When the *Rx Enable* bit is 1b, compliance software performs the return loss test.
8. Once the test is completed, compliance software disconnects the Link under test.

For LFPS test:

1. Compliance software disconnects the Link to be tested (via the PD Controller embedded in the test equipment).
2. Compliance software sets a USB4 Link or TBT3-Compatible Link (to the PD controller).
3. Compliance software disables AT Transactions in the USB4 Port at the test equipment side in order to delay Lane Initialization (see step 8 below).
4. Compliance software connects the Link to be tested (via the PD Controller).
5. The PD Controller sets a USB4 Link or TBT3-Compatible Link.
6. Compliance software sets the USB4 Port at the test equipment side to either support Gen 3 and/or Gen 4 or to not support Gen 3 and/or Gen 4.
7. Compliance software enables AT Transactions in the USB4 Port at the test equipment side in order to proceed with Lane Initialization. Compliance software does not send the Broadcast RT Transaction to prevent High-Speed activation.
8. Compliance software issues a LFPS_TEST Port Operation to the Router/Re-timer adjacent to the USB Type-C connector.
9. Once the transmitter under test is up, compliance software performs checks on the pattern received from the Router Assembly under test.
10. Once the LFPS transmitter compliance test is done, compliance software disconnects the Link under test.

Note: Compliance Operations do not change the Lane Initialization flow unless specifically written otherwise.

8.3.2.2.1 SET_TX_COMPLIANCE (Required)

The SET_TX_COMPLIANCE Port Operation sets the transmit parameters for a USB4 Port.

A USB4 Port shall support the SET_TX_COMPLIANCE Port Operation.

Operation Initiation

This Port Operation does not have Operation Data. The Operation Metadata for the SET_TX_COMPLIANCE Port Operation is defined in Table 8-66.

Table 8-66~~8-65~~. SET_TX_COMPLIANCE Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. For a Router: This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port. For a Re-timer: 0h: Target is the USB4 Port whose SB Register Space is written to. 1h: Target is the USB4 Port whose SB Register Space is not written to.
	8:6	Adapter – Identifies the affected Adapter(s) within the USB4 Port. 000b: TX0 001b: TX1 010b: TX2 (only applies to a Port that supports Asymmetric Link with 3 Tx) 111b: All Adapters All other values are reserved. When this field is set to 111b and the Link is Gen 2/3, the pattern on the Lanes shall have skew between 16 UI and 128 UI.
	12:9	Pattern – Sets the transmitting pattern. 0000b: PRBS31 – a polynomial $G(x) = x^{31} + x^{28} + 1$ shall be used (Gen 2 or Gen 3 only). 0001b: PRBS15 – a polynomial $G(x) = x^{15} + x^{14} + 1$ shall be used (Gen 2 or Gen 3 only). 0010b: PRBS9 – a polynomial $G(x) = x^9 + x^5 + 1$ shall be used (Gen 2 or Gen 3 only). 0011b: PRBS7 – a polynomial $G(x) = x^7 + x^6 + 1$ shall be used (Gen 2 or Gen 3 only). 0100b: SQ2 – a repeating pattern of bits “101010...” (Gen 2 or Gen 3 only). 0101b: SQ4 – a repeating pattern of bits where the repeating pattern is 2 copies of 1b followed by 2 copies of 0b (“1100...” (Gen 2 or Gen 3 only)). 0110b: SQ32 – a repeating pattern of bits where the repeating pattern is 16 copies of 1b followed by 16 copies of 0b (Gen 2 or Gen 3 only). 0111b: SQ128 – a repeating pattern of bits where the repeating pattern is 64 copies of 1b followed by 64 copies of 0b (Required for Gen 2 and Gen 3, Optional for Gen 4). 1000b: PRBS11 – a polynomial $G(x) = x^{11} + x^9 + 1$ shall be used (Gen 4 only). 1001b: PRTS7 – a polynomial $G(x) = 2x^7 + x^2 + 1$ over GF(3) shall be used (Gen 4 only). 1010b: PRTS19 – a polynomial $G(x) = 2x^{19} + x^2 + 1$ over GF(3) shall be used (Gen 4 only). 1011b: STAIRS112 – Repeating 448-trit pattern with a sequence of {0t, 1t, 2t, 1t} values each 112UI in duration shall be used (Gen 4 only). 1100b: SQ224 – a repeating pattern of trits where the repeating pattern is 112 copies of 0t followed by 112 copies of 2t (Gen 4 only) – optional. 1111b: <u>Router - SLOS1, Re-timer WAKE1.0</u> (Gen 2 or Gen 3 only) <u>- optional</u> . For Example: PRBS7 equals 1000 0011 0000 1010 0011 1100 1000 1011 0011 1010 1001 1111 0100 0011 1000 1001 0011 0110 1011 0111 1011 0001 1010 0101 1101 1100 1100 1010 1011 1111 1000 000b STAIRS112 equals a repetition of the following 448 trits: 0000...0001111...1112222...2221111...111 (Gen 4 only) All other values are reserved. Note: The initial seeds for the PRBS11, PRTS7 and PRTS19 patterns are listed in Table 4-66. Note: On-board Re-timer that supports Gen 4 will implement SQ128 and/or SQ224
	16:13	Preset – Bits [3:0] of the Preset number for TxFFE parameters at the transmitter (see Table 3-4 for Gen 2 and Gen 3 or Table 3-24 for Gen 4).

DW	Bit(s)	Field Name and Description
	17	Set Modifications – Enables non-default values for Preset and for Modifications. 0b: Load default TxFFE parameters and ignore the <i>Modifications</i> field. 1b: Load TxFFE parameters from the <i>Preset</i> field and load any signal shaping parameters based on the <i>Modifications</i> field.
	25:18	Modifications – Sets other signal shaping parameters. Bit 0: Disable de-emphasis (0b), or enable de-emphasis (1b). Bit 1: Disable pre-shoot (0b), or enable pre-shoot (1b). All other bits are reserved.
	27:26	Gen 4 Preset – Bits [5:4] of the Preset number for Gen 4 TxFFE parameters at the transmitter (see Table 3-24 for Gen 4). This field only applies to a Gen 4 Link. It shall be set to 00b for a Gen 2 or Gen 3 Link.
	28	SSC/Forward – Determines if SSC/Forward is activated or not. For a Router: 0b: SSC shall be disabled. 1b: SSC shall be activated. For a Re-timer (Gen 4 Link): 0b: Re-timer generates pattern and prevents the transition to Forwarding state. 1b: Re-timer does not prevent the transition to Forwarding state. This field shall affect all enabled transmitters, not only the transmitter specified in the <i>Adapter</i> field of the Operation.
	31:29	Reserved

Operation Completion

After receiving a SET_TX_COMPLIANCE Port Operation, a USB4 Port is in TX Compliance mode and shall disable the transition from Training state to CLd state due to timeouts defined in Section 4.2.1.3.3. When the USB4 Port detects SBRX at logical low for tDisconnectRx, it is no longer in TX Compliance mode, and it shall re-enable the transition from Training state to CLd state due to timeouts.

If the established Link is Gen 4, a USB4 Port that is not adjacent to a USB Type-C connector shall start transmitting the requested Pattern on the transition to CL0 state. A USB4 Port that is adjacent to a USB Type-C connector shall start transmitting the requested Pattern when enabling its transmitters (instead of Gen 4 TS1) after both detecting and transmitting a Broadcast RT Transaction, without the LFPS handshake.

Note: Some of the transitions in the Training Sub-State machine are affected by the SET_TX_COMPLIANCE Port Operation. See section 4.2.1.3.2.2.

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

8.3.2.2.2 SET_RX_COMPLIANCE (Required)

The SET_RX_COMPLIANCE Port Operation sets a receiver to compliance test. The Operation Metadata for the SET_RX_COMPLIANCE Port Operation is defined in Table 8-67.

A USB4 Port shall support the SET_RX_COMPLIANCE Port Operation.

After receiving a SET_RX_COMPLIANCE Port Operation, a USB4 Port is in RX Compliance mode and shall disable the transition from Training state to CLd state due to timeouts defined in Section 4.2.1.3.3. When the USB4 Port detects SBRX at logical low for tDisconnectRx, it is no longer in RX Compliance mode, and it shall re-enable the transition from Training state to CLd state due to timeouts. After receiving a SET_RX_COMPLIANCE Port Operation, A USB4 Port operating at Gen 4 speed shall enable its receivers without requiring an LFPS handshake.

Note: Some of the transitions in the Training Sub-State machine are affected by the SET_RX_COMPLIANCE Port Operation. See Section 4.2.1.3.2.2.

Operation Initiation

This Port Operation does not have Operation Data.

Table 8-67~~8-66~~. SET_RX_COMPLIANCE Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. For a Router: This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port. For a Re-timer: 0h: Target is the USB4 Port whose SB Register Space is written to. 1h: Target is the USB4 Port whose SB Register Space is not written to.
	8:6	Adapter – Identifies the affected Adapter within the USB4 Port. 000b: RX0 001b: RX1 010b: RX2 (only applies to a Port that supports Asymmetric Link with 3 Rx) All other values are reserved.
	11:9	Transmitter State – This field indicates the transmitter (Test Equipment) status. 000b: Transmitter is sending PAM2 signaling without SSC 001b: Transmitter is sending PAM2 signaling with SSC (Gen 2 and Gen 3 only) 010b: Transmitter is sending PAM3 signaling without SSC 011b: Transmitter is sending PAM3 signaling with SSC and Pre-Coding activated All other values are reserved
	12	Clock Switch – This field indicates when a Re-timer can transition to Forwarding state. For a Router: This field is reserved. For a Re-timer (Gen 4): 0h: Re-timer does not transition to Forwarding state in the Router-facing direction. 1h: Re-timer will transition to Forwarding state in the Router-facing direction if all other conditions are met.
	31:13	Reserved

Operation Completion

The Completion for this Operation does not have Completion Metadata.

For a Gen 4 Link, after receiving this Port Operation, the USB4 Port shall update the Completion Data as defined in Table 8-68.

Table 8-68~~8-67~~. SET_RX_COMPLIANCE Operation Data (Gen 4 Link Only)

DW	Bit(s)	Field Name and Description
0	3:0	Receiver State – This field contains a status of the receiver state: 000b: Receiver is not ready for PAM3 001b: Receiver is ready for PAM3 010b: <u>For Router:</u> Receiver is ready for SSC activation <u>For Re-timer:</u> <u>Re- timer is ready for Clock Switch</u> All other values are reserved

	31:4	Reserved
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A Gen 2 or Gen 3 Link does not have Completion Data.

8.3.2.2.3 START_BER_TEST (Required)

The START_BER_TEST Port Operation starts a receiver compliance test using a chosen BER test pattern. The Operation Metadata for the START_BER_TEST Port Operation is defined in Table 8-69.

A USB4 Port shall support the START_BER_TEST Port Operation.

After receiving this Port Operation, a USB4 Port shall do the following for the Adapter targeted by the Operation:

1. Lock the receiver associated with the Adapter on the BER test pattern defined in the Operation Metadata.
2. Set the *DW Count*, *Bit Error Count*, *Error Capture Count*, and *Burst Restart Count* counters to 0.
3. Continue running the BER test pattern until an END_BER_TEST or an END_BURST_TEST Port Operation is received.



CONNECTION MANAGER NOTE

The next Port Operation after a START_BER_TEST Port Operation shall be an END_BER_TEST Port Operation or END_BURST_TEST Port Operation. A Connection Manager shall not initiate another Port Operation while a BER test pattern is running.



IMPLEMENTATION NOTE

This Port Operation is used in the Electrical Compliance to test the Port's receiver. Part of the tests are to verify the Port's receiver can continue meeting the electrical requirements after Clock Switch. If the Port's receiver might lose lock during Clock Switch, it should be able to lock again on the Pattern it was instructed. While the Port's receiver is not locked, it should count all received data as errors. The detection of lock and loss of lock is implementation specific. A possible implementation for pattern lock detection can be receiving at least 100 consecutive trits (in Gen4)/bits (in Gen2 and Gen3) that meet the pseudo random sequence. A possible implementation for pattern loss-of-lock detection can be more than quarter trit/bit errors within a window of at least 500 trits/bits, after pattern lock was originally obtained.

Operation Initiation

This Port Operation does not have Operation Data.

Table 8-698-68. START_BER_TEST Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. For a Router: This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port. For a Re-timer: 0h: Target is the USB4 Port whose SB Register Space is written to. 1h: Target is the USB4 Port whose SB Register Space is not written to.

DW	Bit(s)	Field Name and Description
	8:6	Adapter – Identifies the affected Adapter within the USB4 Port. 000b: RX0 001b: RX1 010b: RX2 (only applies to Port that supports Asymmetric Link with 3 Rx) All other values are reserved.
	12:9	Pattern – Sets the transmitting pattern. Gen 2 and Gen 3 patterns: 0000b: PRBS31 0001b: PRBS15 0010b: PRBS9 0011b: PRBS7 0100b: SQ2 (optional) 0101b: SQ4 (optional) 0110b: SQ32 (optional) Gen 4 patterns: 1000b: PRBS11 1001b: PRTS7 1010b: PRTS19 with Pre-Coding 1011b: PRTS19 without Pre-Coding 1100b: TS2.clksw (optional, see Note 1) All other values are reserved.
	31:13	Reserved
Notes: 1. If TS2.clksw pattern is not supported, the clock switch certification test will use PRTS7 instead.		

Operation Completion

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

8.3.2.2.4 END_BER_TEST (Required)

The END_BER_TEST Port Operation stops a running receiver BER test pattern. The Operation Metadata for the END_BER_TEST Port Operation is defined in Table 8-70.

A USB4 Port shall support the END_BER_TEST Port Operation.

Operation Initiation

This Port Operation does not have Operation Data.

Table 8-70~~8-69~~. END_BER_TEST Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. For a Router: This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port. For a Re-timer: 0h: Target is the USB4 Port whose SB Register Space is written to. 1h: Target is the USB4 Port whose SB Register Space is not written to.

	8:6	Adapter – Identifies the affected Adapter within the USB4 Port. 000b: RX0 001b: RX1 010b: RX2 (only applies to a Port that supports Asymmetric Link with 3 Rx) All other values are reserved.
	31:9	Reserved

Operation Completion

After receiving this Port Operation, a USB4 Port shall stop the *DW/Symbol Count* and *Bit/Trit Error Count* counters associated with the Adapter in the Operation Metadata and shall update the Completion Data as defined in Table 8-71.

The Completion for this Operation does not have Completion Metadata.

Table 8-71~~8-70~~. END_BER_TEST Completion Data

DW	Bit(s)	Field Name and Description
0	31:0	DW/Symbol Count Low – This field contains the lowest 32 bits of the <i>DW/Symbol Count</i> . For a Gen 2 or Gen 3 Link, the <i>DW/Symbol Count</i> is a 48-bit field that contains the number of Doublewords received during the test. For a Gen 4 Link, the <i>DW/Symbol Count</i> is a 48-bit field that contains the number of Symbols received during the test. The counter increments from 0 and shall stop counting at FF...Fh.
1	15:0	DW/Symbol Count High – This field contains the highest 16 bits of the <i>DW/Symbol Count</i> . For a Gen 2 or Gen 3 Link, the <i>DW/Symbol Count</i> is a 48-bit field that contains the number of Doublewords received during the test. For a Gen 4 Link, the <i>DW/Symbol Count</i> is a 48-bit field that contains the number of Symbols received during the test. The counter increments from 0 and shall stop counting at FF...Fh.
	31:16	Bit/Trit Error Count Low – Number of bit/trit errors encountered during the test. For a Gen 2 or Gen 3 Link, the counter increments from 0 and shall stop counting at FFFFh. For a Gen 4 Link, this field contains the lowest 16 bits of the <i>Bit/Trit Error Count</i> . The <i>Bit/Trit Error Count</i> is a 32-bit field that contains the number of error bits/trits detected during the test. The <i>Bit/Trit Error Count</i> increments from 0 and shall stop at FF...Fh.
2	15:0	Bit/Trit Error Count High – This field contains the highest 16 bits of the <i>Bit/Trit Error Count</i> . The <i>Bit/Trit Error Count</i> is a 32-bit field that contains the number of error bits/trits detected during the test. The <i>Bit/trit Error Count</i> increments from 0 and shall stop at FF...Fh. This field is only applicable for a Gen 4 Link. A USB4 Port operating with a Gen 2 or Gen 3 Link shall set this field to 00h.
	31:16	Reserved

Note: To calculate the Bit Error Rate in Gen 2 or Gen 3, the *DW/Symbol Count* should be multiplied by 32. To calculate Trit Error Rate in Gen 4, the *DW/Symbol Count* should be multiplied by 7.

8.3.2.2.5 END_BURST_TEST (Conditional)

The END_BURST_TEST Port Operation stops a running receiver burst BER test pattern.

A USB4 Port shall support the END_BURST_TEST Port Operation if it employs DFE with more than one tap (see Section 3.1.4.3). Otherwise, this Port Operation is not applicable. The END_BURST_TEST Port Operation is used only in Gen 2/3 Links.

Operation Initiation

The Operation Metadata for the END_BURST_TEST Port Operation is defined in Table 8-72.

This Port Operation does not have Operation Data.

Table 8-72~~8-71~~. END_BURST_TEST Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. For a Router: This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port. For a Re-timer: 0h: Target is the USB4 Port whose SB Register Space is written to. 1h: Target is the USB4 Port whose SB Register Space is not written to.
	8:6	Adapter – Identifies the affected Adapter within the USB4 Port. 000b: Lane 0 Adapter 001b: Lane 1 Adapter All other values are reserved.
	31:9	Reserved

Operation Completion

After receiving this Port Operation, a USB4 Port shall stop the *DW Count*, *Burst Restart Count*, and *Error Capture Count* counters associated with the Adapter in the Operation Metadata and shall update the Completion Data as defined in Table 8-73.

The Completion for this Operation does not have Completion Metadata.

Table 8-73~~8-72~~. END_BURST_TEST Completion Data

DW	Bit(s)	Field Name and Description
0	31:0	DW Count Low – This field contains the lowest 32 bits of the <i>DW Count</i> . The <i>DW Count</i> is a 48-bit field that contains the number of Doublewords received during the test. The counter increments from 0 and shall stop counting at FF...Fh.
1	15:0	DW Count High – This field contains the highest 16 bits of a 48-bit number of bits received during the test. This field contains the highest 16 bits of the <i>DW Count</i> . The <i>DW Count</i> is a 48-bit field that contains the number of Doublewords received during the test. The counter increments from 0 and shall stop counting at FF...Fh.
	31:16	Burst Restart Count – Number of burst errors encountered during the test. The counter increments from 0 and shall stop counting at FFFFh. See Section 3.1.4.3 for the definition of the <i>Burst Restart Count</i> counter.
2	31:0	Error Capture Count – Number of error events encountered during the test. The counter increments from 0 and shall stop counting at FF...Fh. See Section 3.1.4.3 for the definition of the <i>Error Capture Count</i> counter.

8.3.2.2.6 READ_BURST_TEST (Conditional)

The READ_BURST_TEST Port Operation reads the *DW Count*, *Burst Restart Count*, and *Error Capture Count* counters. The Operation does not stop execution of the test.

A USB4 Port shall support the READ_BURST_TEST Port Operation if it employs DFE with more than one tap (see Section 3.1.4.3). The END_BURST_TEST Port Operation is used only in Gen 2/3 Links. Otherwise this Port Operation is not applicable.

Operation Initiation

The Operation Metadata for the READ_BURST_TEST Port Operation is defined in Table 8-74.

This Port Operation does not have Operation Data.

Table 8-74~~8-73~~. READ_BURST_TEST Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. For a Router: This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port. For a Re-timer: 0h: Target is the USB4 Port whose SB Register Space is written to. 1h: Target is the USB4 Port whose SB Register Space is not written to.
	8:6	Adapter – Identifies the Adapter within the USB4 Port. 000b: Lane 0 Adapter 001b: Lane 1 Adapter All other values are reserved.
	31:9	Reserved

Operation Completion

After receiving this Port Operation, a USB4 Port shall update the Completion Data as defined in Table 8-75.

The Completion for this Operation does not have Completion Metadata.

Table 8-75~~8-74~~. READ_BURST_TEST Completion Data

DW	Bit(s)	Field Name and Description
0	31:0	DW Count Low – This field contains the lowest 32 bits of the DW Count. The DW Count is a 48-bit field that contains the number of Doublewords received during the test. The counter increments from 0 and shall stop counting at FF...Fh.
1	15:0	DW Count High – This field contains the highest 16 bits of a 48-bit number of bits received during the test. This field contains the highest 16 bits of the DW Count. The DW Count is a 48-bit field that contains the number of Doublewords received during the test. The counter increments from 0 and shall stop counting at FF...Fh.
	31:16	Burst Restart Count – Number of burst errors encountered during the test. The counter increments from 0 and shall stop counting at FFFFh. See Section 3.1.4.3 for the definition of the Burst Restart Count counter.
2	31:0	Error Capture Count – Number of error events encountered during the test. The counter increments from 0 and shall stop counting at FF...Fh. See Section 3.1.4.3 for the definition of the Error Capture Count counter.

8.3.2.2.7 ENTER_EI_TEST (Required)

The ENTER_EI_TEST Port Operation brings a transmitter into electrical idle state.

A USB4 Port shall support the ENTER_EI_TEST Port Operation.

Operation Initiation

The Operation Metadata for the ENTER_EI_TEST Port Operation is defined in Table 8-76.

Table 8-768-75. ENTER_EI_TEST Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. For a Router: This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port. For a Re-timer: 0h: Target is the USB4 Port whose SB Register Space is written to. 1h: Target is the USB4 Port whose SB Register Space is not written to.
	8:6	Adapter – Identifies the Adapter within the USB4 Port. 000b: TX0 001b: TX1 010b: TX2 (only applies to a Port that supports Asymmetric Link with 3 Tx) All other values are reserved.
	31:9	Reserved

This Port Operation does not have Operation Data.

Operation Completion

After receiving an ENTER_EI_TEST Port Operation, a USB4 Port shall disable the transition from Training state to CLd state due to timeouts (defined in Section 4.2.1.3.3). When the USB4 Port detects SBRX at logical low for tDisconnectRx, it shall re-enable the transition from Training state to CLd state due to timeouts.

A Router that receives an ENTER_EI_TEST Port Operation shall transition the Lane transmitter defined in the Operation into electrical idle state.

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

8.3.2.2.8 LFPS_TEST (Conditional)

The LFPS_TEST Port Operation tests LFPS transmission and detection.

A USB4 Port that supports Gen 4 or CLx shall support the LFPS_TEST Port.

Operation Initiation

The Operation Metadata for the LFPS_TEST Port Operation is defined in Table 8-77.

Table 8-778-76. LFPS_TEST Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. For a Router: This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port. For a Re-timer: 0h: Target is the USB4 Port whose SB Register Space is written to. 1h: Target is the USB4 Port whose SB Register Space is not written to.
	8:6	Adapter – Identifies the Adapter within the USB4 Port. 000b: TX0 (for Modes 000b and 001b) \RX0 (for Modes 010b and 011b) 001b: TX1 (for Modes 000b and 001b) \RX1 (for Modes 010b and 011b) 010b: TX2 (for Modes 000b and 001b) \RX2 (for Modes 010b and 011b) (only applies to a Port that supports Asymmetric Link with 3 Tx or 3 Rx) All other values are reserved.
	11:9	Mode – This field defines the LFPS test mode. 000b: Adapter shall transmit LFPS continuously. 001b: Adapter shall transmit 100 cycles of LFPS, transition to Electrical Idle for tPreData and start sending SLOS1 (for Gen 2 or Gen 3) or PRBS11 (for Gen 4). 010b: Adapter shall transmit LFPS continuously after detecting 3 LFPS cycles on the selected receiver. 011b: Adapter shall transmit LFPS when it detects LFPS on the selected receiver. Adapter shall move to Electrical Idle when not detecting LFPS on the selected receiver. Note: In Modes 010b and 011b, when Link is Symmetric, the transmission of LFPS will be on selected Lane transmitter, When the Link is Asymmetric, the transmission of LFPS will be on TX0.
	31:12	Reserved

This Port Operation does not have Operation Data.

Operation Completion

After receiving an LFPS_TEST Port Operation, a USB4 Port shall start transmitting LFPS according to the selected Mode and disable the transition from Training state to CLd state due to timeouts (defined in Section 4.2.1.3.3). When the USB4 Port detects SBRX at logical low for tDisconnectRx, it shall stop transmitting the LFPS and re-enable the transition from Training state to CLd state due to timeouts.

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

8.3.2.2.9 SET_LINK_TYPE (Conditional)

The SET_LINK_TYPE Operation is used to force Lane Reversal or to force the Link to come up as an Asymmetric Link after Lane Initialization. This Operation is used as part of the transmitter compliance test as described in Section 8.3.2.2.

Note: When the USB4 Port detects SBRX at logical low for tDisconnectRx, the effect of a SET_LINK_TYPE Operation is nullified.

A USB4 Port that supports operation with an Asymmetric Link (3 TX and/or 3 RX) shall support the SET_LINK_TYPE Port Operation.

Operation Initiation

The Operation Metadata for the SET_LINK_TYPE Port Operation is defined in Table 8-78.

Table 8-788-77. SET_LINK_TYPE Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port.
	7:6	Link Type – Identifies the type of Link to establish after Lane Initialization: 00b: Port shall set the <i>Target Asymmetric Link</i> field to 00b (Symmetric Link) 01b: Port shall set the <i>Target Asymmetric Link</i> field to 01b (3 transmitters) 10b: Port shall set the <i>Target Asymmetric Link</i> field to 10b (3 receivers) All other values are reserved.
	8	Force Lane Reversal – Identifies whether to override the functional Lane Reversal. 0b: Port shall ignore the <i>Lane Reversal Value</i> and use the information acquired in Phase 1. 1b: Port shall use the <i>Lane Reversal Value</i> instead the information acquired in Phase 1.
	9	Lane Reversal Value – When <i>Force Lane Reversal</i> is set to 1b, this field forces the High-Speed Lanes Reversal. 0b: Port shall keep the designation of Lane 0 and Lane 1 as if the Cable was inserted in a straight insertion. 1b: Port shall swap the designation of Lane 0 and Lane 1 as if the Cable was inserted in a reversed insertion. <i>Note: Sideband SBTX and SBRX should remain as detected in Phase 1.</i>
	31:10	Reserved

This Port Operation does not have Operation Data.

Operation Completion

If the USB4 Port does not support the Link Type in the SET_LINK_TYPE Operation or if the Operation is received after the Port already sent the AT Read Response for the Link Configuration Register Transaction, the Port responds with an error as described in Section 8.3.2.1.

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

8.3.2.3 Service Port Operations

8.3.2.3.1 ROUTER_OFFLINE_MODE (Required)

The ROUTER_OFFLINE_MODE Port Operation transitions a USB4 Port that is not connected into an offline mode. When in this mode, the USB4 Port shall not perform Lane Initialization. The USB4 Port still processes Operations delivered from software.

A USB4 Port shall support the ROUTER_OFFLINE_MODE Port Operation. A USB4 Port shall execute this Operation when delivered locally. A USB4 Port shall reject this Operation when delivered from the Sideband Channel.

Operation Initiation

The *Target* field in the USB4 Port Capability is set to 000b.

This Port Operation does not have Operation Data.

Table 8-79~~8-78~~. ROUTER_OFFLINE_MODE Operation Metadata

DW	Bit(s)	Field Name and Description
0	0	Enter Offline Mode When set to 0b, the USB4 Port shall enter offline mode. When set to 1b, the USB4 Port shall exit offline mode.
	31:1	Reserved

Operation Completion

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

8.3.2.3.2 ENUMERATE_RE-TIMERS (Required)

The ENUMERATE_RE-TIMERS Port Operation causes a USB4 Port to send a Broadcast RT Transaction.

A USB4 Port shall support the ENUMERATE_RE-TIMERS Port Operation. A USB4 Port shall execute this Operation when delivered locally. A USB4 Port shall reject this Operation when delivered from the Sideband Channel.

Operation Initiation

This Port Operation does not have Operation Metadata.

This Port Operation does not have Operation Data.

Operation Completion

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

8.3.2.3.3 FEC_ERRORS_STAT (Required)

The FEC_ERRORS_STAT Port Operation starts, stops, and read the FEC errors counters of the Port.

A USB4 Port that supports Gen 4, shall support the FEC_ERRORS_STAT Port Operation.

Operation Initiation

The Operation Metadata for the FEC_ERRORS_STAT Port Operation is defined in Table 8-80.

Table 8-80~~8-79~~. FEC_ERRORS_STAT Operation Metadata

DW	Bit(s)	Field Name and Description
0	5:0	Port – Identifies the target USB4 Port. For a Router: This field contains the Adapter Number of the Lane 0 Adapter of the target USB4 Port. For a Re-timer: 0h: Target is the USB4 Port whose SB Register Space is written to. 1h: Target is the USB4 Port whose SB Register Space is not written to.

DW	Bit(s)	Field Name and Description
	7:6	Control – Indicates what operation to perform on the FEC Errors Statistics Counters. 00b: Clear Counters 01b: Start Counter 10b: Stop Counters 11b: Read Counters
	31:8	Reserved

Operation Completion

After receiving this Port Operation, a USB4 Port shall:

- If Control = 00b, clear all FEC Errors Statistics Counters.
- If Control = 01b, start all FEC Errors Statistics Counters.
- If Control = 10b, stop all FEC Errors Statistics Counters.
- If Control = 11b, read all FEC Errors Statistics Counters.

The Completion for this Operation does not have Completion Metadata.

After receiving this Port Operation with *Control* field set to 10b or 11b, a USB4 Port shall update the Completion Data as defined in Table 8-81.

Table 8-81~~8-80~~. FEC_ERRORS_STAT Completion Data

DW	Bit(s)	Field Name and Description
0	31:0	FEC Blocks with 0 Error Symbols – This field contains the number of FEC blocks with no error Symbols when RS-FEC is activated. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block without any errors. The Counter shall stop counting at FF...Fh. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.
1	31:0	FEC Blocks with 1 Error Symbol – This field contains the number of FEC blocks with 1 error Symbol when RS-FEC is activated. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 1 error Symbol. The Counter shall stop counting at FF...Fh. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.
2	23:0	FEC Blocks with 2 Error Symbol – This field contains the number of FEC blocks with 2 error Symbols when RS-FEC is activated. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 2 error Symbols. The Counter shall stop counting at FF...Fh. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.
	31:24	Reserved

DW	Bit(s)	Field Name and Description
3	23:0	<p>FEC Blocks with 3 Error Symbol – This field contains the number of FEC blocks with 3 error Symbols when RS-FEC is activated.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 3 error Symbols. The Counter shall stop counting at FF...Fh.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.</p>
	31:24	Reserved
4	15:0	<p>FEC Blocks with 4 Error Symbol – This field contains the number of FEC blocks with 4 error Symbols when RS-FEC is activated.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 4 error Symbols. The Counter shall stop counting at FFFFh.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.</p>
	31:16	<p>FEC Blocks with 5 Error Symbol – This field contains the number of FEC blocks with 5 error Symbols when RS-FEC is activated.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 5 error Symbols. The Counter shall stop counting at FFFFh.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.</p>
5	15:0	<p>FEC Blocks with 6 Error Symbol – This field contains the number of FEC blocks with 6 error Symbols when RS-FEC is activated.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 6 error Symbols. The Counter shall stop counting at FFFFh.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.</p>
	31:16	<p>FEC Blocks with 7 Error Symbol – This field contains the number of FEC blocks with 7 error Symbols when RS-FEC is activated.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 7 error Symbols. The Counter shall stop counting at FFFFh.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.</p>
6	15:0	<p>FEC Blocks with 8 Error Symbol – This field contains the number of FEC blocks with 8 error Symbols when RS-FEC is activated.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 8 error Symbols. The Counter shall stop counting at FFFFh.</p> <p>After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.</p>

DW	Bit(s)	Field Name and Description
	23:16	FEC Blocks with 9 Error Symbol – This field contains the number of FEC blocks with 9 error Symbols when RS-FEC is activated. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 9 error Symbols. The Counter shall stop counting at FFh. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.
	31:24	FEC Blocks with 10 Error Symbol – This field contains the number of FEC blocks with 10 error Symbols when RS-FEC is activated. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 10 error Symbols. The Counter shall stop counting at FFh. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.
7	7:0	FEC Blocks with 11 Error Symbol – This field contains the number of FEC blocks with 11 error Symbols when RS-FEC is activated. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 11 error Symbols. The Counter shall stop counting at FFh. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.
	11:8	FEC Blocks with 12 Error Symbol – This field contains the number of FEC blocks with 12 error Symbols when RS-FEC is activated. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with exactly 12 error Symbols. The Counter shall stop counting at Fh. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.
	15:12	FEC Blocks with more than 12 Error Symbol – This field contains the number of FEC blocks with more than 12 error Symbols when RS-FEC is activated. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 00b, this field shall be cleared to 0. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 01b, this field shall be incremented by 1 for every FEC block with more than 12 error Symbols. The Counter shall stop counting at Fh. After receiving a FEC_ERRORS_STAT Operation with the <i>Control</i> field set to 10b, this field shall stop incrementing.
	31:16	Reserved

8.3.2.4 Receiver Lane Margining Port Operations

The Port Operations defined in the subsections below are used for Receiver Lane Margining tests. See Section 3.1.6 for more details on Receiver Lane Margining.

8.3.2.4.1 READ_LANE_MARGIN_CAP (Required)

The READ_LANE_MARGIN_CAP Port Operation reads the Receiver Lane Margining capabilities of a USB4 Port.

A USB4 Port shall support the READ_LANE_MARGIN_CAP Port Operation.

Operation Initiation

This Port Operation does not have Operation Metadata. This Port Operation does not have Operation Data.

Operation Completion

If completed successfully, the Port Operation returns three Doublewords of Completion Data as shown in Table 8-82. If the Port does not support Gen 4, it shall set DW2 to 0.

The Completion for this Operation does not have Completion Metadata.

Table 8-82~~8-81~~. READ_LANE_MARGIN_CAP Completion Data

DW	Bit(s)	Field Name and Description
0	1:0	Gen 2/3 Receiver Lane Margining Modes This field indicates the Receiver Lane Margining modes supported by the USB4 Port for Gen 2 and Gen 3 Links. 00b: Reserved 01b: Only HW mode supported 10b: Only SW mode supported 11b: Both HW mode and SW mode supported
	2	Multiple-Lane Margining This field indicates whether the USB4 Port supports simultaneous Lane Margining on both Lanes. 0b: Each Lane is tested separately 1b: All Lanes can be tested simultaneously
	4:3	Gen 2/3 Independent High/Low Voltage Margin This field indicates how Gen 2/3 voltage margins are returned: 00b: The Router returns the minimum between the high and low voltage margins 01b: The Router returns either the high voltage margin or the low voltage margin 10b: The Router returns both the high voltage margin and the low voltage margin (relevant only for HW mode) 11b: Reserved
	5	Gen 2/3 Time Margining This field indicates if Time Margining is supported. 0b: Time Margining is not supported for Gen 2/3 1b: Time Margining is supported for Gen 2/3
	12:6	Gen 2/3 Voltage Margin Steps – Mandatory Range This field contains the number of voltage margin steps that are supported by the USB4 Port. The number of margin steps applies to both the high margin and the low margin separately. A Router shall set this value to a minimum of 25.
	18:13	Gen 2/3 Maximum Voltage Offset – Mandatory Range This field contains the maximum supported voltage offset for Gen 2 and Gen 3 Links. The maximum voltage offset applies to both the high margin and the low margin separately. A value of n in this field corresponds to a maximum voltage offset of $[74 + n \times 2]$ mV.
	19	Gen 2/3 Optional Voltage Offset Range This field indicates if the USB4 Port supports an optional voltage offset range. 0b: Optional Voltage Offset Range is not supported 1b: Optional Voltage Offset Range is supported
	26:20	Gen 2/3 Voltage Margin Steps – Optional Range This field contains the number of voltage margin steps that are supported by the USB4 Port for the Optional Voltage Offset Range. The number of margin steps applies to both the high margin and the low margin separately. A Router shall set this value to a minimum of 25. This field is reserved if the <i>Optional Voltage Offset Range</i> field is 0b.

DW	Bit(s)	Field Name and Description
	27	Corresponding Port Supported This field indicate if a USB4 Re-timer supports the activation of Lane Margining on the corresponding Port by executing the Port Operation this Port. See <i>Port Select</i> field in Table 8-82 and Table 8-85. 0b: Executing Lane Margining on the Corresponding Port is not supported. 1b: Executing Lane Margining on the Corresponding Port is supported. For a USB4 Router, this bit shall be set to 0b.
	28	Extended Error Counter Support This field indicate if a USB4 Router/Re-timer supports an extended error counter when using SW Lane Margining. See <i>Extended Error Counter</i> field in Table 8-87. 0b: Extended Error Counter is not supported. 1b: Extended Error Counter is supported.
	31:29	Reserved
1	7:0	Gen 2/3 Maximum Voltage Offset – Optional Range This field contains the maximum supported voltage offset for the optional range. The maximum voltage offset applies to both the high margin and the low margin separately. A value of n in this field corresponds to a maximum voltage offset of $[74 + n \times 2]$ mV. Values larger than A3h are Reserved. This field is reserved if the <i>Optional Voltage Offset Range</i> field is 0b.
	8	Destructive Time Margining This bit indicates whether the time margining test is destructive or non-destructive: 0b: Non-destructive (will not cause actual bit errors on the Link) 1b: Destructive (can cause actual bit errors on the Link) This bit shall be set to 0b if the <i>Time Margining</i> bit is set to 0b.
	10:9	Gen 2/3 Independent Left/Right Timing Margin Test This field indicates how Gen 2/3 timing margins are returned: 00b: The Router returns the minimum between the left and right time margins 01b: The Router returns either the left margin or the right time margin 10b: The Router returns both the left margin and the right margin 11b: Reserved This field shall be set to 0 if the <i>Time Margining</i> bit is set to 0b.
	15:11	Time Margin Steps This field contains the number of time margin steps that are supported by the USB4 Port. The number of margin steps applies to both the left margin and the right margin separately. This field shall be set to 0 if the <i>Time Margining</i> bit is set to 0b. Else, this field shall be set to a value between 07h and 1Fh.
	20:16	Maximum Time Offset This field contains the maximum time offset supported by the USB4 Port. The maximum time offset applies to both the left margin and the right margin separately. A value of n in this field corresponds to a maximum offset of $[0.2 + 0.01 \times n]$ UI. This field shall be set to 0 if the <i>Time Margining</i> bit is set to 0b. Else, this field shall be set to a value between 0h and 1Eh.
	25:21	Min BER Level Contour Support The value in this field (n) indicates the minimum BER level contour supported: For even values of n, the minimal BER level contour supported is $1e[-12 + n/2]$. For odd values of n, the minimal BER level contour supported is $3 \times 1e[-12 + (n-1)/2]$. Values larger than 10h are Reserved. This field is Reserved if the <i>Receiver Lane Margining Modes</i> field is 10b.
	30:26	Max BER Level Contour Support The value in this field (n) indicates the maximum BER level contour supported. For even values n, the maximum BER level contour supported is $1e[-12 + n/2]$. For odd values n, the maximum BER level contour supported is $3 \times 1e[-12 + (n-1)/2]$. Values larger than 10h are Reserved. This field is Reserved if the <i>Receiver Lane Margining Modes</i> field is 10b.

DW	Bit(s)	Field Name and Description
	31	Reserved
2	1:0	Gen 4 Receiver Lane Margining Modes This field indicates the Receiver Lane Margining modes supported by the USB4 Port for a Gen 4 Link. 00b: Reserved 01b: Only HW mode supported 10b: Only SW mode supported 11b: Both HW mode and SW mode supported
	2	Gen 4 Time Margining This field indicates if Time Margining is supported for a Gen 4 Link. 0b: Time Margining is not supported for Gen 4 1b: Time Margining is supported for Gen 4
	8:3	Gen 4 Maximum Voltage Offset This field contains the maximum supported voltage offset for a Gen 4 Link. The maximum voltage offset applies to both the high margin and the low margin separately. A value of n in this field corresponds to a maximum voltage offset of $[74/2 + n]$ mV.
	15:9	Gen 4 Voltage Margin Steps This field contains the number of voltage margin steps that are supported by the USB4 Port for a Gen 4 Link. The number of margin steps applies to both the high margin and the low margin separately. A Router shall set this value to a minimum of 25.
	17:16	Gen 4 Independent High/Low Voltage Margin This field indicates how Gen 4 voltage margins are returned: 00b: The Router returns the minimum between the high and low voltage margins in both lower and upper eye 01b: The Router returns the high voltage margin of both lower and upper eye and the low voltage margin of both lower and upper eye
	19:18	Gen 4 Independent Left/Right Timing Margin Test This field indicates how timing margins are returned: 00b: The Router returns the minimum between the left and right time margins in both lower and upper eye 01b: The Router returns the left margin and the right time margin of both lower and upper eye This field shall be set to 0 if the <i>Gen 4 Time Margining</i> bit is set to 0b.
	31:20	Reserved

8.3.2.4.2 RUN_HW_LANE_MARGINING (Conditional)

The RUN_HW_LANE_MARGINING Operation sets the parameters for HW Mode Receiver Lane Margining and executes a HW Mode Receiver Lane Margining test. If the Port Operation completes successfully, the target of the Operation shall set the Completion Metadata listed in Table 8-85.

A USB4 Port shall support this operation if software margining mode is not supported (see Section 3.1.6.1). If software margining mode is supported, support for this Port Operation is optional. If a USB4 Port supports Destructive Time margining and the *Timing Margin Test* bit is set to 1b, the Port shall not initiate a disconnect when detecting errors.



CONNECTION MANAGER NOTE

If the RUN_HW_LANE_MARGINING Operation runs a timing margin test, and the test is destructive, the Connection Manager shall not enable the Gen 4 Link Recovery flow.

Operation Initiation

This Port Operation does not have Operation Data.

Table 8-838-82. RUN_HW_LANE_MARGINING Operation Metadata

DW	Bit(s)	Field Name and Description
0	2:0	Lane Select This field indicates which Lane(s) to perform the Receiver Lane Margining test on: 000b: RX0 001b: RX1 010b: RX2 (only applies to a Port that supports Asymmetric Link with 3 Rx) 111b: Test runs on all Lanes Other values are Reserved. The Port Operation shall fail if this field is set to 111b and the Router supports Lane Margining on a single Lane only as present in the <i>Two-Lane Margining</i> bit.
	3	Timing Margin Test This bit selects between a voltage margin test and a timing margin test 0b: Perform a voltage margin test 1b: Perform a timing margin test The Port Operation shall fail if this field is set to 1b and the Router does not support timing margin testing.
	4	Enable Margin Tests For a Gen 2/3 voltage margin test, this field enables high margin test or low margin test when the <i>Gen 2/3 Independent High/Low Voltage Margin</i> field in the READ_LANE_MARGIN_CAP Completion Metadata was set to 01b: 0b: Enables low margin test 1b: Enables high margin test For a Gen 4 voltage margin test, this field chooses the lower or upper eye when the <i>Gen 4 Independent High/Low Voltage Margin</i> field in the READ_LANE_MARGIN_CAP Completion Metadata was set to 01b: 0b: Enables margin test on lower eye 1b: Enables margin test on upper eye For a Gen 2/3 timing margin test, this field enables right margin test or left margin test when the <i>Gen 2/3 Independent Left/Right Timing Margin Test</i> field in the READ_LANE_MARGIN_CAP Completion Metadata was set to 01b: 0b: Enables left margin test 1b: Enables right margin test For a Gen 4 timing margin test, this field chooses the lower or upper eye when the <i>Gen 4 Independent Left/Right Timing Margin</i> field in the READ_LANE_MARGIN_CAP Completion Metadata was set to 01b: 0b: Enables margin test on lower eye 1b: Enables margin test on upper eye
	9:5	BER Level Contour This field sets the BER level contour: For even values n, the maximum BER level contour supported is $1e[-12 + n/2]$. For odd values n, the maximum BER level contour supported is $3 \times 1e[-12 + (n-1)/2]$. Values larger than 10h are Reserved.
	10	Enable Optional Voltage Offset Range For a Gen 2/3 voltage margin test, this field enables the mandatory voltage margin offset range or the optional extended voltage offset range when the <i>Gen 2/3 Optional Voltage Offset Range</i> field in the READ_LANE_MARGIN_CAP Completion Metadata was set to 1b: 0b: Enables the mandatory Rx voltage offset range 1b: Enables the optional Rx voltage offset range This bit is reserved for Gen 4.

DW	Bit(s)	Field Name and Description
	11	Port Select This field indicate on which Port the Lane Margining is activated: 0b: Activate Lane Margining on this Port 1b: Activate Lane Margining on the Corresponding Port When using the Operation on a USB4 Router, this bit shall be set to 0b
	31:12	Reserved

Operation Completion

Completion Data for the RUN_HW_LANE_MARGINING Operation depicted in Table 8-85 contains the results for the HW test. Table 8-84 defines how the contents of each field are selected. The Completion Data is 3 DW in length if the Link is Asymmetric with 3 receivers. Otherwise the Completion Data is 2 DW in length.

The Completion for this Operation does not have Completion Metadata.

Table 8-848-83. Contents Selection for RUN_HW_LANE_MARGINING Completion Data

Field	Lane Select	Independent High/Low Voltage Margin & Independent Left/Right Timing Margin Test	Enable Margin Tests	Contents
High / Right Margin (RX0)	001b	x	x	Reserved.
	010b	x	x	Reserved.
	000b or 111b	00b	x	Gen 2/3 – Minimum between the high and low voltage margins / minimum between the left and right time margins. Gen 4 – Minimum between the high and low voltage margin of upper and lower eye / minimum between the left and right time margins of upper and lower eye.
		01b	0b	Gen 2/3 – Reserved. Gen 4 – High voltage margin of lower eye / right time margin of lower eye.
			1b	Gen 2/3 – High voltage margin / right time margin. Gen 4 – High voltage margin of upper eye / right time margin of upper eye.
		10b	x	Gen 2/3 – High voltage margin / right time margin. Gen 4 – Reserved.
Low / Left Margin (RX0)	001b	x	x	Reserved.
	010b	x	x	Reserved.
	000b or 111b	00b	x	Reserved.
		01b	0b	Gen 2/3 – Low voltage margin / left time margin. Gen 4 – Low voltage margin of lower eye / left time margin of lower eye.
			1b	Gen 2/3 –Reserved. Gen 4 – Low voltage margin of upper eye / left time margin of upper eye.
		10b	x	Reserved.

Field	Lane Select	Independent High/Low Voltage Margin & Independent Left/Right Timing Margin Test	Enable Margin Tests	Contents
		10b	x	Gen 2/3 – Low voltage margin / left time margin. Gen 4 – Reserved.
High / Right Margin (RX1)	000b	x	x	Reserved.
	010b	x	x	Reserved.
	001b or 111b	00b	x	Gen 2/3 – Minimum between the high and low voltage margins / minimum between the left and right time margins. Gen 4 – Minimum between the high and low voltage margin of upper and lower eye / minimum between the left and right time margins of upper and lower eye.
		01b	0b	Gen 2/3 – Reserved. Gen 4 – High voltage margin of lower eye / right time margin of lower eye.
			1b	Gen 2/3 – High voltage margin / right time margin. Gen 4 – High voltage margin of upper eye / right time margin of upper eye.
		10b	x	Gen 2/3 – High voltage margin / right time margin. Gen 4 – Reserved.
Low / Left Margin (RX1)	000b	x	x	Reserved.
	010b	x	x	Reserved.
	001b or 111b	00b	x	Reserved.
		01b	0b	Gen 2/3 – Low voltage margin / left time margin. Gen 4 – Low voltage margin of lower eye / left time margin of lower eye.
			1b	Gen 2/3 – Reserved. Gen 4 – Low voltage margin of upper eye / left time margin of upper eye.
		10b	x	Gen 2/3 – Low voltage margin / left time margin. Gen 4 – Reserved.
High / Right Margin (RX2)	000b	x	x	Reserved.
	001b	x	x	Reserved.
	010b or 111b	00b	x	Gen 2/3 – Minimum between the high and low voltage margins / minimum between the left and right time margins. Gen 4 – Minimum between the high and low voltage margin of upper and lower eye / minimum between the left and right time margins of upper and lower eye.
		01b	0b	Gen 2/3 – Reserved. Gen 4 – High voltage margin of lower eye / right time margin of lower eye.
			1b	Gen 2/3 – High voltage margin / right time margin. Gen 4 – High voltage margin of upper eye / right time margin of upper eye.

Field	Lane Select	Independent High/Low Voltage Margin & Independent Left/Right Timing Margin Test	Enable Margin Tests	Contents
		10b	x	Gen 2/3 – High voltage margin / right time margin. Gen 4 – Reserved.
Low / Left Margin (RX2)	000b	x	x	Reserved.
	001b	x	x	Reserved.
	010b or 111b	00b	x	Reserved.
		01b	0b	Gen 2/3 –Low voltage margin / left time margin. Gen 4 – Low voltage margin of lower eye / left time margin of lower eye.
			1b	Gen 2/3 – Reserved. Gen 4 – Low voltage margin of upper eye / left time margin of upper eye.
		10b	x	Gen 2/3 – Low voltage margin / left time margin. Gen 4 – Reserved.

Table 8-85~~8-84~~. RUN_HW_LANE_MARGINING Completion Data

DW	Bit(s)	Field Name and Description
0	2:0	Lane Select This field contains the value of the <i>Lane Select</i> field in the last RUN_HW_LANE_MARGINING Port Operation.
	3	Timing Margin Test This field contains the value of the <i>Timing Margin Test</i> field in the last RUN_HW_LANE_MARGINING Port Operation.
	4	Enable Margin Tests This field contains the value of the <i>Enable Margin Tests</i> field in the last RUN_HW_LANE_MARGINING Port Operation.
	9:5	BER Level Contour This field contains the value of the <i>BER Level Contour</i> field in the last RUN_HW_LANE_MARGINING Port Operation.
	10	Enable Optional Voltage Offset Range This field contains the value of the <i>Enable Optional Voltage Offset Range</i> field in the last RUN_HW_LANE_MARGINING Port Operation.
	11	Port Select This field contains the value of the <i>Port Select</i> field in the last RUN_HW_LANE_MARGINING Port Operation.
	31:12	Reserved.
1	6:0	High / Right Margin (RX0) For a voltage margin test, this field contains the high margin test result for RX0 in terms of number of voltage offset steps to the BER Level Contour. If the high margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset step which was applied during the test. See Note 1. For a time margin test, this field contains the right margin test result for RX0 in terms of number of time offset steps to the BER Level Contour. If the right margin exceeds the Maximum Time Offset this field contains the maximum right offset step which was applied during the test. See Note 2.

DW	Bit(s)	Field Name and Description
	7	High / Right Margin Exceeds Maximum Voltage / Time Offset (RX0) For a voltage margin test, this field indicates if the high margin exceeds the Maximum Voltage Offset for RX0: 0b: High margin does not exceed the Maximum Voltage Offset 1b: High margin exceeds the Maximum Voltage Offset For a time margin test, this field indicates if the right margin exceeds the Maximum Time Offset for RX0: 0b: Right margin does not exceed the Maximum Time Offset 1b: Right margin exceeds the Maximum Time Offset
	14:8	Low / Left Margin (RX0) For a voltage margin test, this field contains the low margin test result for RX0 in terms of number of voltage offset steps to the BER Level Contour. If the Low margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset step which was applied during the test. See Note 3. For a time margin test, this field contains the left margin test result for RX0 in terms of number of time offset steps to the BER Level Contour. If the left margin exceeds the Maximum Time Offset this field contains the maximum left offset step which was applied during the test. See Note 4.
	15	Low / Left Margin Exceeds Maximum Voltage / Time Offset (RX0) For a voltage margin test, this field indicates if the low margin exceeds the Maximum Voltage Offset for RX0: 0b: Low margin does not exceed the Maximum Voltage Offset 1b: Low margin exceeds the Maximum Voltage Offset For a time margin test, this field indicates if the left margin exceeds the Maximum Time Offset for RX0: 0b: Left margin does not exceed the Maximum Time Offset 1b: Left margin exceeds the Maximum Time Offset
	22:16	High / Right Margin (RX1) For a voltage margin test, this field contains the high margin test result for RX1 in terms of number of voltage offset steps to the BER Level Contour. If the high margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset step which was applied during the test. See Note 1. For a time margin test, this field contains the right margin test result for RX1 in terms of number of time offset steps to the BER Level Contour. If the right margin exceeds the Maximum Time Offset this field contains the maximum right offset step which was applied during the test. See Note 2.
	23	High / Right Margin Exceeds Maximum Voltage / Time Offset (RX1) For a voltage margin test, this field indicates if the high margin exceeds the Maximum Voltage Offset for RX1: 0b: High margin does not exceed the Maximum Voltage Offset 1b: High margin exceeds the Maximum Voltage Offset For a time margin test, this field indicates if the right margin exceeds the Maximum Time Offset for RX1: 0b: Right margin does not exceed the Maximum Time Offset 1b: Right margin exceeds the Maximum Time Offset
	30:24	Low / Left Margin (RX1) For a voltage margin test, this field contains the low margin test result for RX1 in terms of number of voltage offset steps to the BER Level Contour. If the low margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset step which was applied during the test. See Note 3. For a time margin test, this field contains the left margin test result for RX1 in terms of number of time offset steps to the BER Level Contour. If the left margin exceeds the Maximum Time Offset this field contains the maximum left offset step which was applied during the test. See Note 4.

DW	Bit(s)	Field Name and Description
	31	Low / Left Margin Exceeds Maximum Voltage / Time Offset (RX1) For a voltage margin test, this field indicates if the low margin exceeds the Maximum Voltage Offset for RX1: 0b: Low margin does not exceed the Maximum Voltage Offset 1b: Low margin exceeds the Maximum Voltage Offset For a time margin test, this field indicates if the left margin exceeds the Maximum Time Offset for RX1: 0b: Left margin does not exceed the Maximum Time Offset 1b: Left margin exceeds the Maximum Time Offset
2	6:0	High / Right Margin (RX2) For a voltage margin test, this field contains the high margin test result for RX2 in terms of the number of voltage offset steps to the BER Level Contour. If the high margin exceeds the Maximum Voltage Offset, this field contains the maximum voltage offset step which was applied during the test. See Note 1. For a time margin test, this field contains the right margin test result for RX2 in terms of the number of time offset steps to the BER Level Contour. If the right margin exceeds the Maximum Time Offset, this field contains the maximum right offset step which was applied during the test. See Note 2.
	7	High / Right Margin Exceeds Maximum Voltage / Time Offset (RX2) For a voltage margin test, this field indicates if the high margin exceeds the Maximum Voltage Offset for RX2: 0b: High margin does not exceed the Maximum Voltage Offset. 1b: High margin exceeds the Maximum Voltage Offset. For a time margin test, this field indicates if the right margin exceeds the Maximum Time Offset for RX2: 0b: Right margin does not exceed the Maximum Time Offset. 1b: Right margin exceeds the Maximum Time Offset.
	14:8	Low / Left Margin (RX2) For a voltage margin test, this field contains the low margin test result for RX2 in terms of the number of voltage offset steps to the BER Level Contour. If the Low margin exceeds the Maximum Voltage Offset, this field contains the maximum voltage offset step which was applied during the test. See Note 3. For a time margin test, this field contains the left margin test result for RX2 in terms of the number of time offset steps to the BER Level Contour. If the left margin exceeds the Maximum Time Offset, this field contains the maximum left offset step which was applied during the test. See Note 4.
	15	Low / Left Margin Exceeds Maximum Voltage / Time Offset (RX2) For a voltage margin test, this field indicates if the low margin exceeds the Maximum Voltage Offset for RX2: 0b: Low margin does not exceed the Maximum Voltage Offset. 1b: Low margin exceeds the Maximum Voltage Offset. For a time margin test, this field indicates if the left margin exceeds the Maximum Time Offset for RX2: 0b: Left margin does not exceed the Maximum Time Offset. 1b: Left margin exceeds the Maximum Time Offset.

DW	Bit(s)	Field Name and Description
<p>Note 1. The High Margin test result can be reported by application software in units of mV by the following conversion:</p> $\text{High Margin (mV)} = \text{High Margin (steps)} \times \text{Maximum Voltage Offset (mV)} \div \text{Voltage Margin Steps (steps)}$ <p>Note 2. The Right Margin test result can be reported by application software in units of UI by the following conversion:</p> $\text{Right Margin (UI)} = \text{Right Margin (steps)} \times \text{Maximum Time Offset (UI)} \div \text{Time Margin Steps (steps)}$ <p>Note 3. The Low Margin test result can be reported by application software in units of mV by the following conversion:</p> $\text{Low Margin (mV)} = \text{Low Margin (steps)} \times \text{Maximum Voltage Offset (mV)} \div \text{Voltage Margin Steps (steps)}$ <p>Note 4. The Left Margin test result can be reported by application software in units of UI by the following conversion:</p> $\text{Left Margin (UI)} = \text{Left Margin (steps)} \times \text{Maximum Time Offset (UI)} \div \text{Time Margin Steps (steps)}$		



CONNECTION MANAGER NOTE

If the RUN_HW_LANE_MARGINING Operation runs a timing margin test, and the test is destructive, then following the execution of this Operation, the Connection Manager can bring the Router out of compliance mode by transitioning it to the Uninitialized state.

8.3.2.4.3 RUN_SW_LANE_MARGINING (Conditional)

The RUN_SW_LANE_MARGINING sets the parameters for SW Mode Receiver Lane Margining and starts the SW Mode Receiver Lane Margining test.

A USB4 Port shall support the RUN_SW_LANE_MARGINING Port Operation if hardware margining mode is not supported (see Section 3.1.6.1). If hardware margining mode is supported, support for this Port Operation is optional.

Operation Initiation

This Port Operation does not have Operation Data.

Table 8-868-85. RUN_SW_LANE_MARGINING Operation Metadata

DW	Bit(s)	Field Name and Description
0	2:0	Lane Select This field indicates which Lane(s) to perform the Receiver Lane Margining test on: 000b: RX0 001b: RX1 010b: RX2 (only applies to a Port that supports Asymmetric Link with 3 Rx) 111b: Test runs on all Lanes Other values are Reserved. The Port Operation shall fail if this field is set to 111b and the Router supports Lane Margining on a single Lane only as present in the <i>Two-Lane Margining</i> bit.
	3	Timing Margin Test This bit selects between a voltage margin test and a timing margin test: 0b: Perform a voltage margin test 1b: Perform a timing margin test The Port Operation shall fail if this field is set to 1b and the Router does not support timing margin testing.

DW	Bit(s)	Field Name and Description
	4	Enable Margin Tests For a voltage margin test, this field enables high margin test or low margin test when the <i>Gen 2/3 Independent High/Low Voltage Margin</i> or the <i>Gen 4 Independent High/Low Voltage Margin</i> field in the READ_LANE_MARGIN_CAP Completion Metadata was set to 01b: 0b: Enables low margin test 1b: Enables high margin test For a timing margin test, this field enables right margin test or left margin test when the <i>Gen 2/3 Independent Left/Right Timing Margin Test</i> or the <i>Gen 4 Independent Left/Right Timing Margin Test</i> field in the READ_LANE_MARGIN_CAP Completion Metadata was set to 01b: 0b: Enables left margin test 1b: Enables right margin test
	5	Enable Optional Voltage Offset Range For a Gen 2/3 voltage margin test, this field enables the mandatory voltage margin offset range or the optional extended voltage offset range when the <i>Optional Voltage Offset Range</i> field in the READ_LANE_MARGIN_CAP Completion Metadata was set to 1b: 0b: Enables the mandatory Rx voltage offset range 1b: Enables the optional Rx voltage offset range This bit is reserved for Gen 4.
	12:6	Voltage Offset / Time Offset In a voltage margin test, this field sets the number of voltage offset steps. In a timing margin test, this field sets the number of time offset steps. Values larger than 1Fh are Reserved when performing a timing margin test.
	14:13	Error Counter 00b: NOP – no change in counter setup 01b: CLEAR – set the error counter to 0 and enable counter 10b: START – start counter, continue counting from last value 11b: STOP – stop counter, do not clear value This field affects the Error Counter for the Lanes that perform the test as selected by the <i>Lane Select</i> field. This field is Reserved if the target of the Port Operation supports destructive Time Margining.
	15	Select PAM3 Eye For a voltage / timing margin test on Gen 4 Link, this field selects the eye on which the measurement is done.: 0b: Measurement shall be done on lower eye 1b: Measurement shall be done on upper eye This field is Reserved if the Link is not Gen 4.
	16	Port Select This field indicate on which Port the Lane Margining is activated: 0b: Activate Lane Margining on this Port 1b: Activate Lane Margining on the Corresponding Port When using the Operation on a USB4 Router, this bit shall be set to 0b
	31:17	Reserved

Operation Completion

The Completion for this Operation does not have Completion Metadata.

The Completion Data for the RUN_SW_LANE_MARGINING Operation depicted in Table 8-87 contains the configuration for the SW test.

Table 8-878-86. RUN_SW_LANE_MARGINING Completion Data

DW	Bit(s)	Field Name and Description
0	2:0	Lane Select This field contains the value of the <i>Lane Select</i> field in the last RUN_SW_LANE_MARGINING Port Operation.
	3	Timing Margin Test This field contains the value of the <i>Timing Margin Test</i> field in the last RUN_SW_LANE_MARGINING Port Operation.
	4	Enable Margin Tests This field contains the value of the <i>Enable Margin Tests</i> field in the last RUN_SW_LANE_MARGINING Port Operation.
	5	Enable Optional Voltage Offset Range This field contains the value of the <i>Enable Optional Voltage Offset Range</i> field in the last RUN_SW_LANE_MARGINING Port Operation.
	12:6	Voltage Offset / Time Offset This field contains the value of the <i>Voltage Offset / Time Offset</i> field in the last RUN_SW_LANE_MARGINING Port Operation.
	13	Port Select This field contains the value of the <i>Port Select</i> field in the last RUN_SW_LANE_MARGINING Port Operation.
	31:14	Reserved

8.3.2.4.4 READ_SW_MARGIN_ERR (Conditional)

The READ_SW_MARGIN_ERR Port Operation reads the error indicators of a Receiver SW Lane Margining test.

A USB4 Port shall support the READ_SW_MARGIN_ERR Port Operation if hardware margining mode is not supported (see Section 3.1.6.1). If hardware margining mode is supported, support for this Port Operation is optional.

If the target of the Port Operation supports Destructive Time Margining, it shall set the Opcode register to a FourCC value of “!CMD”.

Operation Initiation

This Port Operation does not have Operation Metadata.

This Port Operation does not have Operation Data.

Operation Completion

If completed successfully, the Port Operation returns Length number of Doublewords of Completion Metadata.

The Completion for this Operation does not have Completion Data.

Table 8-888-87. READ_SW_MARGIN_ERR Completion Metadata

DW	Bit(s)	Field Name and Description
0	3:0	Error Counter (RX0) This field contains the number of samples with values below the voltage offset measured on RX0. The counter value increments from 0 and if <i>Extended Error Counter</i> is not supported, shall stop counting at Fh.

	7:4	Error Counter (RX1) This field contains the number of samples with values below the voltage offset measured on RX1. The counter value increments from 0 and if <i>Extended Error Counter</i> is not supported, and shall stop counting at Fh.
	11:8	Error Counter (RX2) This field contains the number of samples with values below the voltage offset measured on RX2. The counter value increments from 0 and if <i>Extended Error Counter</i> is not supported, shall stop counting at Fh.
	31:12	Reserved
1	11:0	Extended Error Counter (RX0) If supported (see <i>Extended Error Counter Support</i> field in Table 8-81), this field contain the 12 MSB of the Error Counter for RX0. Together with <i>Error Counter (RX0)</i> it contains the number of samples with values below the voltage offset measured on RX0. The counter shall stop counting at FFFFh.
	31:12	Reserved
2	11:0	Extended Error Counter (RX1) If supported (see <i>Extended Error Counter Support</i> field in Table 8-81), this field contain the 12 MSB of the Error Counter for RX1. Together with <i>Error Counter (RX1)</i> it contains the number of samples with values below the voltage offset measured on RX1. The counter shall stop counting at FFFFh.
	31:12	Reserved
3	11:0	Extended Error Counter (RX2) If supported (see <i>Extended Error Counter Support</i> field in Table 8-81), this field contain the 12 MSB of the Error Counter for RX2. Together with <i>Error Counter (RX2)</i> it contains the number of samples with values below the voltage offset measured on RX2. The counter shall stop counting at FFFFh.
	31:12	Reserved



CONNECTION MANAGER NOTE

If the READ_SW_MARGIN_ERR Operation runs a timing margin test, and the test is destructive, then following the execution of this Operation, the Connection Manager can bring the Router out of compliance mode by transitioning it to the Uninitialized state.

8.3.2.5 Query CLx Latency Tolerance (Conditional)

A USB4 Port that supports CLx Latency Tolerance Capability shall support the Query CLx Latency Tolerance Port Operation.

The Query CLx Latency Tolerance Port Operation is used to collect the recommended CLx Latency Threshold entries reported for the USB4 Routers and USB4 Re-Timer on the link topology, supporting up to four entries. Each CLx Latency Threshold entry describes a recommended timing margin beyond which the port will bring additional power saving merit. A CLx Latency Threshold entry may optionally provide the expected power saving when used. Based on these entries, Software can create a distribution plan for the overall available CLx Exit latency margins between the different components on constructing the link topology.

Note: When the total resulting CLx Latency exceeds the value of $t_{TrainingError}$, a port might initiate Gen4 Link Recovery in case **Gen 4 Link Recovery Avoidance Supported** is 0b, or in case it does not support CLx Latency Tolerance operation. It is recommended for software to disable Gen4 Link Recovery unless both router ports have **Gen 4 Link Recovery Avoidance Supported** set to 1b.

Operation Initiation

This Port Operation does not have Operation Data.

Operation Completion

Table 8-89 describes the Completion Metadata for this operation.

Table 8-89. Query CLx Latency Tolerance Completion Metadata

DW	Bit(s)	Field Name and Description
<u>0</u>	<u>15:0</u>	<p>CLx Exit Time Margin [1] – This field contains a time value in microseconds. This value is the first out of four possible entries, representing a requested time addition for port's CL1 or CL0s exit time. Each threshold brings power saving merit in CL1 or CL0s states in increased order and may be considered by software to be applied (by setting CLx Exit Time Margins using the Set CLx Latency Tolerance Port Operation).</p> <p>A value of 00h for this field is illegal.</p>
<u>0</u>	<u>22:16</u>	<p>CL0s Power Saving Ratio [1] – This field provides the percentage of additional CL0s power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [1], using the Set CLx Latency Tolerance Port Operation. The savings are described with respect to PCL0s, the ports baseline power consumption at CL0s state. For a given PSR (Power Saving Ratio) the expected power consumption is given by $(1-PSR) * PCL0s$.</p> <p>This field is optional. If unused shall be set to 00h. Allowed values:</p> <p>01h: Additional power saving of 1% when entering CL0s 02h: Additional power saving of 2% when entering CL0s ... 63h: Additional power saving of 99% when entering CL0s 64h-7F: Illegal values</p>
<u>0</u>	<u>23</u>	Reserved
<u>0</u>	<u>30:24</u>	<p>CL1 Power Saving Ratio [1] – This field provides the percentage of additional CL1 power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [1], using the Set CLx Latency Tolerance Port Operation. The savings are described with respect to PCL1, the ports baseline power consumption at CL1 state. For a given PSR (Power Saving Ratio) the expected power consumption is given by $(1-PSR) * PCL1$.</p> <p>This field is optional. If unused shall be set to 00h. Allowed values:</p> <p>01h: Additional power saving of 1% when entering CL1 02h: Additional power saving of 2% when entering CL1 ... 63h: Additional power saving of 99% when entering CL1 64h-7F: Illegal values</p>
<u>0</u>	<u>31</u>	Gen 4 Link Recovery Avoidance Supported – This field shall be set to 1b only for implementations that support avoiding the initiation of Gen 4 Link Recovery when exiting CL0s or CL1 due to a tTrainingError expiration. Otherwise, this field shall be set to 0b.
<u>1</u>	<u>15:0</u>	<p>CLx Exit Time Margin [2] – This field contains a time value in microseconds. This value is the 2nd out of the four possible thresholds as described for CLx Exit Time Margin [1].</p> <p>This field is optional. If unused shall be set to 00h.</p>

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<u>1</u>	<u>22:16</u>	<u>CL0s Power Saving Ratio [2] – This field provides the percentage of additional CL0s power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [1]., similar to CL0s Power Saving Ratio [1]</u>
<u>1</u>	<u>23</u>	<u>Reserved</u>
<u>1</u>	<u>30:24</u>	<u>CL1 Power Saving Ratio [2] – This field provides the percentage of additional CL1 power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [2]., similar to Power Saving Ratio [1].</u>
<u>1</u>	<u>31</u>	<u>Reserved</u>
<u>2</u>	<u>15:0</u>	<u>CLx Exit Time Margin [3] – This field contains a time value in microseconds. This value is the 3rd out of the four possible thresholds as described for CLx Exit Time Margin [1].</u> <u>This field is optional. If unused shall be set to 00h.</u>
<u>2</u>	<u>22:16</u>	<u>CL0s Power Saving Ratio [3] – This field provides the percentage of additional CL0s power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [3]., similar to CL0s Power Saving Ratio [1]</u>
<u>2</u>	<u>23</u>	<u>Reserved</u>
<u>2</u>	<u>30:24</u>	<u>CL1 Power Saving Ratio [3] – This field provides the percentage of additional CL1 power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [3]., similar to CL1 Power Saving Ratio [1].</u>
<u>2</u>	<u>31</u>	<u>Reserved</u>
<u>3</u>	<u>15:0</u>	<u>CLx Exit Time Margin [4] – This field contains a time value in microseconds. This value is the 4th out of the four possible thresholds as described for CLx Exit Time Margin [1].</u> <u>This field is optional. If unused shall be set to 00h.</u>
<u>3</u>	<u>22:16</u>	<u>CL0s Power Saving Ratio [4] – This field provides the percentage of additional CL0s power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [4]., similar to CL0s Power Saving Ratio [1]</u>
<u>3</u>	<u>23</u>	<u>Reserved</u>
<u>3</u>	<u>30:24</u>	<u>CL1 Power Saving Ratio [4] – This field provides the percentage of additional CL1 power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [4]., similar to CL1 Power Saving Ratio [1].</u>
<u>3</u>	<u>31</u>	<u>Reserved</u>

8.3.2.6 Set CLx Latency Tolerance (Optional)

A USB4 Port may optionally support the CLx Latency Tolerance Port Operation.

The CLx Latency Tolerance Port Operation is used to provide a USB4 Port extra timing margins to be used on any subsequent exit from CL0s or CL1. The provided CLx Exit Time Margins are the total extra time allowed for the USB4 Port to be distribute between the different transition states (or steps) beyond those defined in Table 4-73.

A USB4 Port that implements this optional capability shall exit CL0s or CL1 within at most “CLx Exit Time Margins” beyond the time defined under Section 4.2.1.6.5(Equation 4-3 to Equation 4-11). The port shall adhere to modifications to the CLx Exit Time Margins after being received (mainly considered after the values are reduced).

When the USB4 link disconnects, the “CLx Exit Time Margins” field returns to its default value (000h).

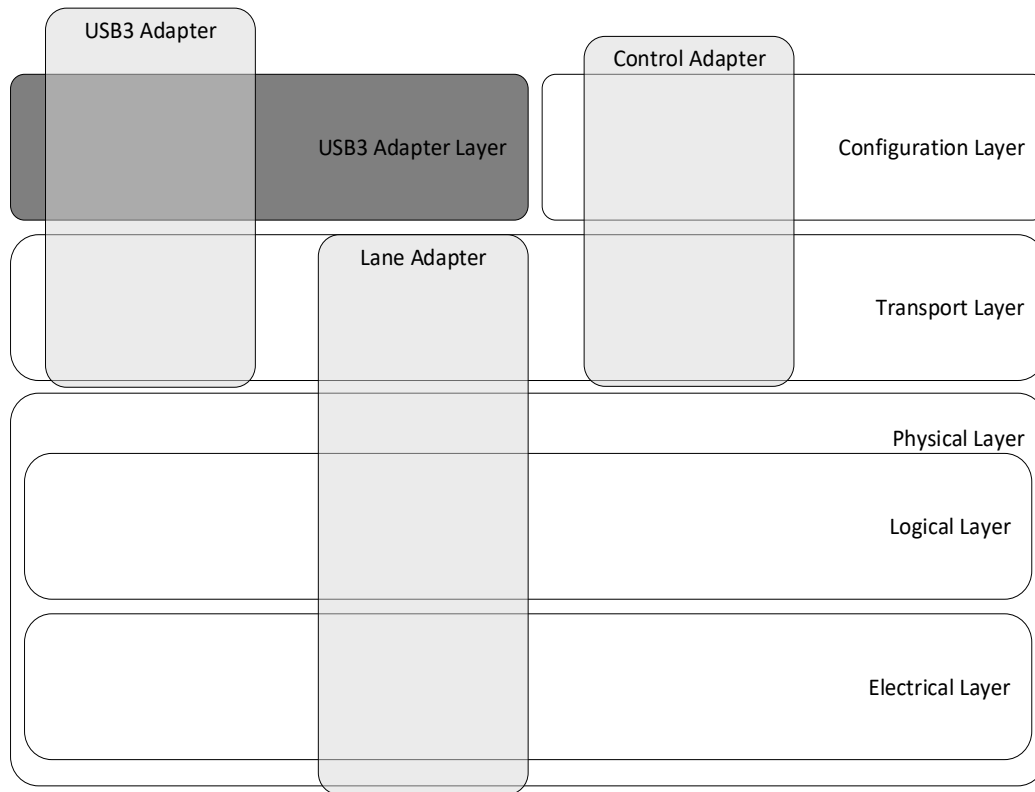
A port that operates in Gen 4 link rate shall not initiate Gen 4 Link Recovery in if both **Gen 4 Link Recovery Avoidance Supported** bit and **Gen 4 Link Recovery Avoidance Enabled** bit are set to 1b, and the tTrainingError timer expires when exiting CL0s or at Training state when exiting CL1 as defined in Section 4.2.1.6.5.4 and Section 4.2.1.6.5.1.2.

A port that implements this port operation and runs at Gen 4 link rate may avoid invoking Gen 4 Link Recovery at the expiration of tTrainingError time when exiting CL0s or CL1, when setting CLx Exit Time Margins to any value other than 000h

This Port Operation does not have Operation Data. The Operation Metadata for the SET CLX LATENCY TOL Port Operation is defined in Table 8-90.

Table 8-90. Set CLx Latency Tolerance Operation Metadata

DW	Bit(s)	Field Name and Description
0	10:0	CLx Exit Time Margins – Sets the additional time margin budget for the USB4 Port to use when exiting CL0s and CL1. The value of this field: 000h: No timing margins are allowed (feature is disable). This is the default value. Other values define the number of microseconds that may be added to the CL0s and CL1 exit time budget for the source.
0	30:11	Reserved
0	31	Gen 4 Link Recovery Avoidance Enable 0b: The port may avoid the initiation of Gen 4 Link Recovery when exiting CL0s or CL1 due to a tTrainingError expiration if CLx Exit Time Margins was set to any value other than 000h (default) 1b: The port shall avoid the initiation of Gen 4 Link Recovery when exiting CL0s or CL1 due to a tTrainingError expiration. Enabling this bit has no impact if Gen 4 Link Recovery Avoidance Supported is set to 1b

9 USB3 Tunneling**Gen X System Level Requirements****USB4® Hosts:**

A USB4 Host shall support USB3 Gen X tunneling. The Host Router in a USB4 Host shall have one Downstream USB3 Gen X Adapter per Downstream Facing Port. Each Downstream USB3 Gen X Adapter shall interface to a downstream port on the host controller.

USB4 Hubs:

A USB4 Hub shall support USB3 Gen X tunneling. A USB4 Hub shall incorporate an internal USB SuperSpeed Plus hub per the USB 3.2 Specification with the modifications defined in this chapter.

The Device Router in a USB4 Hub shall have:

- An Upstream USB3 Gen X Adapter that interfaces with the upstream port of the internal USB 3.2 hub.
- For each Downstream Facing Port, a Downstream USB3 Gen X Adapter that interfaces to a downstream port on the internal USB 3.2 hub.

USB4 Devices:

A USB4 Device may optionally support USB3 Gen X tunneling. A USB4 Device that supports USB3 Gen X tunneling shall incorporate either an internal USB SuperSpeed Plus hub or an internal USB peripheral device per the USB 3.2 Specification with the modifications defined in this chapter.

The Device Router in a USB4 Device that supports USB3 Gen X tunneling shall have an Upstream USB3 Gen X Adapter that interfaces to the upstream port of the internal USB 3.2 peripheral device or internal USB 3.2 hub.

Gen T System Level Requirements

USB4 Hosts:

A USB4 Host may optionally support USB3 Gen T tunneling. The Host Router in a USB4 Host that supports Gen T tunneling shall have at least one Downstream USB3 Gen T Adapter. In case the Host Router does not support full Gen T connectivity (*Gen T Full Connectivity Support* bit is set to 0b), it shall have one Downstream USB3 Gen T Adapter per USB4 Downstream Facing Port. Each Downstream USB3 Gen T Adapter shall interface to at least one downstream USB3 Gen T Port on the host controller.

USB4 Hubs and USB4-Based Docks:

A USB4-Based Dock may optionally support USB3 Gen T tunneling. A USB4-Based Dock that supports USB3 Gen T tunneling shall:

- Incorporate one or more USB3 Gen T Ports where each USB3 Gen T Port is connected to an Internal USB3 Gen T Peripheral.
- Have a single Upstream USB3 Gen T Adapter that interfaces to each of the USB3 Gen T Port(s).
- Support Gen X tunneling to all Internal USB3 Gen T Peripherals.
- Support native USB 3.2 operation to all Internal USB3 Gen T Peripherals.

Note: A USB4 Hub or USB4-Based Dock supports USB3 Gen T tunneling as a “pass through”, even if does not contain any USB3 Gen T Ports or a USB3 Gen T Adapter. Sections 9.1 through 9.5 only apply to USB4-Based Docks that support USB3 Gen T Tunneling by including a USB3 Gen T Adapter and USB3 Gen T Port(s) as described above. Section 9.6 applies to all USB4 Hubs and USB4-Based Docks.

USB4 Devices:

A USB4 Device may optionally support USB3 Gen T tunneling. A USB4 Device that supports USB3 Gen T tunneling shall:

- Incorporate one or more USB3 Gen T Ports where each USB3 Gen T Port is connected to an Internal USB3 Gen T Peripheral.
- Have a single Upstream USB3 Gen T Adapter that interfaces to each of the USB3 Gen T Port(s).
- Support Gen X tunneling to all Internal USB3 Gen T Peripherals.
- Support native USB 3.2 operation to all Internal USB3 Gen T Peripherals.

An Internal USB3 Hub shall not contain any USB3 Gen T Ports.

9.1 USB3 Adapter Layer

Note: The term “USB3 Adapter” is used to collectively refer to a USB3 Gen X Adapter and/or a USB3 Gen T Adapter.

9.1.1 Encapsulation

When a USB3 Adapter Layer receives one of the USB3 constructs listed in this section from the Internal USB3 Component, it encapsulates the construct in a Tunneled Packet then passes it to the Transport Layer for transmission over the USB4 fabric. The USB3 Adapter Layer encapsulates the USB3 constructs listed in Table 9-1.

Table 9-1. Encapsulated USB3 Constructs

USB3 Construct	USB3 Gen X Adapter	USB3 Gen T Adapter
Low Frequency Periodic Signaling (LFPS)	YES	NO
Ordered Sets	YES	NO
Link Commands	YES	YES
Link Management Packets (LMP)	YES	NO
Transaction Packets (TP)	YES	YES
Isochronous Timestamp Packets (ITP)	YES	YES
Data Packets (DP)	YES	YES
Nullified Data Packets	YES	YES
Out of Band Message (OOBM)	NO	YES

A USB3 Adapter Layer shall follow the rules below when encapsulating a USB3 construct into a Tunneled Packet:

- An LFPS event, an Ordered Set, an Out of Band Message, a Link Management Packet, a Transaction Packet, and an Isochronous Timestamp Packet shall each be encapsulated into a single separate Tunneled Packet.
- A Link Command for Gen X and a Coalesced Link Command for Gen T shall each be encapsulated into a single separate Tunneled Packet. See Section 9.1.1.3.
- A Data Packet shall be encapsulated into one or more Tunneled Packets. A Tunneled Packet shall not contain data from more than one Data Packet. See Section 9.1.1.8.
- Idle Symbols shall be discarded by the USB3 Adapter Layer.
- The byte and bit ordering of an LFPS within a Tunneled Packet shall be as described in Section 9.1.1.1.
- The byte and bit ordering of an Ordered Set within a Tunneled Packet shall be as described in Section 9.1.1.2.
- The byte and bit ordering of an Out of Band Message within a Tunneled Packet shall be as described in Section 9.1.1.10.
- The bytes and bits in a Tunneled Packet payload, other than LFPS, Out of Band Messages, and Ordered Sets, shall be packed in the same order as the original USB3 construct, including the USB3 framing symbols. The first byte (i.e. the least-significant byte of the encapsulated construct) is mapped to B0 in the Tunneled Packet payload (see Figure 4-20). Bits [7:0] in each byte of the encapsulated construct are mapped to bits [7:0], respectively, in the corresponding byte of the Tunneled Packet payload. Section 9.1.1.3.1 defines how a USB3 Link Command is mapped to a Tunneled Packet.

**IMPLEMENTATION NOTE**

The amount of buffering at the USB3 Adapter is implementation specific as it balances the tradeoff between USB3 Tunneling performance and USB3 link latency. It is recommended that implementations make the amount of buffers configurable.

The PDF field in a Tunneled Packet identifies the type of USB3 construct contained therein. Table 9-2 defines the PDF values that shall be used for each type of USB3 construct.

Table 9-2. PDF Values for USB3 Tunneling Packets

PDF	Type (Gen X)	Type (Gen T)	Payload of Tunneled Packet
0h	LFPS	OOBM	Indication for an LFPS sequence or Out of Band Message
1h	Ordered Set	Rsvd	One TS1, TS2, or SDS Ordered Set
2h	Link Commands		Gen X: One USB3 Link Command Gen T: One to Four USB3 Link Commands
3h	LMP / TP / ITP	TP / ITP	One LMP, TP, Deferred DPH, or ITP Header Packet
4h	Start DP Segment		The first segment of a USB3 Data Packet (DPH and DPP)
5h	Middle DP Segment		A segment of a USB3 Data Packet that is not the first segment and is not the last segment
6h	End DP Segment		The last segment of a USB3 Data Packet that is broken into more than one segment
7h	Rsvd	NDP	One DPH of a nullified USB3 Data Packet
8h – Dh		Rsvd	Reserved
Eh		PM Packet	Power Management Packet Payload. See Section 5.1.3.1.1
Fh		Rsvd	Reserved

If a USB3 Adapter receives a Tunneled Packet with a PDF value that is Rsvd, it shall discard the Tunneled Packet and shall not send any Packets in response.

9.1.1.1 LFPS Encapsulation (Gen X Only)

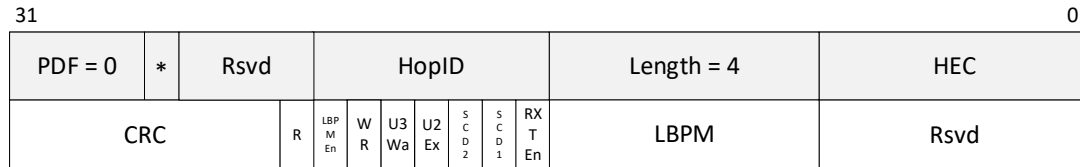
An LFPS Tunneled Packet shall contain a single Doubleword of payload as defined in Table 9-3 and shall have the structure shown in Figure 9-1. A USB3 Gen X Adapter Layer shall not transfer an LFPS event to the Transport Layer unless that event is listed in Table 9-3.

A USB3 Gen X Adapter Layer shall set no more than one of bits [22:17] in an LFPS Tunneled Packet to 1b.

Table 9-3. LFPS Tunneled Packet Payload

Bits	Name	Description
7:0	<i>Rsvd</i>	Reserved.
15:8	<i>LBPM</i>	Shall contain the LBPM PHY Capability byte. Only valid when the LBPM Enable bit is set to 1b.
16	<i>Rx Term Enable</i>	This bit represents the state of the local low-impedance receiver termination. It shall be set to 1b if the low-impedance receiver termination is on. It shall be set to 0b if the low-impedance receiver termination is off. In any LFPS packet, this bit shall represent the current value of the low-impedance receiver termination.
17	<i>SCD1</i>	Set to 1b following assertion of SCD1 by the Internal USB3 Component. Otherwise shall be set to 0b.
18	<i>SCD2</i>	Set to 1b following assertion of SCD2 by the Internal USB3 Component. Otherwise shall be set to 0b.
19	<i>U2 Exit</i>	Set to 1b following assertion of U2 Exit by the Internal USB3 Component. Otherwise shall be set to 0b.
20	<i>U3 Wakeup</i>	Set to 1b following assertion of U3 Wakeup by the Internal USB3 Component. Otherwise shall be set to 0b.
21	<i>Warm Reset</i>	Set to 1b following assertion of Warm Reset by the Internal USB3 Component. Otherwise shall be set to 0b.
22	<i>LBPM Enable</i>	Set to 1b following assertion of LBPM by the Internal USB3 Component. Otherwise shall be set to 0b.

23	<i>Rsvd</i>	Reserved.
31:24	<i>CRC</i>	Cyclic Redundancy Code covering bits [23:0] of the payload. It shall be calculated as defined in Section 9.1.1.1.1.

Figure 9-1. LFPS Tunneled Packet Format

* SupplID

9.1.1.1.1 CRC

The *CRC* field shall cover bits [23:0] of payload. It shall be calculated as defined in Section 5.1.2.1.1, using the following bit order:

1. Bit 7 to bit 0
2. Bit 15 to bit 8
3. Bit 23 to bit 16

When a USB3 Gen X Adapter Layer receives an LFPS Tunneled Packet, it shall verify the *CRC* field value. The USB3 Gen X Adapter Layer may correct single-bit errors in the LFPS Tunneled Packet payload. After correcting an error, a Router shall continue on as if the error had never occurred. When an error is detected but not corrected, the packet with the error shall be dropped and no other action taken on its behalf.

See Appendix A for example CRC calculations.

9.1.1.1.2 Rx Term Enable

The USB3 Gen X Adapter Layer shall send an LFPS Tunneled Packet to the Transport Layer when the local value of Rx termination changes or when the *Path Enable* bit in the USB3 Gen X Adapter Configuration Capability changes from 0b to 1b. The packet shall be sent 3 times.

A Router shall implement a mechanism that allows a USB3 Gen X Adapter Layer to indicate far-end receiver termination to the Internal USB3 Component.

When a Router is not in sleep state and is not in the process of transitioning into or out of sleep state, a USB3 Gen X Adapter Layer shall indicate far-end receiver termination to the Internal USB3 Component when all the following are true:

- Path Setup is complete
- The USB3 Gen X Adapter Layer received an LFPS Tunneled Packet with the *Rx Term Enable* bit set to 1b and the USB3 Gen X Adapter Layer has not received any subsequent LFPS Tunneled Packets with the *Rx Term Enable* bit set to 0b.

When a Router transitions to sleep state, a USB3 Gen X Adapter Layer shall maintain the same indicator value as before entry to sleep state. The USB3 Gen X Adapter Layer shall continue to maintain the indicator value until either:

- The Valid bit in the USB3 Gen X Adapter Configuration Capability is set to 1b after the Router exits sleep state. After the Valid bit is set to 1b, the USB3 Gen X Adapter Layer shall set the indicator as defined above.

- A disconnect on the paired USB4 Port occurs. If a disconnect occurs on the paired USB4 Port, the USB3 Gen X Adapter Layer may set the Path Established indicator to false.

9.1.1.1.3 SCD1

The USB3 Gen X Adapter Layer shall send an LFPS Tunneled Packet to the Transport Layer with the *SCD1* bit set to 1b when instructed to do so by the Internal USB3 Component. The packet shall be sent 3 times.

A USB3 Gen X Adapter Layer that receives an LFPS Tunneled Packet from the Transport Layer with the *SCD1* bit set to 1b shall indicate reception of SCD1 to the Internal USB3 Component until it receives a Tunneled Packet with different contents.

9.1.1.1.4 SCD2

The USB3 Gen X Adapter Layer shall send an LFPS Tunneled Packet to the Transport Layer with the *SCD2* bit set to 1b when instructed to do so by the Internal USB3 Component. The packet shall be sent 3 times.

A USB3 Gen X Adapter Layer that receives an LFPS Tunneled Packet from the Transport Layer with the *SCD2* bit set to 1b shall indicate reception of SCD2 to the Internal USB3 Component until it receives a Tunneled Packet with different contents.

9.1.1.1.5 U2 Exit

The USB3 Gen X Adapter Layer shall send an LFPS Tunneled Packet to the Transport Layer with the *U2 Exit* bit set to 1b when the Internal USB3 Component indicates a U2 Exit event. The packet shall be sent 3 times.

A USB3 Gen X Adapter Layer that receives an LFPS Tunneled Packet from the Transport Layer with the *U2 Exit* bit set to 1b shall indicate reception of a U2 Exit LFPS to the Internal USB3 Component until it receives a Tunneled Packet with different contents.

9.1.1.1.6 U3 Wakeup

When the Internal USB3 Component indicates the start of a U3 Wakeup event and a USB3 Gen X Path is enabled, a USB3 Gen X Adapter Layer shall send 3 LFPS Tunneled Packets to the Transport Layer. Each LFPS Tunneled Packet shall have the *U3 Wakeup* bit set to 1b.

If a USB3 Gen X Adapter Layer detects the beginning of a U3 Wakeup event before a USB3 Gen X Path is enabled, it shall ignore the USB3 Wakeup event and shall not send any LFPS Tunneled Packets for that event.

The USB3 Gen X Adapter Layer may send an LFPS Tunneled Packet with the *U3 Wakeup* bit set to 0b to the Transport Layer when the Internal USB3 Component starts to transmit SS signaling.

A USB3 Gen X Adapter Layer that receives an LFPS Tunneled Packet from the Transport Layer with the *U3 Wakeup* bit set to 1b shall indicate reception of a U3 Wakeup LFPS to the Internal USB3 Component until it receives a Tunneled Packet with different contents.

9.1.1.1.7 Warm Reset

When Warm Reset is asserted by the Internal USB3 Component, the Downstream USB3 Gen X Adapter Layer shall:

- Discard any queued Tunneled Packets.

Note: Only Tunneled Packets in the USB3 Gen X Adapter Layer are discarded. A Tunneled Packet that is passed to the Transport Layer before Warm Reset is asserted may still be transmitted.

- Send an LFPS Tunneled Packet to the Transport Layer with the *Warm Reset* bit set to 1b. The packet shall be sent 3 times.

While Warm Reset is active, a Downstream USB3 Gen X Adapter shall discard any Tunnel Packets it receives and clear any indication of LFPS reception towards the Internal USB3 Component.

An Upstream USB3 Gen X Adapter Layer that receives an LFPS Tunneled Packet with the *Warm Reset* bit set to 1b shall indicate assertion of a Warm Reset to the Internal USB3 Component until it receives a Tunneled Packet with different contents.

The Downstream USB3 Gen X Adapter Layer shall send an LFPS Tunneled Packet to the Transport Layer with the *Warm Reset* bit set to 0b when Warm Reset is de-asserted by the Internal USB3 Component. The packet shall be sent 3 times.

An Upstream USB3 Gen X Adapter Layer that receives an LFPS Tunneled Packet from the Transport Layer with the *Warm Reset* bit set to 0b shall indicate de-assertion of a Warm Reset to the Internal USB3 Component until it receives a Tunneled Packet with different contents.

After Warm Reset is de-asserted, a USB3 Gen X Adapter Layer shall not forward any Ordered Sets, packets, or events to the Internal USB3 Component that were received before or during Warm Reset assertion.

Note: The duration between the received Tunneled Packets with the Warm Reset bit set to 1b and the received Tunneled Packets with the Warm Reset bit set to 0b can be smaller than t_{Reset} as defined in the USB 3.2 Specification.

9.1.1.1.8 LBPM

The USB3 Gen X Adapter Layer shall send an LFPS Tunneled Packet to the Transport Layer with the *LBPM Enable* bit set to 1b when instructed to do so by the Internal USB3 Component. The *LBPM* field shall contain the USB3 LBPM construct. Bits[7:0] of the USB3 LBPM are mapped to Bits[7:0] of the *LBPM* field, respectively. The LFPS Tunneled Packet shall be sent 3 times.

A USB3 Gen X Adapter Layer that receives an LFPS Tunneled Packet with the *LBPM Enable* bit set to 1b shall do the following until it receives a Tunneled Packet with different contents:

- Indicate reception of LBPM to the Internal USB3 Component.
- Communicate the value in the *LBPM* field to the Internal USB3 Component.



IMPLEMENTATION NOTE

Part of the ecosystem depends on a sufficient delay between states when performing USB3 Link Training over the tunnel. To ensure interoperability, it is recommended to follow the following delays:

- *After sending PHY Capabilities LFPS, wait at least 230us before sending the PHY Ready LFPS*
- *After sending PHY Ready LFPS, wait at least 170us before sending TS1*

9.1.1.1.9 LFPS Stop

A USB3 Gen X Adapter Layer shall send an LFPS Tunneled Packet to the Transport Layer with bits [22:17] set to 00h for the following cases:

- The Internal USB3 Component indicates no LFPS Response Timeout for U3 Exit.
- The Internal USB3 Component indicates Warm Reset done.

It is recommended that a USB3 Gen X Adapter Layer send an LFPS Tunneled Packet to the Transport Layer with bits [22:17] set to 00h for the following cases:

- The Internal USB3 Component indicates a Polling LFPS Timeout.
- The Internal USB3 Component indicates no LFPS Response Timeout for U2 Exit.

The LFPS Tunneled Packet shall be sent 3 times.

9.1.1.2 Ordered Set Encapsulation (Gen X Only)

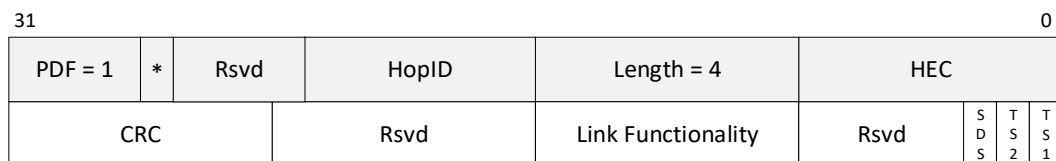
An Ordered Set Tunneled Packet shall have the single Doubleword payload defined in Table 9-4 and shall have the structure shown in Figure 9-2.

A USB3 Gen X Adapter Layer shall set one and no more than one of bits [2:0] in an Ordered Set Tunneled Packet.

Table 9-4. Ordered Set Tunneled Packet Payload

Bits	Name	Description
0	TS1	Set to 1b after a TS1 Ordered Set or a TSEQ Ordered Set is received from the Internal USB3 Component. Otherwise shall be set to 0b.
1	TS2	Set to 1b after a TS2 Ordered Set is received from the Internal USB3 Component. Otherwise shall be set to 0b.
2	SDS	Set to 1b after a SDS Ordered Set is received from the Internal USB3 Component. Otherwise shall be set to 0b.
7:3	Rsvd	Reserved.
15:8	Link Functionality	TS1 or TS2 Ordered Sets – Shall contain the USB3 Link Functionality construct. Bits[7:0] of the USB3 Link Functionality are mapped to Bits[7:0] of the <i>Link Functionality</i> field, respectively. TSEQ Ordered Set – set to 00h by the USB3 Gen X Adapter Layer. SDS Ordered Set – set to 00h by the USB3 Gen X Adapter Layer.
23:16	Rsvd	Reserved.
31:24	CRC	Cyclic Redundancy Code covering bits[23:0] of the payload. It shall be calculated as defined in Section 9.1.1.1.1.

Figure 9-2. Ordered Set Tunneled Packet Format



* SupplID

When a USB3 Gen X Adapter Layer receives a TSEQ, TS1, TS2, or SDS Ordered Set from the USB3 Gen X Port that is not identical to the previous Ordered Set received from the USB3 Gen X Port, it shall send 3 copies of an Ordered Set Tunneled Packet to the Transport Layer, with the fields set as defined in Table 9-4.

Note: TSEQ Ordered Sets are used by the Internal USB3 Component for synchronization. They are not needed on USB4. However, a receiving Internal USB3 Component cannot be idle during the time when TSEQ are normally transmitted, so USB4 treats a TSEQ Ordered Set the same as a TS1 Ordered Set.

All other Ordered Sets received from the Internal USB3 Component shall be discarded by the USB3 Gen X Adapter Layer and shall not cause an Ordered Set Tunneled Packet to be sent to the Transport Layer.

A USB3 Gen X Adapter Layer shall only send Ordered Sets that target Lane 0 to the Transport Layer. A USB3 Gen X Adapter Layer shall discard Ordered Sets that target Lane 1 so that they are not sent over the USB4 Fabric.

When a USB3 Gen X Adapter Layer receives an Ordered Set Tunneled Packet, it shall verify the CRC field value. The USB3 Gen X Adapter Layer may correct single-bit errors in the Ordered Set Tunneled Packet payload. After correcting an error, a Router shall continue as if the error had never occurred. When an error is detected but not corrected, the packet with the error shall be dropped and no other action taken on its behalf.

After verifying the CRC field value, a USB3 Gen X Adapter Layer shall:

- If the *TS1* bit in the received Ordered Set Tunneled Packet is set to 1b, indicate reception of TS1 Ordered Set to the Internal USB3 Component.
- If the *TS2* bit in the received Ordered Set Tunneled Packet is set to 1b, indicate reception of TS2 Ordered Set to the Internal USB3 Component.
- If the *SDS* bit in the received Ordered Set Tunneled Packet is set to 1b, indicate reception of SDS Ordered Set to the Internal USB3 Component.
- Communicate the value in the *Link Functionality* field to the Internal USB3 Component.

9.1.1.3 Link Command Encapsulation

9.1.1.3.1 Gen X Link Command Encapsulation

A USB3 Gen X Adapter Layer that receives a Link Command from the Internal USB3 Component shall send a Link Command Tunneled Packet to the Transport Layer with a 2-Doubleword payload. The payload shall contain the Link Command.

Upon receiving a Link Command Tunneled Packet from the Transport Layer, a USB3 Gen X Adapter Layer shall transfer the Link Command Tunneled Packet to the Internal USB3 Component.

Figure 9-3. Gen X Link Command Tunneled Packet Format

31						0
PDF = 2	*	Rsvd	HopID	Length = 8	HEC	
SLC		SLC	SLC	EPF		
Link Command Word Byte 0		Link Command Word Byte 1	Link Command Word Byte 0	Link Command Word Byte 1		

* SupplD

9.1.1.3.2 Gen T Link Command Encapsulation

A Gen T Adapter that receives a Coalesced Link Command from the Internal USB3 Component shall send a Link Command Tunneled Packet with one of the formats shown in Figure 9-4. Figure 9-4A shows the encapsulation of a Coalesced Link Command that is comprised of a single doubleword. Figure 9-4B shows the encapsulation of a Coalesced Link Command that is comprised of two doublewords. The Coalesced Link Command is defined in Section 9.4.1.5.

Figure 9-4. Gen T Link Command Tunneled Packet Formats

31						0
PDF = 2	*	Rsvd	HopID	Length = 4	HEC	
DW0.Word0 [7:0]		DW0.Word0 [15:8]	DW0.Word1[7:0]	DW0.Word1 [15:8]		

A) Coalesced Link Command with 1 DW

31						0
PDF = 2	*	Rsvd	HopID	Length = 8	HEC	
DW0.Word0 [7:0]		DW0.Word0 [15:8]	DW0.Word1[7:0]	DW0.Word1 [15:8]		
DW1.Word0 [7:0]		DW1.Word0 [15:8]	DW1.Word1[7:0]	DW1.Word1 [15:8]		

* SupplD

B) Coalesced Link Command with 2 DWs

Upon receiving a Link Command Tunneled Packet from the Transport Layer, a USB3 Gen T Adapter Layer shall extract the Coalesced Link Command from the Tunneled Packet and send the Coalesced Link Command to the Internal USB3 Component.

9.1.1.4 Idle Symbols

A USB3 Adapter Layer shall drop any Idle Symbols received from the Internal USB3 Component.

**IMPLEMENTATION NOTE**

A USB3 Adapter Layer can send Idle symbols to an Internal USB3 Component as needed to maintain the expected behavior of the Internal USB3 Component. For example:

- *A USB3 Adapter Layer may send Idle Symbols towards the Internal USB3 Component while in U0 whenever no other Symbols are sent to the Internal USB3 Component.*
- *A USB3 Adapter Layer may send 16 Idle Symbols towards the Internal USB3 Component after it sends an SDS Ordered Set to the Internal USB3 Component.*

9.1.1.5 LMP Encapsulation (Gen X Only)

A USB3 Gen X Adapter Layer that receives a USB3 Link Management Packet (LMP) from the Internal USB3 Component shall send an LMP Tunneled Packet to the Transport Layer with a 5-Doubleword payload. The payload shall contain the framed (see Section 7.2.1.1.1 in the USB 3.2 Specification) LMP.

Upon receiving an LMP Tunneled Packet from the Transport Layer, a USB3 Gen X Adapter Layer shall transfer the LMP to the Internal USB3 Component.

9.1.1.6 TP Encapsulation

A USB3 Adapter Layer that receives a USB3 Transaction Packet (TP) from the Internal USB3 Component shall send a TP Tunneled Packet to the Transport Layer. For a USB3 Gen X Adapter Layer, the payload shall contain the framed TP (see Section 7.2.1.1.1 in the USB 3.2 Specification for more information on framing).

If the USB3 Adapter Layer, receives a Deferred DPH from the Internal USB3 Component, it shall send a TP Tunneled Packet to the Transport Layer. For a USB3 Gen X Adapter Layer, the payload shall contain the Deferred DPH and its USB3 framing symbols.

Upon receiving a TP Tunneled Packet from the Transport Layer, a USB3 Adapter Layer shall transfer the TP to the Internal USB3 Component.

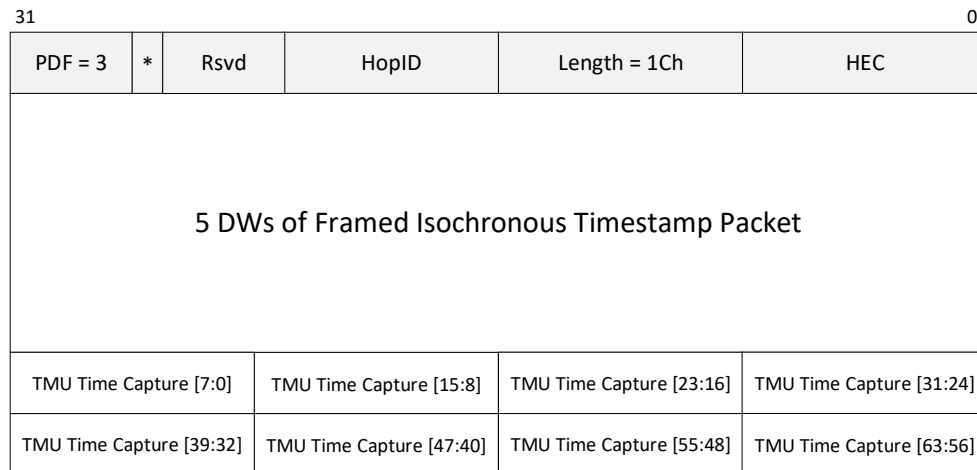
9.1.1.7 ITP Encapsulation

A Downstream USB3 Adapter Layer that receives an Isochronous Timestamp Packet (ITP) from the Internal USB3 Component shall:

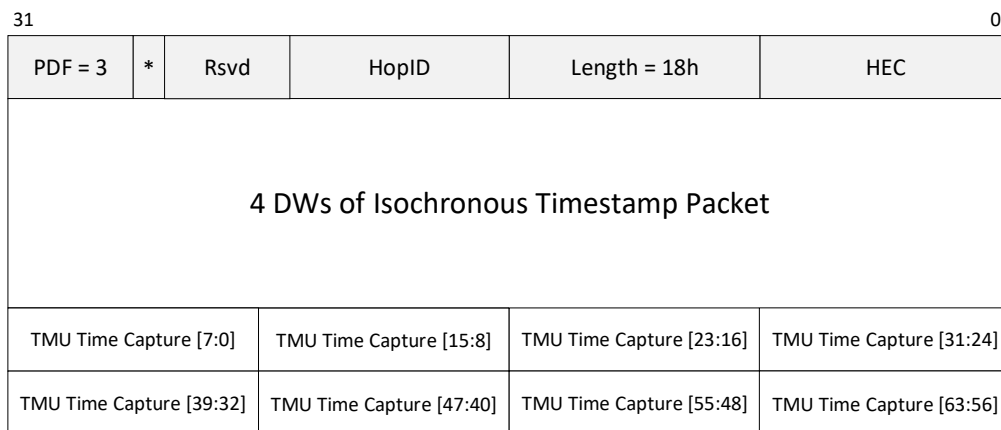
1. Set the *TMU Time Capture* field to the nanosecond portion of the current Host Router Time.

Note: If the Domain operates in Inter-Domain mode and it is a follower, then the Host Router Time refers to the Inter-Domain Host Router Time defined in Section 7.4.2. Otherwise, it refers to Host Router Time defined in Section 7.4.1.

2. Send an ITP Tunneled Packet with the format defined in Figure 9-5 (for Gen X) or Figure 9-6 (for Gen T) to the Transport Layer. The payload contains the ITP, followed by 2 Doublewords of the *TMU Time Capture* field. For a USB3 Gen X Adapter Layer, the ITP shall include the four framing symbols (see Section 7.2.1.1.1 in the USB 3.2 Specification).

Figure 9-5. Gen X ITP Tunneled Packet Format

* SupplID

Figure 9-6. Gen T ITP Tunneled Packet Format

* SupplID

An Upstream USB3 Adapter Layer that receives an ITP Tunneled Packet from the Transport Layer shall:

1. If the Router does not support the Time Synchronization Protocol, proceed to step 4.
2. Else, update the *Delta* field of the ITP according to the formula below:
 - Updated *Delta* = *Delta* + (Host Router Time Nanosecond – TMU Time Capture) / *tlsochTimeStampGranularity*.

Note: *tlsochTimeStampGranularity* is defined in the USB 3.2 Specification.

Note: If the Domain operates in Inter-Domain mode and it is a follower, then the Host Router Time refers to the Inter-Domain Host Router Time defined in Section 7.4.2. Otherwise, it refers to Host Router Time defined in Section 7.4.1.

- A USB3 Adapter Layer shall meet the required accuracy of the *Delta* field in the ITP as defined by Section 8.7 of the USB 3.2 Specification.
3. If the Adapter Layer is a USB3 Gen X Adapter Layer, update the *CRC-16* field in the ITP.
4. Forward the ITP to the Internal USB3 Component.

If the *Time Disruption* bit is set to 1b in Router Configuration Space, an Upstream USB3 Adapter Layer shall set the *Delayed* bit in the Link Control Word to 1b.

If the *Time Disruption* bit is set to 0b, an Upstream USB3 Adapter Layer may set the *Delayed* bit to 1b. The decision when to set the *Delayed* bit is implementation specific.

A USB3 Gen X Adapter Layer shall recalculate the *CRC-5* field within the Link Control Word if it modified the *Delayed* bit.



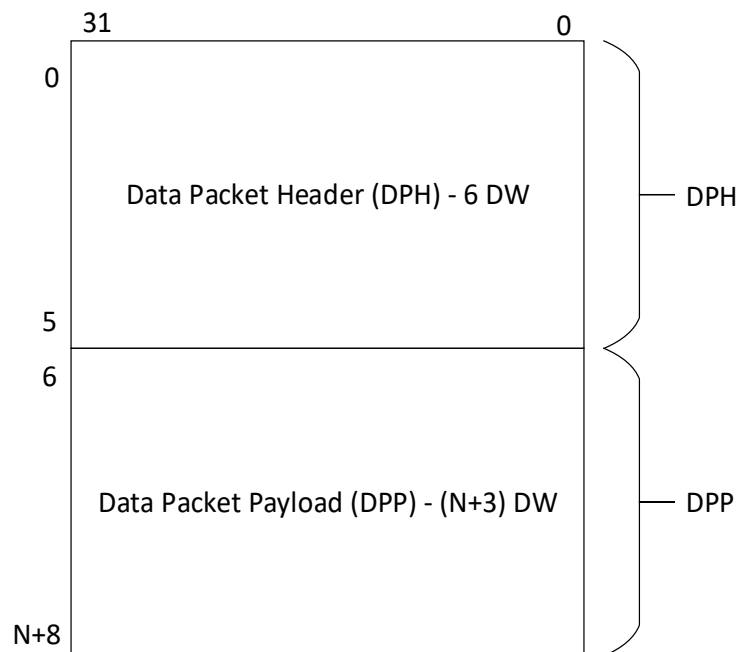
IMPLEMENTATION NOTE

It is recommended that the TMU in a Router sample time as close as possible to the Internal USB3 Component.

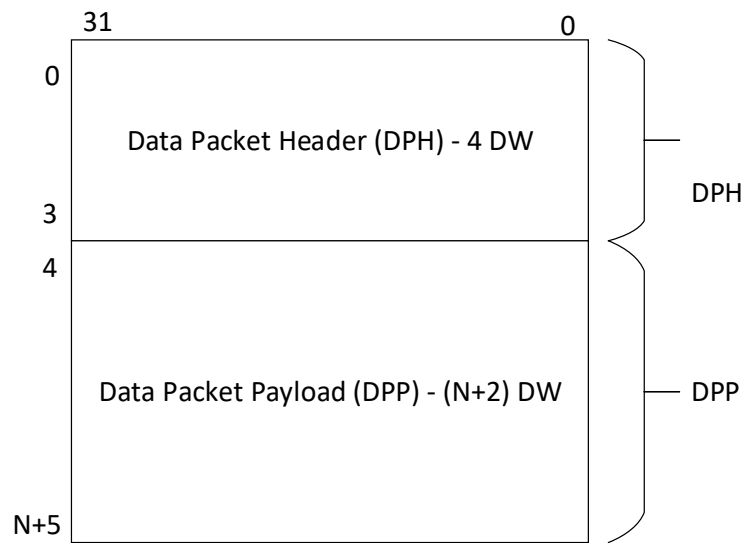
9.1.1.8 Data Packet (DP) Encapsulation

A USB3 Adapter Layer segments a USB3 Data Packet and its USB3 framing symbols into one or more Tunneled Packets for transport over the USB4 Fabric. Before segmentation, the USB3 Data Packet includes the Data Packet Header (DPH) and the Data Packet Payload (DPP) as depicted in Figure 9-7 (for Gen X) or Figure 9-8 (for Gen T). The USB3 framing symbols for Gen T are defined in Section 9.4.1.1.

Figure 9-7. Structure of an Unsegmented USB3 Data Packet (Gen X)



N = Number of data Doublewords.
DPP could have any Byte alignment

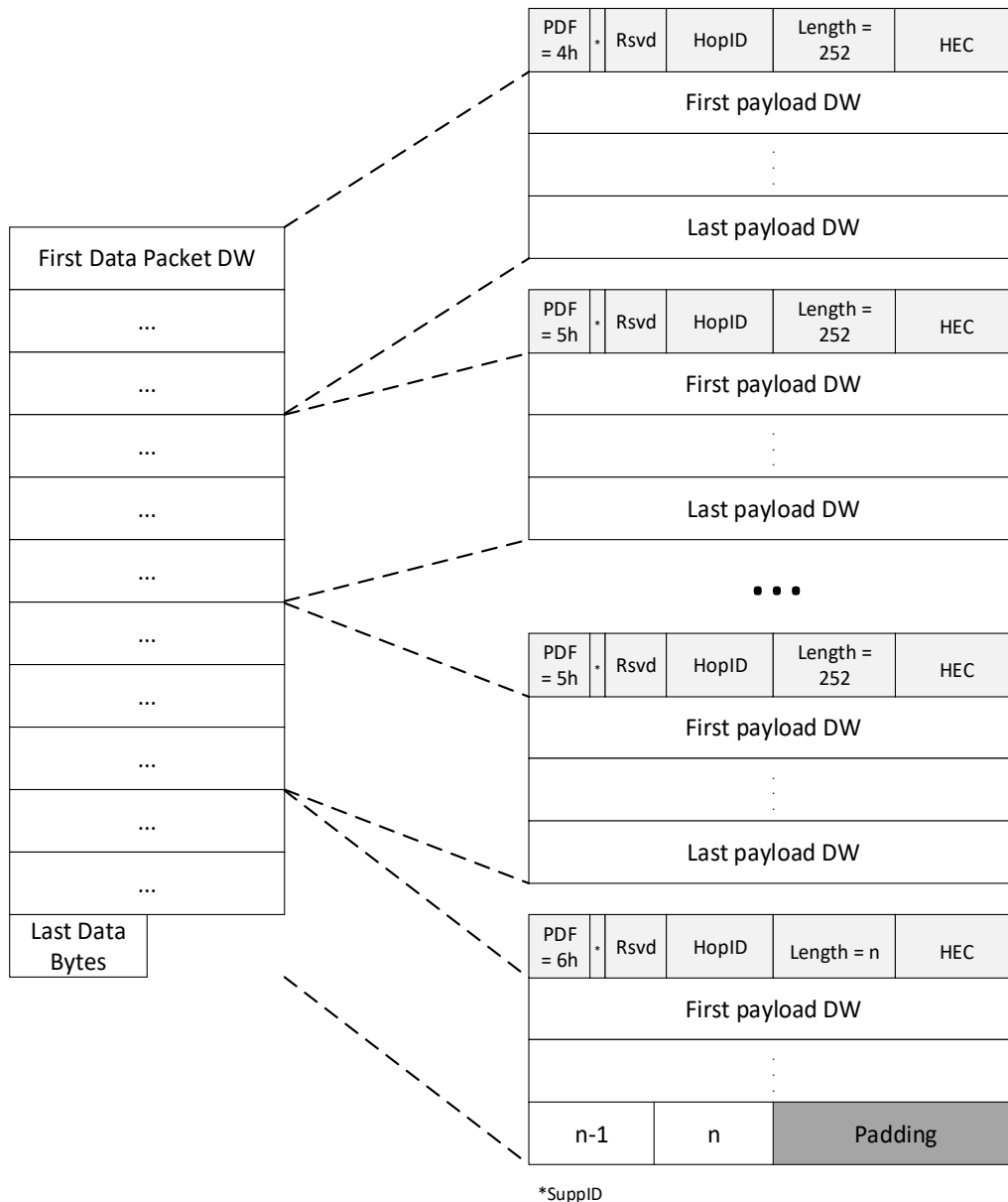
Figure 9-8. Structure of an Unsegmented USB3 Data Packet (Gen T)

N = Number of data Doublewords.
DPP could have any Byte alignment

If the size of a USB3 Data Packet is 252 bytes or less, then the USB3 Adapter Layer shall send a single Tunneled Packet of type *Start DP Segment* to the Transport Layer. The Tunneled Packet shall carry the unsegmented USB3 Data Packet as payload and any padding needed for DW alignment.

If the size of a USB3 Data Packet is larger than 252 bytes, the USB3 Data Packet shall be segmented into multiple Tunneled Packets as shown in Figure 9-9. When a USB3 Adapter Layer segments a USB3 Data Packet into Multiple Tunneled Packets, it shall follow the rules below:

- All Tunneled Packets with the possible exception of the last packet shall include 252 bytes of payload.
- The first Tunneled Packet shall be of type *Start DP Segment*.
- Any following Tunneled Packets other than the last Tunneled Packet shall be of type *Middle DP Segment*.
- The last Tunneled Packet shall:
 - Be of type *End DP Segment*.
 - Pad the payload to be Doubleword aligned.
 - Payload size shall not exceed 252 bytes.
- The Tunneled Packets shall be sent to the Transport Layer such that the byte ordering of the original USB3 Data Packet is maintained.

Figure 9-9. Segmentation of a USB3 Data Packet

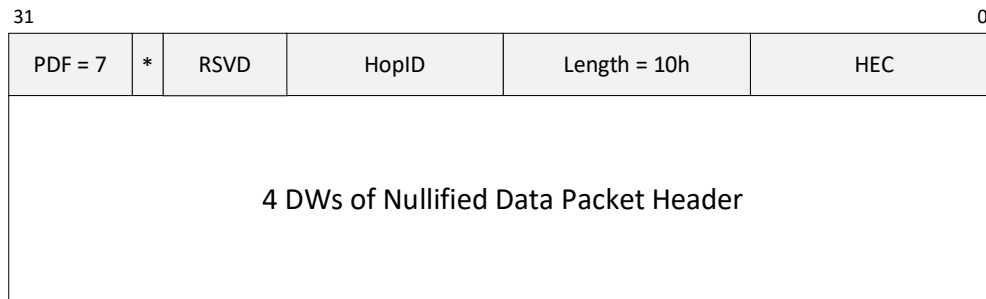
When re-assembling Tunneled Packets into USB3 Data Packets, the USB3 Adapter Layer shall:

- Drop a Tunneled Packet of type *Middle DP Segment* that comes immediately after a Tunneled Packet of type *End DP Segment*.
- Drop a Tunneled Packet of type *End DP Segment* that comes immediately after a Tunneled Packet of type *End DP Segment*.
- Nullify or partially nullify a USB3 Data Packet when both of the following are true:
 - A Tunneled Packet of type *Start DP Segment* is received and the length information in the USB3 DPH indicates it does not fit into a single Tunneled Packet.
 - A Tunneled Packet of type *End DP Segment* is not received within tReassemble from the reception of the Tunneled Packet of type *Start DP Segment*.

9.1.1.9 Nullified DP (Gen T Only)

A USB3 Gen T Adapter Layer that receives a nullified USB3 Data Packet (NDP) from the Internal USB3 Component shall send an NDP Tunneled Packet to the Transport Layer, while a partially nullified USB3 Data Packet is encapsulated as a Data Packet (DP). The NDP Tunneled Packet structure is shown in Figure 9-10.

Upon receiving an NDP Tunneled Packet from the Transport Layer, a USB3 Gen T Adapter Layer shall transfer the nullified USB3 Data Packet to the Internal USB3 Component.

Figure 9-10. Tunneled NDP Packet Format

* SupplD

9.1.1.10 OOBM Encapsulation (Gen T Only)

A USB3 Gen T Adapter Layer sends an OOBM Tunnel Packet for the following out of band message indications:

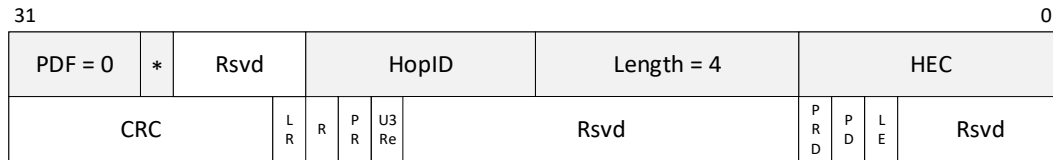
- *Link Error*
- *Port Disabled*
- *Port Reset Done*
- *U3 Resume*
- *Port Reset*
- *Link Ready*

An OOBM Tunneled Packet shall contain a single Doubleword of payload as defined in Table 9-5 and shall have the structure shown in Figure 9-11. A USB3 Gen T Adapter shall only set one of bits 5, 6, 7, 20, 21, and 23 in an OOBM Tunneled Packet payload.

Table 9-5. OOBM Tunneled Packet Payload

Bits	Name	Description
4:0	<i>Rsvd</i>	Reserved.
5	<i>Link Error</i>	Set to 1b to indicate that the device LTSSM transitioned into the ERROR state.
6	<i>Port Disabled</i>	Set to 1b to indicate that the LTSSM transitioned into the DISABLED state.
7	<i>Port Reset Done</i>	Set to 1b to indicate that device transmitter and receiver reset is complete.
19:8	<i>Rsvd</i>	Reserved.
20	<i>U3 Resume</i>	Set to 1b following assertion of U3 Wakeup by the Internal USB3 Component.
21	<i>Port Reset</i>	Set to 1b following assertion of Warm Reset by the Internal USB3 Component.
22	<i>Rsvd</i>	Reserved.
23	<i>Link Ready</i>	Set to 1b to indicate that USB3 Gen T Adapter and Internal USB3 Component transmitter and receiver are ready.

Bits	Name	Description
31:24	<i>CRC</i>	Cyclic Redundancy Code covering bits [23:0] of the payload. The CRC shall be calculated as defined in Section 9.1.1.1.1.

Figure 9-11. OOBM Packet Format

* SupplD

9.1.1.10.1 CRC

The *CRC* field shall be calculated as defined in Section 9.1.1.1.1, using the following bit order:

1. Bit 7 to bit 0
2. Bit 15 to bit 8
3. Bit 23 to bit 16

When a USB3 Gen T Adapter Layer receives an OOBM Tunneled Packet, it shall verify the *CRC* field value. The USB3 Gen T Adapter Layer may correct single-bit errors in the OOBM Tunneled Packet payload. After correcting an error, a Router shall continue on as if the error had never occurred. When an error is detected but not corrected, the packet with the error shall be dropped and no other action taken on its behalf.

9.1.1.10.2 Link Error

An Upstream USB3 Gen T Adapter Layer shall send an OOBM Tunneled Packet to the Transport Layer with the *Link Error* bit set to 1b when it receives a link error indication from the Internal USB3 Component.

When a Downstream USB3 Gen T Adapter Layer receives an OOBM Tunneled Packet from the Transport Layer with the *Link Error* bit set to 1b, it shall indicate reception of link error to the Internal USB3 Component.

9.1.1.10.3 Port Disabled

A USB3 Gen T Adapter Layer shall send an OOBM Tunneled Packet to the Transport Layer with the *Port Disabled* bit set to 1b when it receives a port disabled indication from the Internal USB3 Component.

When a USB3 Gen T Adapter Layer receives an OOBM Tunneled Packet from the Transport Layer with the *Port Disabled* bit set to 1b, it shall indicate reception of port disabled to the Internal USB3 Component.

9.1.1.10.4 Port Reset Done

An Upstream USB3 Gen T Adapter Layer shall send an OOBM Tunneled Packet to the Transport Layer with the *Port Reset Done* bit set to 1b when it receives a port reset done indication from the Internal USB3 Component.

When a Downstream USB3 Gen T Adapter Layer receives an OOBM Tunneled Packet from the Transport Layer with the *Port Reset Done* bit set to 1b, it shall indicate reception of port reset done to the Internal USB3 Component.

9.1.1.10.5 U3 Resume

An Upstream USB3 Gen T Adapter Layer shall send an OOBM Tunneled Packet to the Transport Layer with the *U3 Resume* bit set to 1b when it receives a U3 resume indication from the Internal USB3 Component.

When a Downstream USB3 Gen T Adapter Layer receives an OOBM Tunneled Packet from the Transport Layer with the *U3 Resume* bit set to 1b, it shall indicate reception of U3 resume to the Internal USB3 Component.

9.1.1.10.6 Port Reset

A Downstream USB3 Gen T Adapter Layer shall send an OOBM Tunneled Packet to the Transport Layer with the *Port Reset* bit set to 1b when it receives a port reset indication from the Internal USB3 Component.

When an Upstream USB3 Gen T Adapter Layer receives an OOBM Tunneled Packet from the Transport Layer with the *Port Reset* bit set to 1b, it shall indicate reception of port reset to the Internal USB3 Component.

9.1.1.10.7 Link Ready

A USB3 Gen T Adapter Layer shall send an OOBM Tunneled Packet to the Transport Layer with the *Link Ready* bit set to 1b when it receives a link ready indication from the Internal USB3 Component.

When a USB3 Gen T Adapter Layer receives an OOBM Tunneled Packet from the Transport Layer with the *Link Ready* bit set to 1b, it shall indicate reception of link ready to the Internal USB3 Component.

9.1.2 Bandwidth Negotiation (Gen X Only)

A Host Router uses the *Consumed Upstream Bandwidth*, *Consumed Downstream Bandwidth*, *Allocated Upstream Bandwidth*, and *Allocated Downstream Bandwidth* fields in the USB3 Gen X Adapter Configuration Space to negotiate bandwidth between a Connection Manager and the Internal USB3 Gen X Host Controller. The Connection Manager sets the *Allocated Upstream Bandwidth* and *Allocated Downstream Bandwidth* fields. The Internal USB3 Gen X Host Controller sets the *Consumed Upstream Bandwidth* and *Consumed Downstream Bandwidth* fields.

Note: All bandwidth values are USB4 Link bandwidth.

To prevent a race condition between the Connection Manager and the Internal USB3 Gen X Host Controller, the Host Router implements a locking mechanism that uses the *Connection Manager Request* and *Host Controller Ack* fields as follows:

- When the *Host Controller Ack* field = 0 (The default value):
 - The Internal USB3 Gen X Host Controller may read the *Allocated Upstream Bandwidth* and/or *Allocated Downstream Bandwidth* fields.
 - The Internal USB3 Gen X Host Controller may update the *Consumed Upstream Bandwidth* and/or *Consumed Downstream Bandwidth* fields.
 - The value in the *Consumed Upstream Bandwidth* field shall not exceed the value in the *Allocated Upstream Bandwidth* field.
 - The value in the *Consumed Downstream Bandwidth* field shall not exceed the value in the *Allocated Downstream Bandwidth* field.
- When the *Host Controller Ack* field = 1:
 - The Internal USB3 Gen X Host Controller shall not read the *Allocated Upstream Bandwidth* or *Allocated Downstream Bandwidth* fields.
 - The Internal USB3 Gen X Host Controller shall not update *Consumed Upstream Bandwidth* or *Consumed Downstream Bandwidth* fields.

A Router shall set the *Host Controller Ack* bit to 1b within t_{SetHCA} time after the *Connection Manager Request* bit is set to 1b.

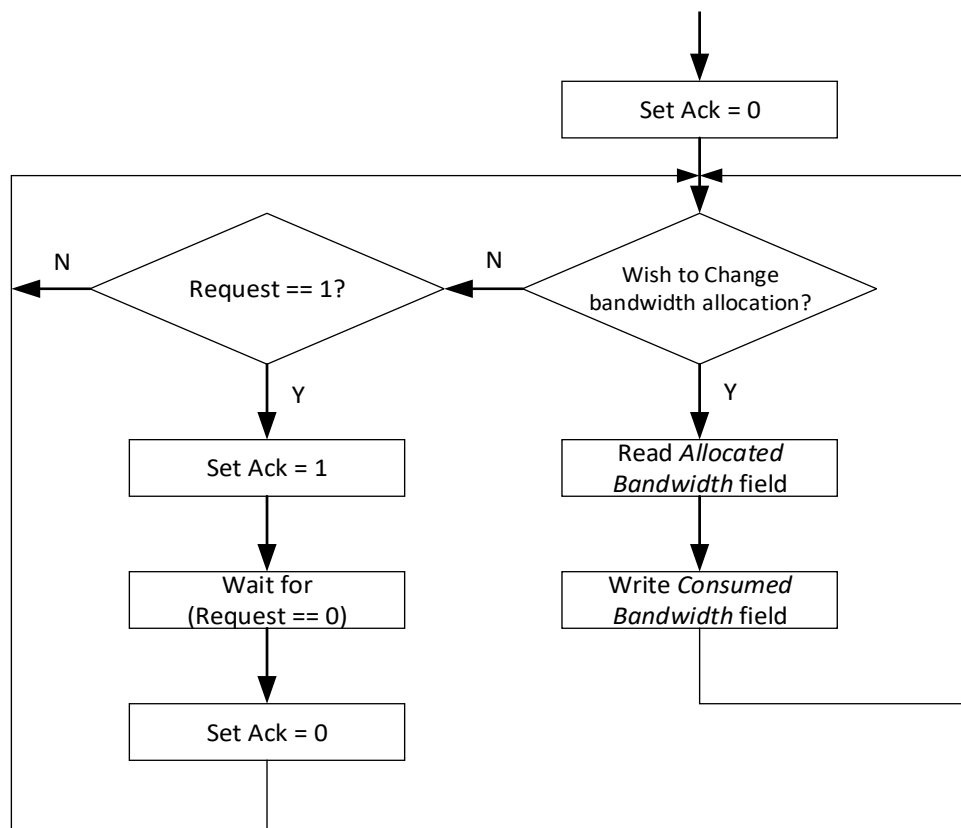
The Internal USB3 Gen X Host Controller shall negotiate bandwidth as shown in Figure 9-12.

When the USB3 link reaches U0 state, a USB3 Gen X Adapter Layer shall:

- Set the *Actual Link Rate* field to indicate the established link rate.
- Set the *USB3 Link Valid* field to 1b.

When the USB3 link is not in the U0, Recovery, U2 or U3 states, a USB3 Gen X Adapter Layer shall set the *USB3 Link Valid* field to 0b.

Figure 9-12. Bandwidth Negotiation by the Internal Host Controller



Request = Connection Manager Request bit in the USB3 Adapter Configuration Capability

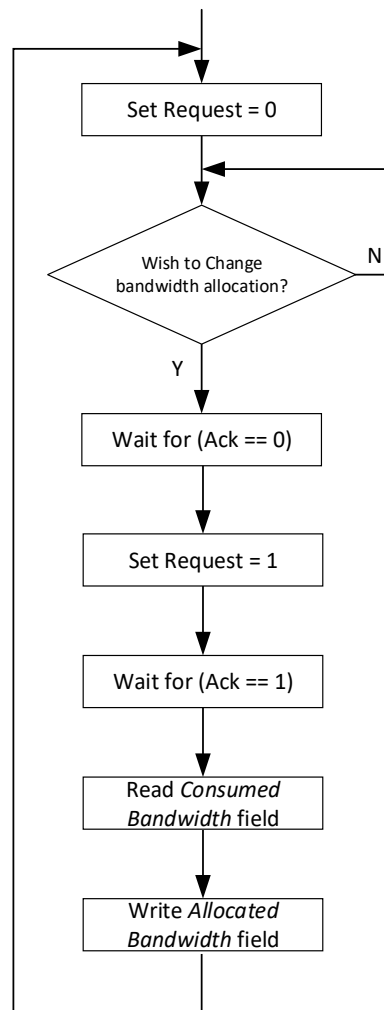
Ack = Host Controller Ack bit in the USB3 Adapter Configuration Capability

**CONNECTION MANAGER NOTE**

A Connection Manager uses the Connection Manager Request and Host Controller Ack fields as follows:

- *When the Host Controller Ack field = 0 (The default value):*
 - *The Connection Manager shall not update the Scale, the Allocated Upstream Bandwidth or Allocated Downstream Bandwidth fields.*
 - *The Connection Manager shall not read the Consumed Upstream Bandwidth or Consumed Downstream Bandwidth fields.*
- *When the Host Controller Ack field = 1:*
 - *The Connection Manager can read the Consumed Upstream Bandwidth and/or Consumed Downstream Bandwidth fields.*
 - *The Connection Manager can change the Scale, the Allocated Upstream Bandwidth and/or Allocated Downstream Bandwidth fields.*

The Connection Manager negotiates bandwidth as shown in Figure 9-13.

Figure 9-13. Bandwidth Negotiation by the Connection Manager

Request = Connection Manager Request bit in the USB3 Adapter Configuration Capability

Ack = Host Controller Ack bit in the USB3 Adapter Configuration Capability

9.1.3 Flow Control

A USB3 Adapter shall not discard a Tunneled Packet due to lack of credits in the USB4 Fabric. When insufficient credits are available, the Router shall queue the Tunneled Packet and shall transport it once sufficient credits are available.

9.1.4 PM Packet (Gen T Only)

The USB3 Gen T Adapter is allowed to send PM Packet in the following conditions:

- When a USB3 Gen T Port transitions to the U2 state, the USB3 Gen T Adapter shall send a PM Packet over the Path that corresponds to the USB3 Gen T Port. The USB3 Gen T Adapter sends one PM Packet per transition to U2. If the *U2CL2 Enable* bit is set to 1b in the Gen T Port Configuration Space, then the *CLx State* field shall be set to 11b (both CL1 and CL2 are allowed). Otherwise, the *CLx State* field shall be set to 01b.
- When a USB3 Gen T Port transitions to the U3 state, the USB3 Gen T Adapter shall send a PM Packet over the Path that corresponds to the USB3 Gen T Port. The USB3 Gen T

Adapter sends one PM Packet per transition to U3. The *CLx State* field shall be set to 11b (both CL1 and CL2 are allowed).

- When a USB3 Gen T Port transitions to the Disabled state, the USB3 Gen T Adapter shall send a PM Packet over the path that corresponds to the USB3 Gen T Port. The USB3 Gen T Adapter sends one PM Packet per transition to Disabled. The CLx State field shall be set to 11b (both CL1 and CL2 are allowed).

Note: System software may set the *U2CL2 Enable* bit to 1b in the Gen T Port Configuration Space in the following cases:

- The endpoint reports a *BELT* value greater than the *U2 exit latency plus tConvergeTime*.
- The endpoint reports a *BELT* value greater than the *U2 exit latency* and it sets the *Accurate ITP Required* bit to 0b in the Device BOS Descriptor.

9.1.5 Path Established (Gen T Only)

A USB3 Gen T Adapter shall implement a mechanism that indicates that a Path is established to the Internal USB3 Gen T Component.

When a Router is not in sleep state and is not in the process of transitioning into or out of sleep state, a USB3 Gen T Adapter Layer shall set the Path Established indicator towards the corresponding USB3 Gen T Port according to the following rules:

- Path Established = true when the *Path Enable* bit is set to 1b and *Valid* bit is set to 1b.
- Path Established = false when the *Path Enable* bit is set to 0b and *Valid* bit is set to 1b.
- Path Established retains its value when the *Valid* bit is set to 0b.

When a Router transitions to sleep state, a USB3 Gen T Adapter Layer shall maintain the same Path Established indicator value as before entry to sleep state. The USB3 Gen T Adapter Layer shall continue to maintain the indicator value until either:

- The *Valid* bit in the USB3 Gen T Adapter Configuration Capability is set to 1b after the Router exits sleep state. After the *Valid* bit is set to 1b, the USB3 Gen T Adapter Layer shall set the Path Established indicator as defined above.
- A disconnect on the paired USB4 Port occurs. If a disconnect occurs on the paired USB4 Port, the USB3 Gen T Adapter Layer may set the Path Established indicator to false.

9.1.6 Timing Parameters

Table 9-6 lists the timing parameters for a USB3 Adapter Layer.

Table 9-6. USB3 Adapter Timing Parameters

Parameter	Description	Min	Max	Units
tReassemble	Time used to determine loss of a USB3 Data Packet segment. Measured from the beginning of Start DP segment to the end of End DP segment.	100	--	μs
tSetHCA	Time from setting the <i>Connection Manager Request</i> bit to 1b until setting the <i>Host Controller Ack</i> bit to 1b.	--	100	ms

9.2 Internal USB3 Gen X Component

This section defines the functionality of the Internal USB3 Gen X Component that interfaces with a USB3 Gen X Adapter.

A USB3 Physical Layer is not needed in a USB3 Gen X Port that interfaces with a USB3 Gen X Adapter. Therefore, Physical Layer scrambling is not performed, regardless of the value of the *Disable Scrambling* bit in a received TS Ordered Set. SKIP insertion is also not performed.



IMPLEMENTATION NOTE

The Internal USB3 Component in a USB4 Device or USB4 Hub needs to preserve standard USB 3.2/USB 2.0 functionality for the cases where the USB4 Device or USB4 Hub is connected to a host port that supports only USB 3.2 functionality. As such, it follows the USB 3.2 specification requirement to fall back to USB 2.0 mode when unable to detect SuperSpeed terminations after 8 consecutive far-end receiver termination detection attempts.

For a USB4 Link, the USB3 Gen X Adapter on the USB4 Device or USB4 Hub does not expose terminations until after the USB3 tunnel is established. An implementation needs to ensure that its integrated USB3 device does not erroneously fall back to USB2 mode due to the device not detecting far-end receiver terminations after 8 attempts. This can be done through various implementation specific methods.

9.2.1 Link Layer

An Internal USB3 Component port that interfaces to a USB3 Gen X Adapter Layer shall implement a Link Layer as defined in the USB 3.2 Specification with the modifications, configurations, and parameters described in this section.

The Link Layer shall support Gen 2 Single-Lane (2x1) and may support Gen 2 Dual-Lane (2x2). No other Link capabilities shall be supported.

An Internal USB3 Component shall not send a LBPM PHY Capability with a value of 0 in bits [3:2].

Note: The USB3 LBPM handshake between the two Internal USB3 Components ports determines the link that will be established.

9.2.1.1 Link Training and Status State Machine (LTSSM)

The Link Layer shall implement a Link Training and Status State Machine (LTSSM) with the following adjustments:

- Loopback state shall not be supported.
- Compliance Mode state shall not be supported.
- U1 state shall not be supported.
 - U1 LGO shall not be sent.
- When the LTSSM of an Upstream Facing Port is in Disabled state, it shall unconditionally transition to the Rx.Detect state.
- TS1 and TS2 shall not be scrambled.

Note: The actual number of generated Ordered Sets and LFPS is not communicated between the two sides of the link.

9.2.1.2 Timers and Timeouts

Table 9-7 lists the timing parameters that have different values than those defined in the USB 3.2 Specification. An Internal USB3 Component shall use the parameter values in Table 9-7.

Table 9-7. USB3 Timers and Timeout Values

Parameter	Value
tPollingSCDLFPSTimeout	60 μ s
tPortConfiguration	40 μ s
PENDING_HP_TIMER	Min Value: 20μs, Max Value: 100μs
PM_LC_TIMER	20 μ s
PM_ENTRY_TIMER	36 μ s

**IMPLEMENTATION NOTE**

It is recommended that implementations make the values in Table 9-7 configurable.

9.2.2 USB3 Protocol Layer

The Internal USB3 Component shall implement a Protocol Layer as defined in the USB 3.2 Specification with the following adjustments:

- LDM Protocol shall not be supported over ports that interfaces a USB3 Gen X Adapter.

9.2.3 Descriptors

The Internal USB3 Component shall implement Descriptors as defined in the USB 3.2 Specification with the following adjustments:

- If a Router supports entering CL1 or CL2 when the Internal USB3 Component is in U2 state, then the value for wU2DevExitLat shall include the maximum sum of the Router enter and exit time from the supported CLx.

9.3 USB3 Gen X Paths

A USB3 Gen X Adapter Layer shall set the HopID to 8 in the header of an outgoing Tunneled Packet before handing it off to the Transport Layer for routing.

9.3.1 Path Setup**CONNECTION MANAGER NOTE**

If a Connection Manager sets up a USB3 Gen T Path to an Upstream USB3 Gen T Adapter, and the Gen X Adapter Coupled bit is set to 1b in that Adapter, then the Connection Manager shall not set up a USB3 Gen X Path to the Upstream USB3 Gen X Adapter in that Device Router. If Gen X Adapter Coupled bit is set to 0b in that Adapter, then a Connection Manager shall set a USB3 Gen X Path to the Upstream USB3 Gen X Adapter in that Device Router, regardless if a USB3 Gen T Path is set or not.

To set up USB3 Gen X Paths, a Connection Manager shall configure the USB3 Gen X Paths, then set both the Path Enable bit and the Valid bit in the USB3 Gen X Adapter Configuration Capability to 1b. A Connection Manager shall configure a USB3 Gen X Path with the Dedicated Flow Control Buffer Allocation scheme.

A Connection Manager shall configure the Output HopID to be 8 for the segment of a USB3 Gen X Path that goes from a USB4 Port to a USB3 Gen X Adapter.

When the Path Enable bit and the Valid bit in the USB3 Gen X Adapter Configuration Capability are both set to 1b, Path Setup is complete and the USB3 Gen X Adapter Layer may:

- Indicate far-end receiver termination to the Internal USB3 Component as defined in Section 9.1.1.1.2.
- Issue USB3 Tunneled Packets to the Transport Layer as defined in this chapter.



CONNECTION MANAGER NOTE

When tearing down an old USB3 Path before setting up a new USB3 Path, a Connection Manager shall wait at least 500 ms after setting the Path Enable bit to 0b before setting up the new USB3 Path. This is to allow enough time for the Internal USB3 Component port to reach the Detect state.

9.3.2 Path Teardown



CONNECTION MANAGER NOTE

Before tearing down a USB3 Gen X Path, a Connection Manager needs to disable the Path by setting the Path Enable bit in the USB3 Gen X Adapter Configuration Capability to 0b and the Valid bit in the USB3 Gen X Adapter Configuration Capability to 1b.

When a Device Router either detects a disconnect on an Upstream Facing Port, or the *Path Enable* bit in the Upstream USB3 Gen X Adapter is set to 0b and the *Valid* bit is set to 1b in the USB3 Gen X Adapter Configuration Capability:

- The Upstream USB3 Gen X Adapter Layer shall:
 - Not issue any Tunneled Packets to the Transport Layer.
 - Remove far-end receiver termination to the Internal USB3 Component as defined in Section 9.1.1.1.2.
- The Internal USB3 Component port shall detect a disconnect within 500 ms.
- The integrated Enhanced SuperSpeed Hub within the Device Router shall ensure that any SuperSpeed or Enhanced SuperSpeed devices on its downstream-facing ports transition to the default state. This can be achieved by either issuing a Warm Reset to the devices or initiating a disconnect/reconnect (either by cycling power or removing terminations).



IMPLEMENTATION NOTE

When a USB4 Device is reconnected after an Upstream Facing Port disconnect, host system software expects the integrated Enhanced SuperSpeed Hub within the USB4 Device to come up in its default state. A USB4 Device therefore needs to ensure that the integrated hub goes through a reset after the Device Router detects a disconnect on the Upstream Facing Port.



CONNECTION MANAGER NOTE

A USB device connected to a downstream port of the integrated hub may fall back to USB 2.0 operation when the hub is reset. Host system software needs to restore the original operating mode of the USB device.

When the *Path Enable* bit in a Downstream USB3 Gen X Adapter is set to 0b (including a Downstream Facing Port disconnect, see Section 4.4.5.2.1) and the *Valid* bit is set to 1b in the USB3 Gen X Adapter Configuration Capability:

- The Downstream USB3 Gen X Adapter Layer shall:
 - Not issue any Tunneled Packets to the Transport Layer.
 - Remove far-end receiver termination to the Internal USB3 Component as defined in Section 9.1.1.1.2.
- The Internal USB3 Component port shall detect a disconnect within 500 ms.



CONNECTION MANAGER NOTE

After a Router exits from sleep state, a Connection Manager may disable a USB3 Path that was enabled before sleep state entry. To disable the Path, the Connection Manager sets the Path Enable bit in the USB3 Gen X Adapter Configuration Capability to 0b and sets the Valid bit in the USB3 Gen X Adapter Configuration Capability to 1b. If the Connection Manager does not disable a Path after exit from sleep state, it shall set up the Path again as if it is a new Path.

9.4 Internal USB3 Gen T Component

This section defines the functionality of the Internal USB3 Gen T Component that interfaces with a USB3 Gen T Adapter. An Internal USB3 Gen T Component shall operate according to the rules for SuperSpeedPlus operation as defined in the USB 3.2 Specification with the modifications defined in this section.

9.4.1 Link Layer

9.4.1.1 USB Gen T Packet Framing

An Internal USB3 Gen T Component only uses a few of the framing symbols defined in the USB 3.2 Specification. This is to better utilize the underlying features of the USB4 Link and optimize usage of the available bandwidth.

An Internal USB3 Gen T Component shall not use DPHP, SDP, SHP, SLC and these framing symbols are deprecated. EPF along with END and EDB shall still be used to indicate whether a DPP is good (END) or bad (EDB). This is to allow the USB3 link or USB3 Gen T Adapter to indicate a void data packet if it runs into an error condition while transmitting the DPP.

The length field replica in a DPHP shall not be transmitted in a USB3 Gen T Tunneled Packet.

9.4.1.2 Link Command Word Definition

The Link Command Word shall be 16 bits long and shall have the format shown in Table 9-8.

Table 9-8. Link Command Word Format

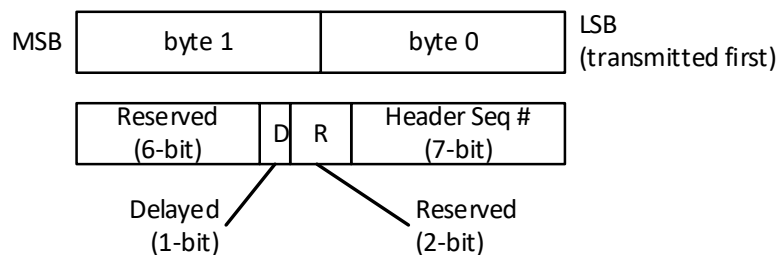
Name	Link Command Format ¹															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
LGOOD_n	R	0	0	0	0	0	R	R	R	n: 0...127						
LCRD1_x	R	0	0	0	1	0	R	R	R	R	x: 1...63					
LCRD2_y	R	0	0	0	1	1	R	R	R	R	y: 1...63					
LGO_U2	R	0	1	0	0	0	R	R	R	R	R	R	0	0	1	0
LGO_U3	R	0	1	0	0	0	R	R	R	R	R	R	0	0	1	1
LAU	R	0	1	0	1	0	R	R	R	R	R	R	R	R	R	R
LXU	R	0	1	1	0	0	R	R	R	R	R	R	R	R	R	R
LPMA	R	0	1	1	1	0	R	R	R	R	R	R	R	R	R	R
LKAI_n	R	1	0	0	0	0	R	R	0	0	R	R	n: 0...15			
LKAR	R	1	0	0	0	0	R	R	0	1	R	R	R	R	R	R

Name	Link Command Format ¹															
LKAN	R	1	0	0	0	0	R	R	1	0	R	R	R	R	R	R
NOP	R	1	1	1	1	1	R	R	R	R	R	R	R	R	R	R
1. Bits marked as 'R' are Reserved.																

9.4.1.3 Link Control Word

The Link Control Word shall have the format shown in Figure 9-14.

Figure 9-14. USB3 Gen T Link Control Word



As shown in Figure 9-14, the Link Control Word contains a 7-bit Header Sequence Number, 2-bit Reserved, a Delayed bit (DL), and the final 6-bits Reserved.

9.4.1.4 Link Credits and Burst Size

Table 9-9 lists the number of Link Credits and the Max Burst Size for each speed supported by the USB 3.2 Specification as well as for USB3 Gen T operation.

Table 9-9. Link Credits and Maximum Burst Size

Gen	Number of Link Credits	Max Burst Size
Gen 1x1 (Gen X)	4	16
Gen 1x2 (Gen X)	Type 1: 4, Type 2: 4	16
Gen 2x1 (Gen X)	Type 1: 4, Type 2: 4	16
Gen 2x2 (Gen X)	Type 1: 7, Type 2: 7	16
Tunnel – Gen 2x1 (Gen X)	Type 1: 4, Type 2: 4	16
Tunnel – Gen 2x2 (Gen X)	Type 1: 7, Type 2: 7	16
USB3 Gen T	Type 1: 63, Type 2: 63	64

9.4.1.5 Link Command Aggregation and Coalescing

An Internal USB3 Gen T Component shall support Link Command Aggregation and Coalescing. Once the link is in LTSSM.U0, the Internal USB3 Gen T Component shall turn on Link Command Aggregation if the *Link Commands Aggregation Enable* bit is set to 1b in the USB3 Gen T Adapter Configuration Space.

Note: Link Commands Aggregation permits sending LCRD1_x, LCRD2_y, and LGOOD_n with the most recent index (i.e. skipping over indexes) regardless of the value of the Link Commands Aggregation Enable bit. The value of tLC_AggrThreshold is defined for keeping the Link Command maximal rate as one for every 4KB of transferred user payload. While the Link Commands Aggregation Enable bit is set to 0b, the rules below for Link Command Aggregation and Coalescing still apply, except that the Internal USB3 Gen T Component does not need to maintain tLC_AggrThreshold intervals between Coalesced Link Command Packets.

An Internal USB3 Gen T Component shall send a Link Command (if it has one to send) without waiting for *tLC_AggrThreshold* upon any of the following:

- Entry into LTSSM.U0.
- After a *tLC_AggrThreshold* time interval passes without any Link Commands.
- If the Link Command is not an LGOOD_n, LCRD1_x, or LCRD2_y.
- If the *Link Commands Aggregation Enable* bit is cleared.
- All subsequent Link Commands shall be sent (if such are needed) at *tLC_AggrThreshold* intervals except as listed above while the USB3 Gen T LTSSM is in U0. The transmission of a Link Command may be delayed in the following cases:
 - The USB3 Gen T Port is in the process of transmitting a USB3 Data Packet
 - The USB4 Path associated with the USB3 Gen T Port is blocked by insufficient USB4 credits
 - The USB4 Path associated with the USB3 Gen T Port is blocked by USB4 packets being transmitted on a different USB4 path on the USB4 link.

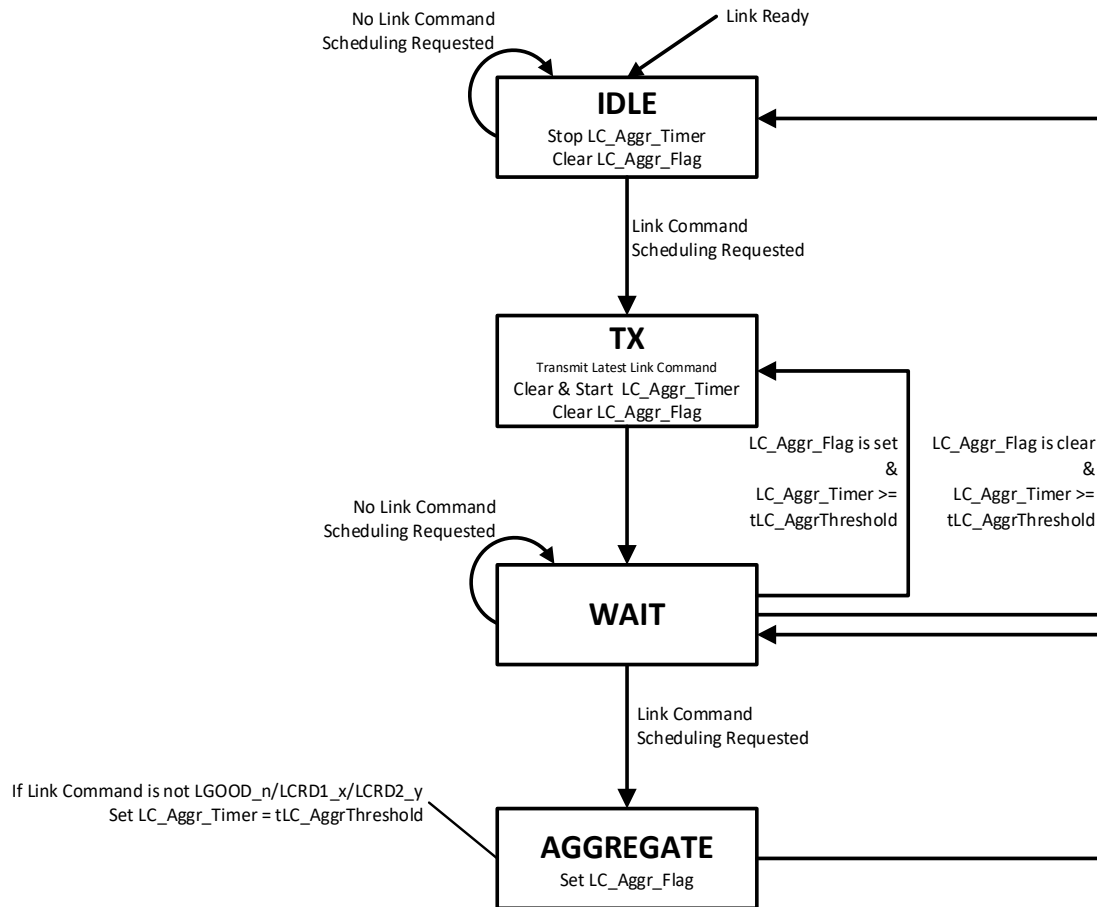
The Internal USB3 Gen T Component shall send the last LGOOD_n/LCRD1_x/LCRD2_y Link Commands as per the Header Packets received during the *tLC_AggrThreshold* period, then update the Rx Header Sequence Number and Rx Buffer Credit indexes accordingly. For example, if an Internal USB3 Gen T Component successfully received two Header Packets during the *tLC_AggrThreshold* period, the Internal USB3 Gen T Component sends the LGOOD_n corresponding to the second Header Packet it received. In addition, if the Internal USB3 Gen T Component frees up any Header Buffers, it shall send the LCRD1_x/LCRD2_y corresponding to the last Header Buffer that was freed.



IMPLEMENTATION NOTE

A Gen T Port needs to avoid transmitting LCRD1_x or LCRD2_y after freeing a packet buffer before an LGOOD_n is transmitted for the corresponding packet to which the LCRD1_x/LCRD2_y is associated.

Figure 9-15 shows an example of an implementation of the Link Command Aggregation state machine.

Figure 9-15. Example Link Command Aggregation State Machine (Informative)

In addition to Link Command Aggregation, an Internal USB3 Gen T Component shall perform Link Command Coalescing. An Internal USB3 Gen T Component may coalesce up to four Link Commands. A Coalesced Link Command Packet shall contain either two or four Link Commands. The ordering rules of the Link Commands within a Coalesced Link Command Packet are detailed below.

- A Gen T Port shall send 2 DWs if both LCRD1_x and LCRD2_y are present, or if there is a Link Command which is not LGOOD_n/LCRD1_x/LCRD2_y, otherwise it shall send a single DW.
- First word (Word0 in DW0): If LGOOD_n is present then LGOOD_n, else NOP.
- Second word (Word1 in DW0): If LCRD1_x is present then LCRD1_x, else if LCRD2_y is present then LCRD2_y, else NOP.
- Third word (Word0 in DW1): If LCRD2_y is present and was not included in the second word then LCRD2_y, else NOP.
- Fourth word (Word1 in DW1): If any other Link Command present then that Link Command, else NOP.

Table 9-10 shows examples of the order and location of individual Link Commands within a Coalesced Link Command Packet.

Table 9-10. Example Link Command Coalescing

Link Commands	DW0[Word 0]	DW0[Word 1]	DW1[Word 0]	DW1[Word 1]
LGOOD_n, LCRD2_y	LGOOD_n	LCRD2_y	NA	NA
LGOOD_n, LCRD1_x, LCRD2_y	LGOOD_n	LCRD1_x	LCRD2_y	NOP
LGOOD_n, LCRD2_y, LGO_UX	LGOOD_n	LCRD2_y	NOP	LGO_UX
LCRD1_x, LCRD2_y	NOP	LCRD1_x	LCRD2_y	NOP
LPMA	NOP	NOP	NOP	LPMA
LCRD2_y	NOP	LCRD2_y	NA	NA
LCRD1_x, LKAI_n	NOP	LCRD1_x	NOP	LKAI_n
LGOOD_n, LKAR	LGOOD_n	NOP	NOP	LKAR
LKAN	NOP	NOP	NOP	LKAN

9.4.1.5.1 Link Keep-Alive

The Link Keep-Alive mechanism provides the means for a Gen T downstream port to infer a Gen T upstream port disconnect within a shorter time. When Link Keep-Alive is enabled, a Gen T upstream port transmits dedicated Link Commands periodically while it is idle. When a Gen T downstream port does not receive packets on an Ingress Paths within the expected duration, it can conclude that a remote upstream Gen T port has disconnected.

Software determines whether Link Keep-Alive for Gen T downstream ports is supported. The means by which software determines whether or not Link Keep-Alive for a Gen T downstream port is supported and enabled/disabled, is outside the scope of this specification.

A Gen T upstream Port shall support Link Keep-Alive. A Gen T downstream port may optionally support Link Keep-Alive.

The LKAI_n (Link Keep-Alive Interval) Link Command is transmitted by a Gen T downstream port to communicate Link Keep-Alive time intervals to a remote Gen T upstream port. The LKAI Link Command is transmitted using a Coalesced Link Command. A LKAI_0 Link Command is used to disable Link Keep-Alive. Other LKAI_n Link Commands are used to enable Link Keep-Alive. The value of 'n' (bits 3:0 in the LKAI_n Link Command Word) describes the following time intervals:

- The Link Keep-Alive Idle interval is defined as $[n * 2\mu s]$.
- The definition of the Link Keep-Alive Wait interval is implementation-specific. However, it is recommended that Link Keep-Alive Wait interval be defined as at least $[(n+2) * 2\mu s]$.
- For example, a LKAI_15 Link Command defines a Link Keep-Alive Idle interval of 30 microseconds, and a Link Keep-Alive Wait interval of 34 microseconds.

The LKAR (Link Keep-Alive Response) Link Command is transmitted by a Gen T upstream port to acknowledge the modification of Link Keep-Alive configuration.

The LKAN (Link Keep-Alive Notification) Link Command is transmitted by a Gen T upstream port to interrupt Link Keep-Alive Idle intervals as described below.

After software enables Link Keep-Alive for a Gen T downstream port:

- The Gen T downstream port shall send a single LKAI_n Link Command (other than LKAI_0) reflecting the updated Link Keep-Alive Wait interval configuration in the following cases:
 - The port is in the LTSSM.U0 state when directed by the software.

- Upon transitioning to LTSSM.U0, if the port was not in LTSSM.U0 when directed by the software.
- After transmitting the LKAI_n Link Command:
 - If an LKAR Link Command is not received within tUSB3KeepAliveTimeout, the port may transition to LTSSM.ERROR state.
 - Otherwise, enable Link Keep-Alive with the corresponding Link Keep-Alive Wait interval for the port after receiving LKAR Link Command.
- While Link Keep-Alive is enabled, the downstream port may transition from LTSSM.U0 state to LTSSM.ERROR state if it does not receive any USB3 Gen T Tunneled Packets for that port within the Link Keep-Alive Wait interval.

Link Keep-Alive for a Gen T downstream port is disabled in the following cases:

- When directed by software.
- The Gen T downstream port transmits a single LKAI_0 Link Command when the port is in LTSSM.U0 state and receives LKAR Link Command from the Gen T upstream port.
- When the port exits LTSSM.U0 state.
- After POR.

When Link Keep-Alive is disabled, a Gen T downstream port shall not transmit LKAI_n Link Commands until directed to do so by software. Software shall guarantee that at least tUSB3KeepAliveUpdate time elapses between a Gen T downstream port sending two LKAI_n Link Commands with different LKAI_n encodings.

When Link Keep-Alive is disabled as a result of exiting from LTSSM.U0 state:

- If the transition was from LTSSM.U0 to LTSSM.U2 or LTSSM.U3 state, then upon exiting LTSSM.U2 or LTSSM.U3 and re-entering LTSSM.U0 state, the Gen T downstream port shall re-enable Link Keep-Alive according to the existing LKA software settings without requiring any action by the software.
- Else, if the transition was from LTSSM.U0 to a state other than LTSSM.U2 or LTSSM.U3, a Gen T downstream port shall not transmit LKAI_n Link Commands until directed to do so by the software.

When a Gen T upstream port that supports Link Keep-Alive receives an LKAI_n Link Command:

- The Gen T upstream port shall respond with a single LKAR Link Command within tUSB3KeepAliveResponse when the port is in LTSSM.U0.
- If the received Link Command is not an LKAI_0, the Gen T upstream port shall enable Link Keep-Alive using the Link Keep-Alive Idle interval corresponding to the received LKAI_n Link Command.
- When Link Keep-Alive is enabled:
 - While the port is in LTSSM.U0 state, the Gen T upstream port shall send a LKAN Link Command if it has not transmitted any other USB3 Gen T Tunneled Packets while in idle state within the Link Keep-Alive Idle interval.
 - The Gen T upstream port may not transmit a LKAN Link Command if a USB3 Gen T Tunneled Packet is transmitted before the Link Keep-Alive Idle interval elapses.

A Gen T upstream port shall disable Link Keep-Alive as follows:

- When the port is not in LTSSM.U0 state, the port shall not retain the Link Keep-Alive Idle interval on transition from LTSSM.U0 to any other state.
- After receiving an LKAI_0 Link Command.

A Gen T upstream port shall not send LKAR or LKAN Link Commands when Link Keep-Alive is disabled.

Note that all of the above requirements in LTSSM.U0 state also apply during the LGO_U2 and LGO_U3 entry sequences. However, an LKAI_n Link Command is not transmitted after sending an LAU or LPMA Link Command.

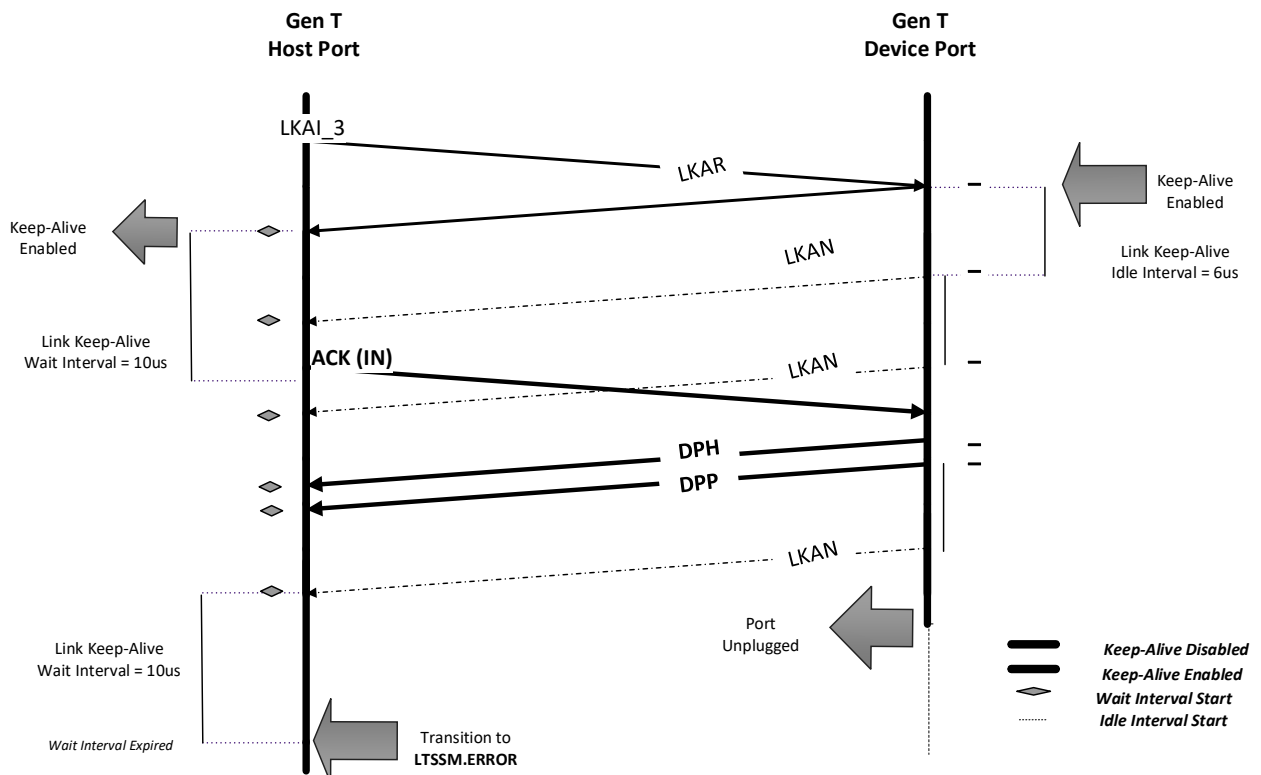


IMPLEMENTATION NOTE

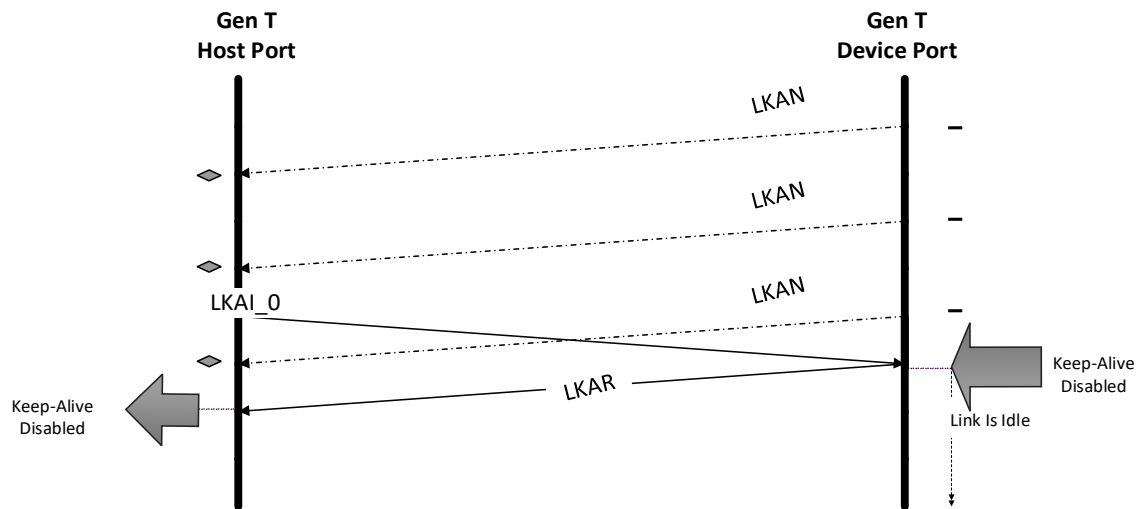
Although Link Keep-Alive is disabled when the port is not in LTSSM.U0 state, a Gen T downstream port may retain the last Link Keep-Alive software configuration while it is in the DSPORT.Enabled state. Therefore, after software configures Link Keep-Alive, the Gen T downstream port does not require any additional software configuration to send the previous LKAI_n value when transitioning to LTSSM.U0 state from LTSSM.U3 or LTSSM.U2 states.

Example 1: Figure 9-16 illustrates Link Keep-Alive being enabled in LTSSM.U0 state, followed by an upstream port disconnect. The upstream port disconnect causes a Link Keep-Alive Wait interval timeout, which then causes the downstream port to transition to LTSSM.ERROR state.

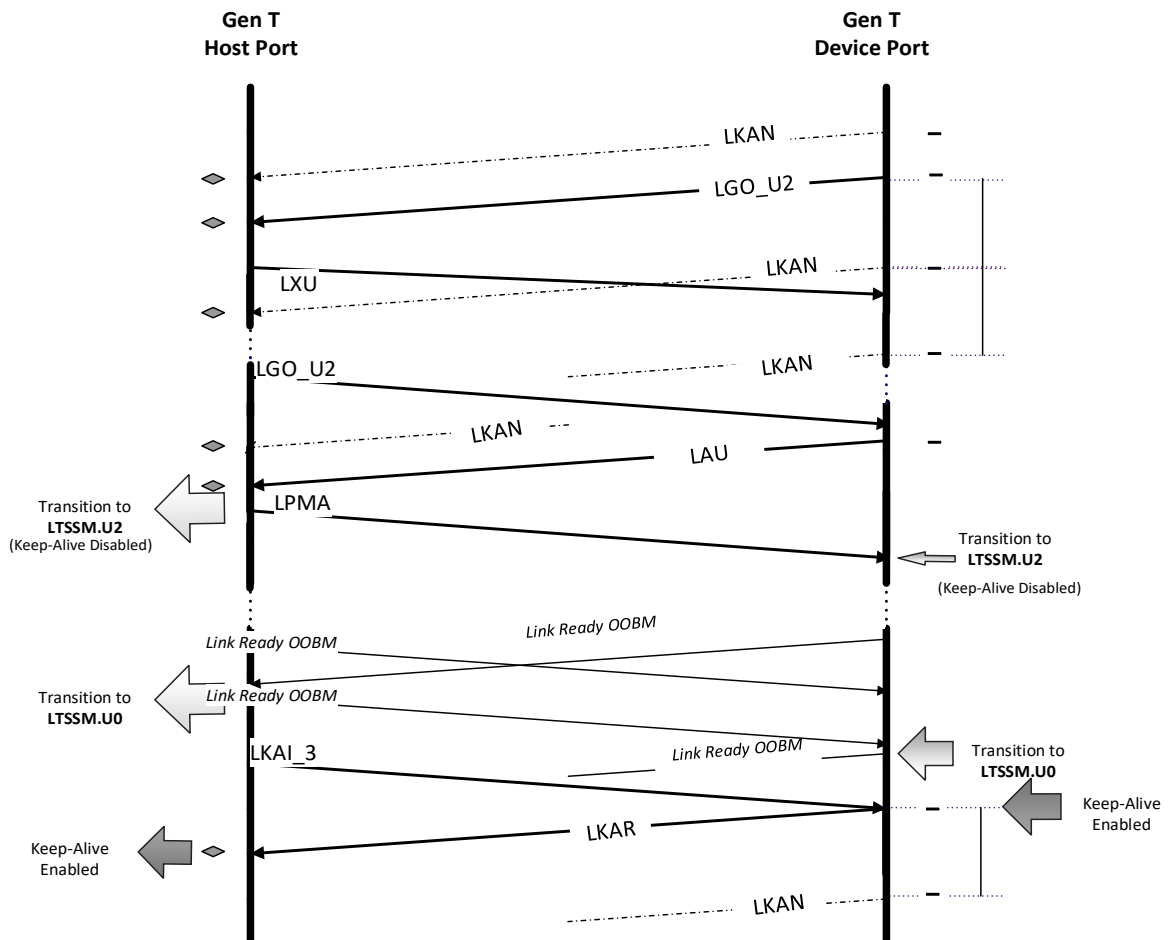
Figure 9-16. Link Keep-Alive Flow (Example 1)



Example 2: Figure 9-17 illustrates Link Keep-Alive being disabled in LTSSM.U0 state, after which the downstream port stops monitoring for an upstream presence.

Figure 9-17. Link Keep-Alive Flow (Example 2)

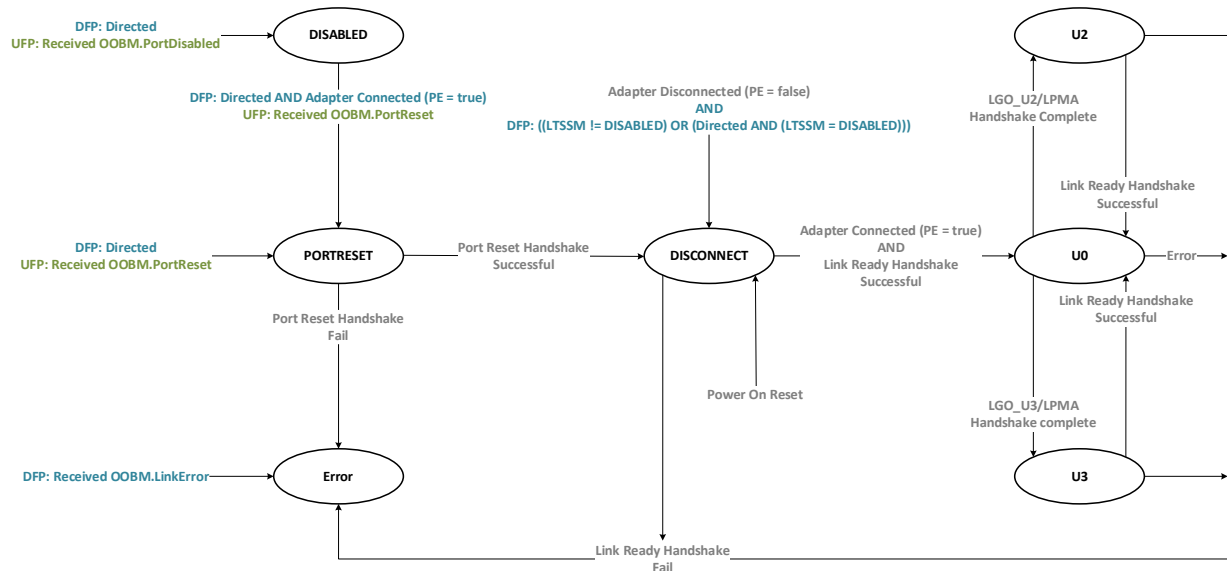
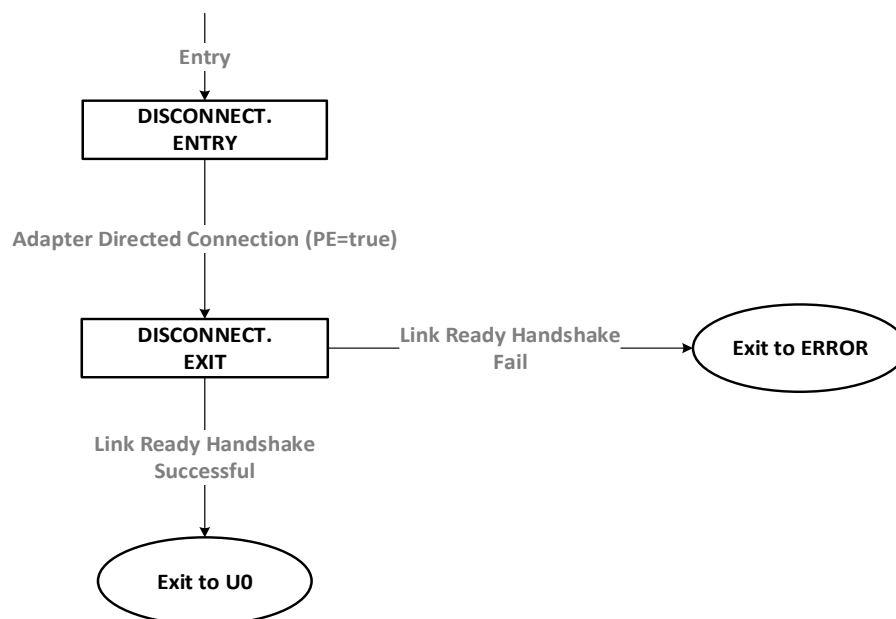
Example 3: Figure 9-18 illustrates Link Keep-Alive being disabled then enabled during unsuccessful and then successful LTSSM.U2 entry. The example shows an LTSSM.U2 exit sequence to LTSSM.U0, which reenables Link Keep-Alive in the downstream port.

Figure 9-18. Link Keep-Alive Flow (Example 3)

9.4.1.6 Link Training and Status State Machine (LTSSM)

The Link Training and Status State Machine (LTSSM) is a state machine defined for link connectivity and link power management. The LTSSM for a USB3 Gen T Port is a simplified version of the LTSSM defined in the USB 3.2 Specification.

A USB3 Gen T Port shall support the LTSSM shown in Figure 9-19.

Figure 9-19. USB3 Gen T LTSSM**9.4.1.6.1 LTSSM.DISCONNECT****Figure 9-20. Example DISCONNECT Substate Machine**

This is the default state of a USB3 Gen T Port after Power On Reset (POR). A USB3 Gen T Port shall remain in this state until the USB3 Gen T Adapter indicates that Path Established is true. When Path Established is true, the USB3 Gen T Port shall send an *OOBM.LinkReady* message to

the link partner and start the *tOOBMPolling* timer. Once the Link Ready handshake is successful, the LTSSM shall move to U0 state.

The LTSSM shall transition to the DISCONNECT state upon any of the following conditions:

- After POR.
- For a USB3 Gen T downstream port, from the LTSSM.DISABLED state when directed to enable the port and Path Established is false.
- For a USB3 Gen T downstream port (from any state other than DISABLED) or a USB3 Gen T upstream port, when Path Established is false in the corresponding USB3 Gen T Adapter.

9.4.1.6.2 LTSSM.U0

A USB3 Gen T Port shall enter the LTSSM.U0 state as follows:

- From the LTSSM.DISCONNECT state:
 - When Path Established is true and a Link Ready handshake is successful.
- From the LTSSM.U2 and LTSSM.U3 states:
 - After a Link Ready handshake is successful.

A USB3 Gen T Port initiates a Link Ready Handshake by sending an OOBM.*LinkReady* message to the link partner. The USB3 Gen T Port shall continue to send OOBM.*LinkReady* messages at *tOOBMPolling* intervals until it receives an OOBM.*LinkReady* from the link partner. After receiving at least one OOBM.*LinkReady* from the link partner, a USB3 Gen T Port shall enter LTSSM.U0. The USB3 Gen T Port shall send one last OOBM.*LinkReady* as the first packet after entry into LTSSM.U0. The last OOBM.*LinkReady* shall be sent no later than *tOOBMPolling* Max time after entering LTSSM.U0.

Note: A USB3 Gen T Port shall ignore all OOBM.LinkReady messages when it is in LTSSM.U0.

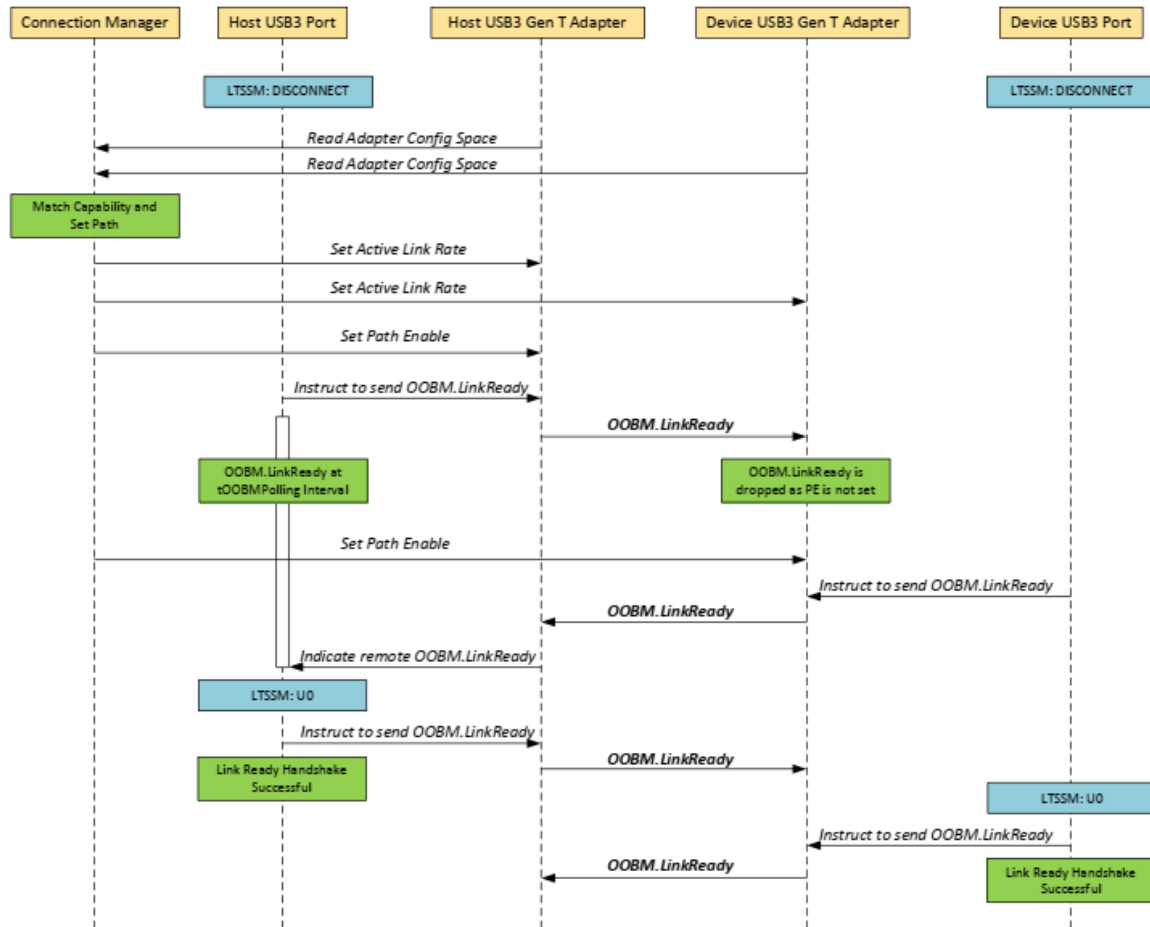
After the Link Ready Handshake completes, a USB3 Gen T Port shall transition into the U0 state and it shall:

- Set the Type 1 and Type 2 Rx Header Buffer Credit Count to 63.
- Set the Header Sequence Number to zero.
- Set the Rx Header Buffer Credit Number to 1.

The USB3 Gen T Port shall not advertise the starting Header Sequence Number and shall not advertise the Rx Header Buffer Credit Number.

Note that when a USB3 Gen T Port enters LTSSM.U0 from LTSSM.PORTRESET or LTSSM.DISABLED, it shall transition through LTSSM.DISCONNECT.

An example flow of the LTSSM transitioning from LTSSM.DISCONNECT to LTSSM.U0 is shown in Figure 9-21.

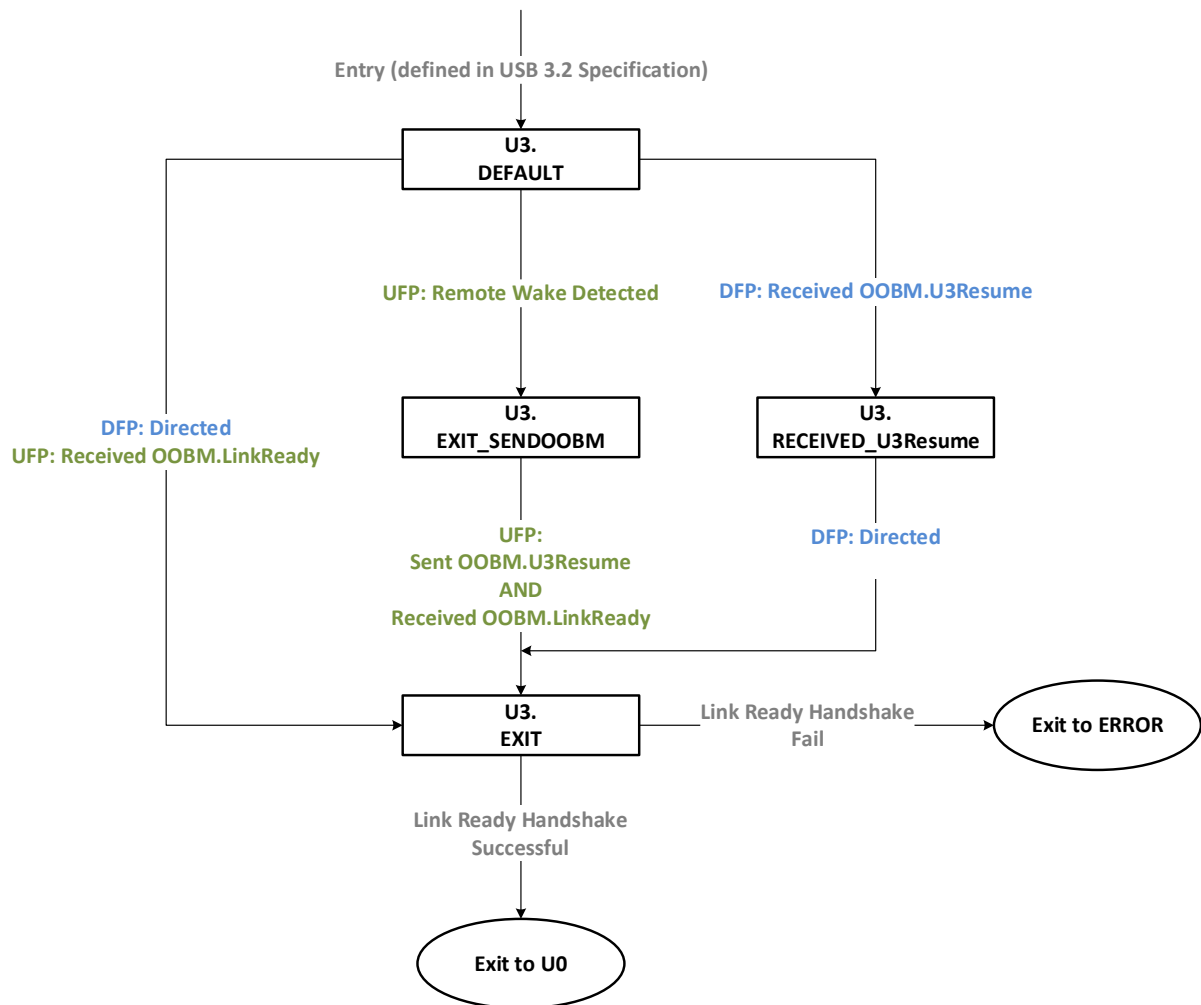
Figure 9-21. USB3 Gen T Link Ready Handshake Sequence

A USB3 Gen T Port shall complete the Link Ready Handshake within $tPortReadyTimeout$.

If an error occurs while in LTSSM.U0 the USB3 Gen T Port shall transition to the LTSSM.ERROR state. A USB3 Gen T Port shall not support the LRTY Link command and shall not implement any header retry mechanism.

9.4.1.6.3 LTSSM.U3

Figure 9-22. Example U3 Substate Machine



A USB3 Gen T Port shall enter the LTSSM.U3 state as defined in the USB 3.2 Specification. A USB3 Gen T Port in LTSSM.U3 shall not transmit any packets and it shall not accept any packets.

Exit from LTSSM.U3 may be initiated by a Remote Wake capable device or by the Host. A Remote Wake capable Internal USB3 Gen T Component shall request a wake by sending an `OOBM.U3Resume` message while staying in U3. It shall send `OOBM.U3Resume` at `tOOBMPolling` intervals until it receives an `OOBM.LinkReady` from the Host. Once it receives the `OOBM.LinkReady`, it shall complete the Link Ready handshake as described in Section 9.4.1.6.2.

Note: There is no timing requirement on when a Host sends the `OOBM.LinkReady` as it is dependent on software.

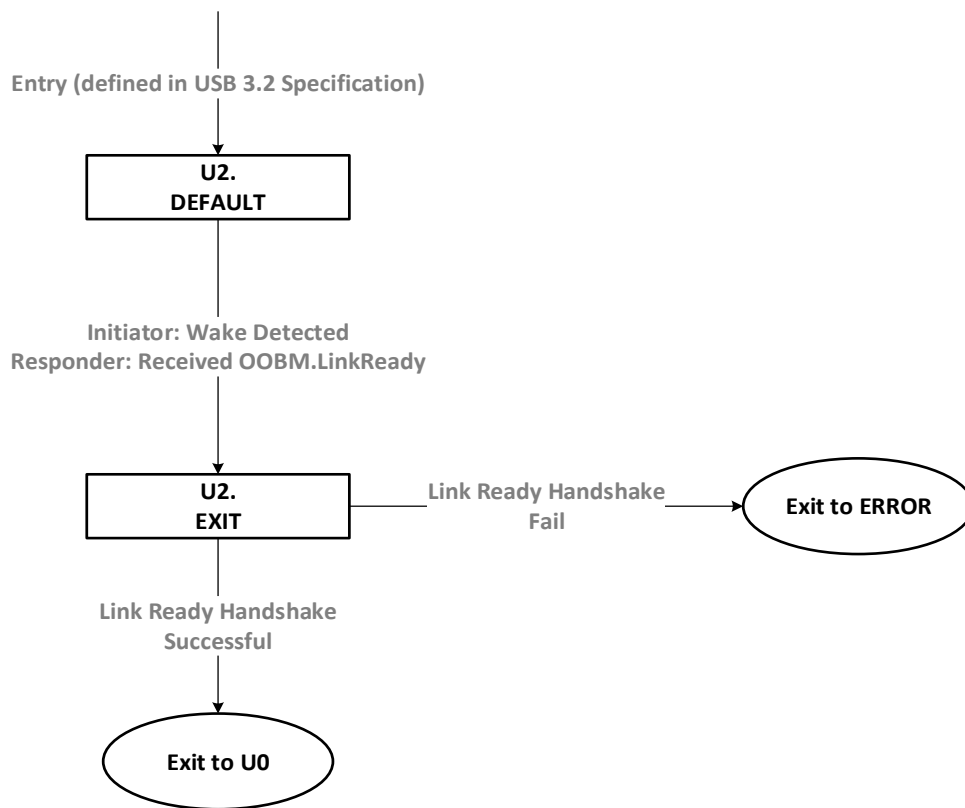
A Host-initiated LTSSM.U3 exit is directed by system software. When directed to do so by system software, a USB3 Gen T downstream port shall initiate the LTSSM.U3 exit by initiating a Link Ready handshake as described in Section 9.4.1.6.2.

If an error occurs while in LTSSM.U3 (expired `tPortReadyTimeout`), the USB3 Gen T Port shall transition to the LTSSM.ERROR state.

When a USB3 Gen T Port is in LTSSM.U3, the USB4 Link may transition to the CLx state as described in Section 4.2.1.6.

9.4.1.6.4 LTSSM.U2

Figure 9-23. Example U2 Substate Machine



A USB3 Gen T Port shall enter the LTSSM.U2 state as defined in the USB 3.2 Specification. A USB3 Gen T Port in LTSSM.U2 shall not transmit any packets and it shall not accept any packets.

If the Internal USB3 Gen T Component has data to transfer, it shall wake up the USB3 Gen T Component that it is connected to by initiating a Link Ready handshake with its link partner as described in Section 9.4.1.6.2.

If an error occurs while in LTSSM.U2 (expired *tPortReadyTimeout*), the USB3 Gen T Port shall transition to the LTSSM.ERROR state.

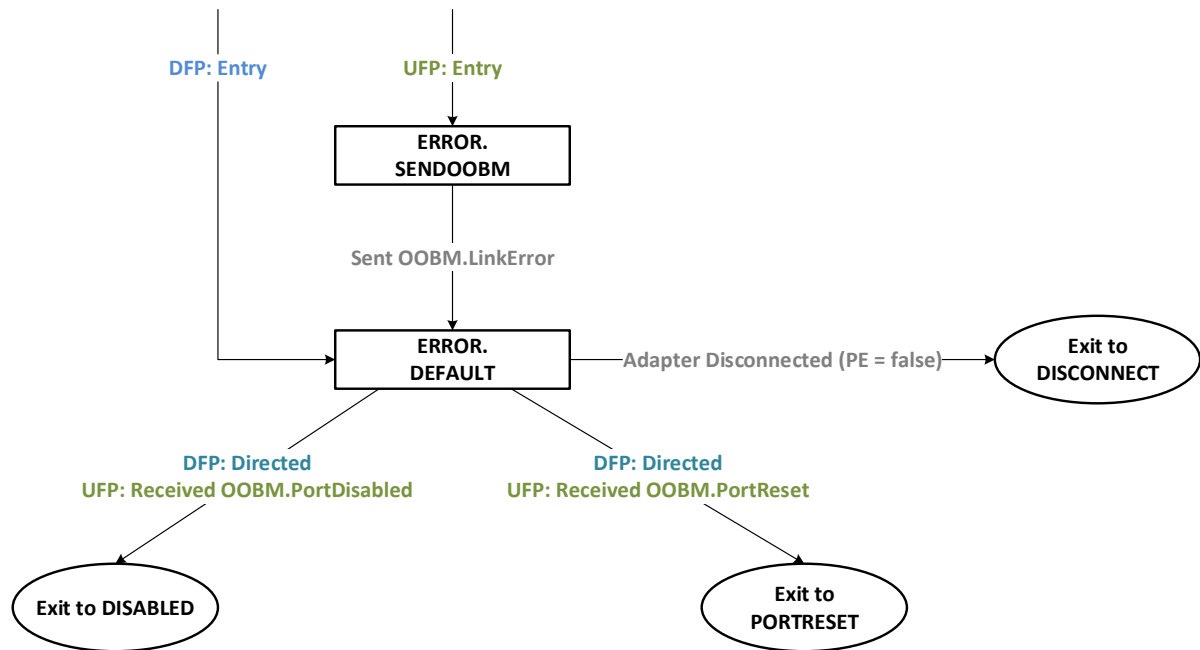
When a USB3 Gen T Port is in LTSSM.U2, the USB4 Link may transition to the CL1/CL2 state as described in Section 4.2.1.6.

The U2 Inactivity Timer shall reset when any of the following occur:

- Software changes the value of the U2 Inactivity Timer
- Any OOBM is transmitted or received.
- Any USB3 Tunneled Packet is received (excluding Link Commands other than LXU).
- Any USB3 Tunneled Packet is transmitted (excluding ITP).

9.4.1.6.5 LTSSM.ERROR

Figure 9-24. Example ERROR Substate Machine



A USB3 Gen T upstream port shall send one *OOBM.LinkError* to the USB3 Gen T downstream port upon entering the LTSSM.ERROR state. The USB3 Gen T Port shall not transmit any additional packets. After the USB3 Gen T Port enters the LTSSM.ERROR state, it shall discard any USB3 Tunneled Packets and shall continue to receive and process OOBMs.

A USB3 Gen T downstream port shall indicate that it is in the LTSSM.ERROR state to system software in order for it to take appropriate action.

A USB3 Gen T downstream port exits from the LTSSM.ERROR state in one of the following ways:

- To the LTSSM.PORTRESET state, if directed to do so by system software.
- To the LTSSM.DISABLED state, if directed to do so by system software.
- To the LTSSM.DISCONNECT state, if Path Established is false.

A USB3 Gen T upstream port exits from the LTSSM.ERROR state in one of the following ways:

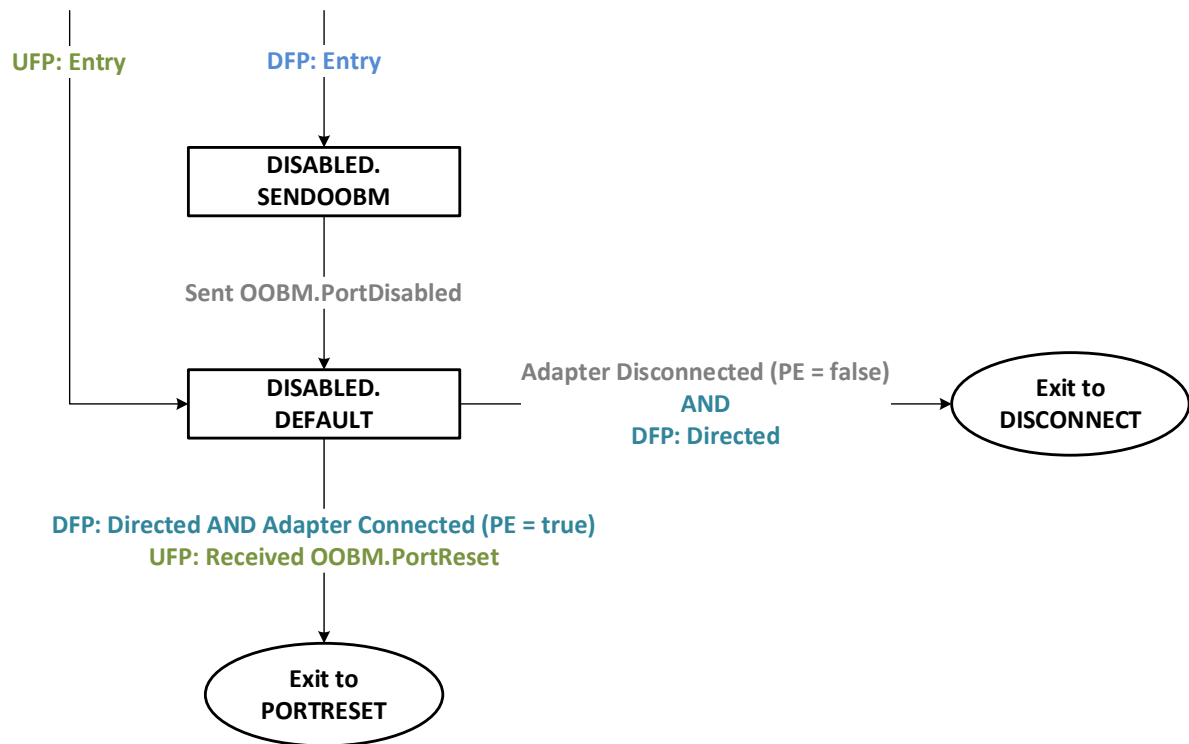
- To the LTSSM.PORTRESET state, upon reception of *OOBM.PortReset*.
- To the LTSSM.DISABLED state, upon reception of *OOBM.PortDisabled*.
- To the LTSSM.DISCONNECT state, if Path Established is false.

A USB3 Gen T Port shall enter the LTSSM.ERROR state by the errors listed in Section 9.4.1.6.8, which leads to transitioning to the LTSSM.ERROR state.

A USB3 Gen T downstream port in LTSSM.U0 state shall enter LTSSM.ERROR state on reception of *OOBM.LinkError*. When Link Keep-Alive is enabled, a Gen T downstream port in LTSSM.U0 state may enter LTSSM.ERROR as described in Section 9.4.1.5.1.

9.4.1.6.6 LTSSM.DISABLED

Figure 9-25. Example DISABLED Substate Machine



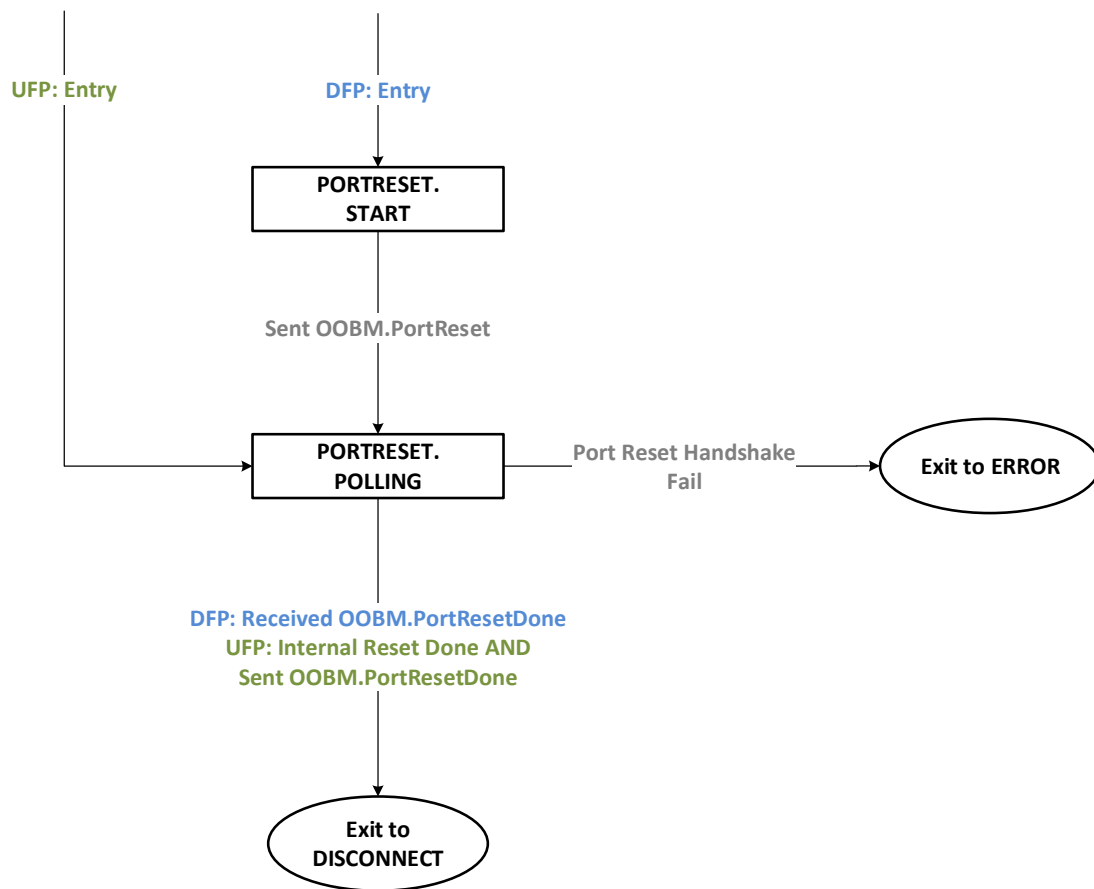
A USB3 Gen T downstream port shall send one *OOBM.PortDisabled* upon entering the LTSSM.DISABLED state if Path Established is true. The USB3 Gen T Port shall not transmit any additional packets and it shall not accept any packets from its link partner while in the LTSSM.DISABLED state.

A USB3 Gen T downstream port shall transition to the LTSSM.DISABLED state when directed to do so by system software. A USB3 Gen T upstream port shall transition to the LTSSM.DISABLED state upon reception of an *OOBM.PortDisabled*.

A USB3 Gen T downstream port shall exit from the LTSSM.DISABLED state when directed to do so by system software. A USB3 Gen T upstream port shall exit from the LTSSM.DISABLED state either upon receiving an *OOBM.PortReset* or when Path Established is false.

9.4.1.6.7 LTSSM.PORTRESET

Figure 9-26. Example PORTRESET Substate Machine



A USB3 Gen T downstream port shall enter the LTSSM.PORTRESET state as directed by system software.

When performing a Port Reset, the USB3 Gen T downstream port shall do the following:

1. Upon entering this state, send an *OOBM.PortReset* message to the link partner and start the *tOOBMPolling* timer. The USB3 Gen T downstream port shall send an *OOBM.PortReset* at *tOOBMPolling* intervals.
2. Wait for an *OOBM.PortResetDone* from the link partner.
3. Transition to the LTSSM.DISCONNECT state.

When a USB3 Gen T upstream port receives an *OOBM.PortReset*, it shall:

1. Complete its internal reset flow.
2. Respond back with an *OOBM.PortResetDone*.
3. Transition to the LTSSM.DISCONNECT state.

If the Port Reset handshake fails to complete within *tPortReadyTimeout* time, the USB3 Gen T Port shall transition to the LTSSM.ERROR state.

**IMPLEMENTATION NOTE**

A USB3 Gen T upstream port may ignore the first received OOBM.*PortReset* after sending a OOBM.*PortResetDone*.

9.4.1.6.8 Error Checking

An Internal USB3 Gen T Component shall process errors using the error checking mechanism and flow defined in the USB 3.2 Specification. However, there shall be no recovery for errors in Link Command transactions. Upon detecting an error or a timeout, the USB3 Gen T Port shall transition to the LTSSM.ERROR state as mentioned in Table 9-11.

Table 9-11 lists the various types of errors and how each error is detected and handled.

Table 9-11. Error Detection and Handling

Error	Example	Action Taken by the Detecting USB3 Gen T Port	Detecting the Error by the Link Partner
Link Ready handshake failure	Link Ready timeout (tPortReadyTimeout)	Transition to LTSSM.ERROR state	Subsequent Link Ready handshake completion timeout (tPortReadyTimeout)
Port Reset handshake failure	Port Reset timeout (tPortReadyTimeout)	Transition to LTSSM.ERROR state	Subsequent Link Ready handshake completion timeout (tPortReadyTimeout)
Inferred UFP Disconnect (DFP only)	Host did not detect LKAN within the Wait Interval while in U0 state	Optional transition to LTSSM.ERROR state	UFP: Subsequent transaction results in PENDING_HP_TIMER or CREDIT_HP_TIMER or PM_LC_TIMER Timeout
UFP Error Message (DFP only)	Reception of OOBM. <i>LinkError</i>	Transition to LTSSM.ERROR state	None (UFP already in LTSSM.Error State)
PENDING_HP_TIMER Timeout	LGOOD_n not received upon PENDING_HP_TIMER timeout	Transition to LTSSM.ERROR state	UFP: Subsequent transaction results in PENDING_HP_TIMER or CREDIT_HP_TIMER or PM_LC_TIMER Timeout DFP: Reception of OOBM. <i>LinkError</i>
Rx Header Sequence Number Error	The Header Sequence Number in the received header packet exceeds the expected Rx Header Sequence Number, or Rx Header Buffer is not available to store the packet	Transition to LTSSM.ERROR state	UFP: Subsequent transaction results in PENDING_HP_TIMER or CREDIT_HP_TIMER or PM_LC_TIMER Timeout DFP: Reception of OOBM. <i>LinkError</i>
Type 1/Type 2 Rx Buffer Credit Error	LCRD1_x or LCRD2_y was received out of order	Transition to LTSSM.ERROR state	UFP: Subsequent transaction results in PENDING_HP_TIMER or CREDIT_HP_TIMER or PM_LC_TIMER Timeout DFP: Reception of OOBM. <i>LinkError</i>
LGOOD_n with unexpected Header Sequence Number	The Header Sequence Number in the received LGOOD_n does not match any of the outstanding ACK Tx Header Sequence Numbers	Transition to LTSSM.ERROR state	UFP: Subsequent transaction results in PENDING_HP_TIMER or CREDIT_HP_TIMER or PM_LC_TIMER Timeout DFP: Reception of OOBM. <i>LinkError</i>

CREDIT_HP_TIMER Timeout	LCRD1_x or LCRD2 y not received upon CREDIT_HP_TIMER timeout.	Transition to LTSSM.ERROR state	UFP: Subsequent transaction results in PENDING_HP_TIMER or CREDIT_HP_TIMER or PM_LC_TIMER Timeout
			DFF: Reception of OOBM.LinkError
PM_ENTRY_TIMEOUT	Timeout after sending LAU without receiving LPMA	Transition to LTSSM.Ux state	None
PM_LC_TIMER Timeout	Timeout after sending LGO_Ux without receiving neither LAU nor LXU	Transition to LTSSM.ERROR state	UFP: Subsequent transaction results in PENDING_HP_TIMER or CREDIT_HP_TIMER or PM_LC_TIMER Timeout
			DFF: Reception of OOBM.LinkError
Invalid Link Command Word	Identifying an invalid link command word within a Gen T Link Command Tunneled Packet	Ignored	Subsequent transaction results in PENDING_HP_TIMER or CREDIT_HP_TIMER or PM_LC_TIMER Timeout
			Future Link Command Word may not be supported
Invalid OOBM	Identifying an invalid OOBM Tunneled Packet Payload if CRC check is correct.	Ignored	Transitioning to LTSSM.Error state on timeout, or no impact
Data Packet Framing Error	Packet is missing END/EDB symbols	Transition to LTSSM.ERROR state	UFP: Subsequent transaction results in PENDING_HP_TIMER or CREDIT_HP_TIMER or PM_LC_TIMER Timeout
			DFF: Reception of OOBM.LinkError

9.4.1.7 USB3 Gen T Link Timing Parameters

Table 9-12 lists the timing parameters (in addition to the Timing Parameters in Table 9-7) for an Internal USB3 Gen T Component. Table 9-13 lists the USB3 Timing parameters that are modified for an Internal USB3 Gen T Component.

Table 9-12. Additional USB3 Gen T Timing Parameters

Name	Description	Min	Max	Units
tOOBMPolling	Time between two OOBM Packets ¹	8	12	μs
tPortReadyTimeout	Time to successfully complete a Link Ready Handshake or Port Reset handshake	1000	1100	ms
tLC_AggrThreshold	Time before any pending Link Commands shall be sent	Gen 4: 440 Gen 3: 880	Gen 4: 950 Gen 3: 2100	ns
tUSB3KeepAliveTimeout	The time for the Gen T downstream port to wait for LKAR Link Command after transmitting LKAI_n Link Command on Link Keep-Alive activation.	20	--	μs
tUSB3KeepAliveResponse	The time for the Gen T upstream port to respond with LKAR Link Command after receiving LKAI_n Link Command.	--	1.5	μs
tUSB3KeepAliveUpdate	The time between transmitting two LKAI_n Link Commands with different encoding.	10	--	ms
1. The tOOBMPolling is a requirement for the Gen T Port transmitter. The time between two OOBM Packets at the Gen T Port receiver may be outside the tOOBMPolling timing definition.				

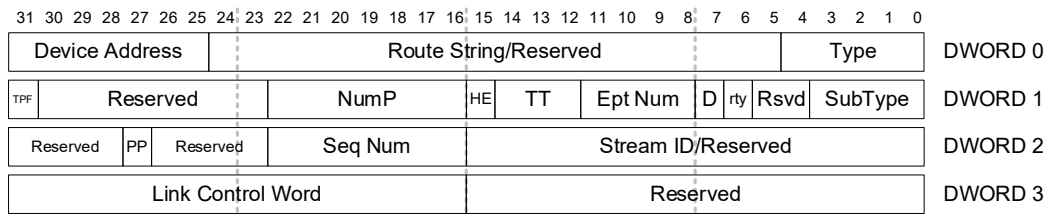
Table 9-13. Modified USB3 Gen T Timing Parameters

Name	Value
PENDING_HP_TIMER	200 μ s
PM_LC_TIMER	100 μ s
PM_ENTRY_TIMER	200 μ s
Ux_EXIT_TIMER	This timer is deprecated.
tDHPResponse	This timer is deprecated.

9.4.2 USB3 Protocol Layer**9.4.2.1 Transaction, Data, Isochronous Timestamp Packets**

The size of the *Seq Num* and *NumP* fields are increased in all TPs and DPHs when tunneling USB3 Gen T traffic. The *CRC-16* field in all TP, DPH, and ITP is deprecated and shall be set to zero. In addition, Isochronous Transfers are not supported in a USB4 Device tunneling USB3 Gen T traffic, the Transfer Type (TT) field setting for the Isochronous Transfer Type is deprecated and shall be Reserved.

An ACK TP shall have the format shown in Figure 9-27 with the modified fields described in Table 9-14.

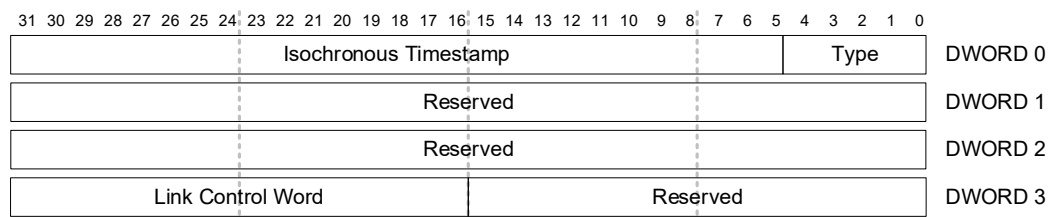
Figure 9-27. ACK Transaction Packet**Table 9-14. ACK TP Format**

Width (bits)	Offset (DW:bit)	Description																		
<u>3</u>	<u>1:12</u>	<p><u>Transfer Type (TT)</u></p> <p><u>When operating in SuperSpeed mode, the value of this field is Reserved and shall be set to zero.</u></p> <p><u>When operating in SuperSpeedPlus mode, this field is defined as follows:</u></p> <table><tr><th><u>Value</u></th><th><u>Meaning</u></th></tr><tr><td><u>100b</u></td><td><u>Control Transfer Type</u></td></tr><tr><td><u>101b</u></td><td><u>Reserved</u></td></tr><tr><td><u>110b</u></td><td><u>Bulk Transfer Type</u></td></tr><tr><td><u>111b</u></td><td><u>Interrupt Transfer Type</u></td></tr><tr><td><u>001b</u></td><td><u>Reserved</u></td></tr><tr><td><u>010b</u></td><td><u>Reserved</u></td></tr><tr><td><u>011b</u></td><td><u>Reserved</u></td></tr><tr><td><u>000b</u></td><td><u>Unknown for ACKs and deferred DPs originating from SuperSpeed bus instances. Reserved for all other ACKs and DPs. Refer to chapter 10.</u></td></tr></table>	<u>Value</u>	<u>Meaning</u>	<u>100b</u>	<u>Control Transfer Type</u>	<u>101b</u>	<u>Reserved</u>	<u>110b</u>	<u>Bulk Transfer Type</u>	<u>111b</u>	<u>Interrupt Transfer Type</u>	<u>001b</u>	<u>Reserved</u>	<u>010b</u>	<u>Reserved</u>	<u>011b</u>	<u>Reserved</u>	<u>000b</u>	<u>Unknown for ACKs and deferred DPs originating from SuperSpeed bus instances. Reserved for all other ACKs and DPs. Refer to chapter 10.</u>
<u>Value</u>	<u>Meaning</u>																			
<u>100b</u>	<u>Control Transfer Type</u>																			
<u>101b</u>	<u>Reserved</u>																			
<u>110b</u>	<u>Bulk Transfer Type</u>																			
<u>111b</u>	<u>Interrupt Transfer Type</u>																			
<u>001b</u>	<u>Reserved</u>																			
<u>010b</u>	<u>Reserved</u>																			
<u>011b</u>	<u>Reserved</u>																			
<u>000b</u>	<u>Unknown for ACKs and deferred DPs originating from SuperSpeed bus instances. Reserved for all other ACKs and DPs. Refer to chapter 10.</u>																			

Width (bits)	Offset (DW:bit)	Description
7	1:16	Number of Packets (NumP). This field is used to indicate the number of Data Packet buffers that the receiver can accept. The value in this field shall be less than or equal to the maximum burst size supported by the endpoint as determined by the value in the <i>bMaxBurst</i> field in the Endpoint Companion Descriptor (refer to Section 9.4.3.4).
8	1:23	Reserved.
7	2:16	Sequence Number (Seq Num). This field is used to identify the sequence number of the next expected data packet.
1	2:23	Reserved.
16	3:0	Reserved.

An Isochronous Timestamp Packet shall have the format shown in Figure 9-28.

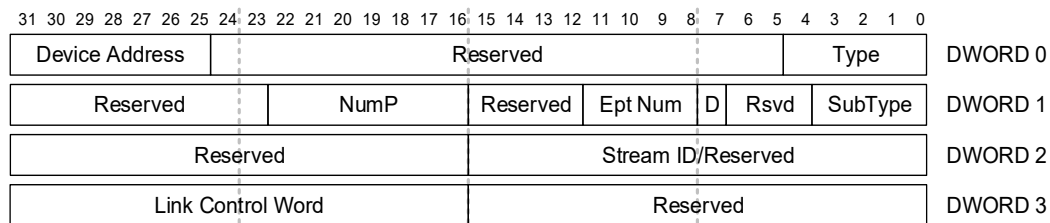
Figure 9-28. Isochronous Timestamp Packet



The Bus Interval Adjustment Control field is deprecated and shall not be sent by a USB4 Device tunneling USB3 Gen T traffic. The Correction field is not used and shall be Reserved in an Isochronous Timestamp Packet.

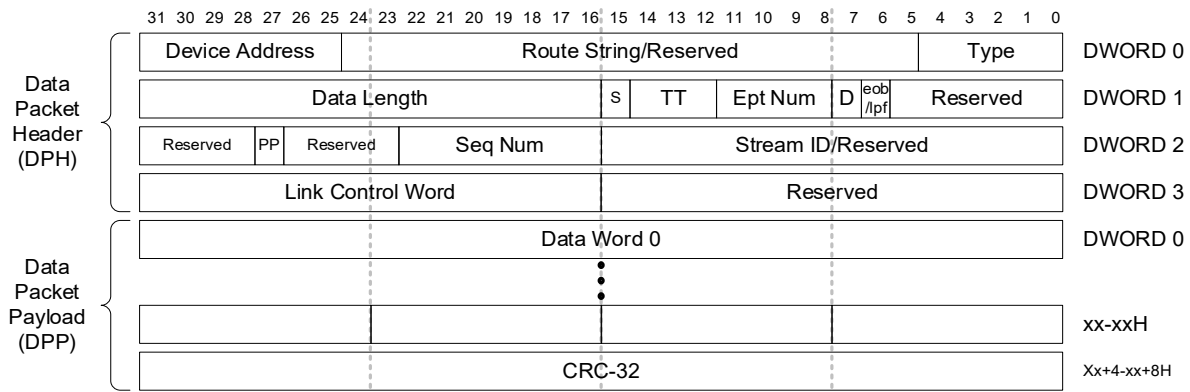
An ERDY TP shall have the format shown in Figure 9-29.

Figure 9-29. ERDY Transaction Packet



The SUBLINK_SPEED Device Notification TP is deprecated and shall not be sent by a USB4 Device tunneling USB3 Gen T traffic.

A Data Packet shall have the format shown in Figure 9-30 with the modified fields is described in Table 9-15.

Figure 9-30. Data Packet

Note : The additional length field following the DPH used by SuperSpeedPlus data packets is not used when operating in USB3 Gen T Mode.

Table 9-15. Data Packet Format

Width (bits)	Offset (DW:bit)	Description
6	1:0	Reserved.
7	2:16	Sequence Number (Seq Num). This field is used to identify the sequence number of the DP. Note that the sequence number wraps around at 127.
1	2:23	Reserved.

9.4.2.2 PING TPs

A USB4 Host may optionally send PING TPs to a USB4 Device when tunneling USB3 Gen T traffic because there is a virtual direct connection between the USB4 Host and the USB4 Device.

9.4.2.3 USB3 Gen T Burst Transactions

This section defines the additional burst requirements that apply to a USB3 Gen T Port.

A USB3 Gen T Port shall not exceed tGenTMaxBurstInterval time between DP bursts from a device endpoint to the host or from the host to a device endpoint.

Since the USB3 Gen T Tunneling architecture allows multiple IN endpoints, a single USB4 Device may be ready to burst multiple DPs from multiple endpoints whenever the link is available. A USB3 Gen T Port shall not exceed tGenTMaxDeviceMultiPacketInterval time between concurrent DP bursts from different device endpoints to the host.

9.4.2.4 USB3 Gen T Bulk/Interrupt IN and OUT Transactions

An Internal USB3 Gen T Component shall follow the rules defined in the USB 3.2 Specification for a SuperSpeedPlus Device with respect to Bulk and Interrupt IN/OUT transactions, except that the sequence number shall wrap around at 127 instead of 31.

Note: USB3 Gen T Interrupt endpoints can be allocated up to 70% of the total available bandwidth on the USB4 Link.

9.4.2.5 USB3 Gen T Control Transactions

An Internal USB3 Gen T Component shall follow the rules defined in the USB 3.2 Specification for a SuperSpeedPlus Device with respect to Control transactions, except that the sequence number shall wrap around at 127 instead of 31.

9.4.2.6 USB3 Gen T Isochronous Transactions

~~An Internal USB3 Gen T Component shall follow the rules defined in the USB 3.2 Specification for a SuperSpeedPlus Device with respect to Isochronous transactions, except for the following:~~

- ~~• The sequence number shall wrap around at 127 instead of 31.~~
- ~~• A USB3 Gen T Host Port shall be able to accept and send up to 96 DPs per endpoint per bus interval when tunneling USB3 Gen T traffic.~~

~~Note: Periodic endpoints can be allocated up to 70% of the total available bandwidth on the USB4 Link.~~

Isochronous Transfers are not supported in a USB4 Device tunneling USB3 Gen T traffic, and this section is deprecated.

9.4.2.7 USB3 Gen T Protocol Timing Parameters

Table 9-16 lists the timing parameters that an Internal USB3 Gen T Component shall adhere to when responding to ACKs while bursting.

Table 9-16. Timing Parameters

Name	Description	Min	Max	Units
tGenTMaxBurstInterval	When the device is operating in USB3 Gen T Mode, time between DP bursts from the device endpoint to the host.	--	50	ns
tGenTMaxDeviceMultiPacketInterval	When the device is operating in USB3 Gen T Mode, time between concurrent DP bursts from different device endpoints to the host.	--	50	ns

9.4.3 Framework Layer

9.4.3.1 USB Peripheral Device States

A USB4 Peripheral Device that supports USB3 Tunneling shall follow the USB Peripheral Operational Device State machine as shown in Figure 9-31. A USB4 Peripheral Device that is a Compound Device shall follow the Operational Device State Diagram in Figure 9-32.

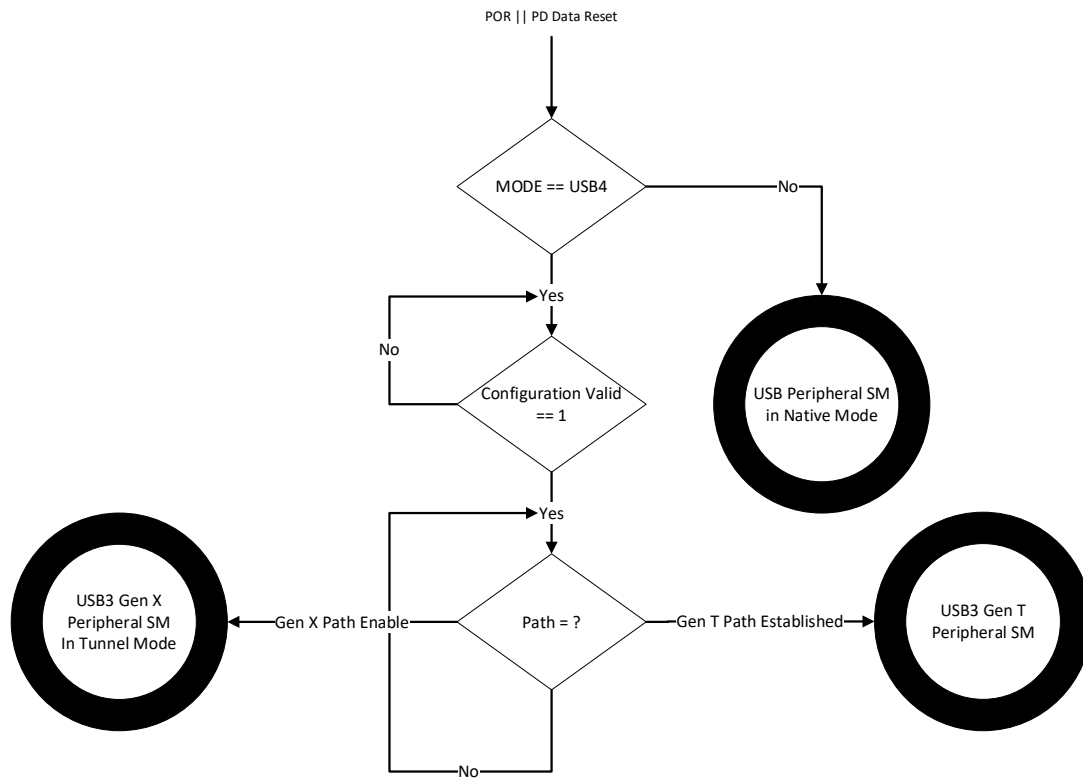
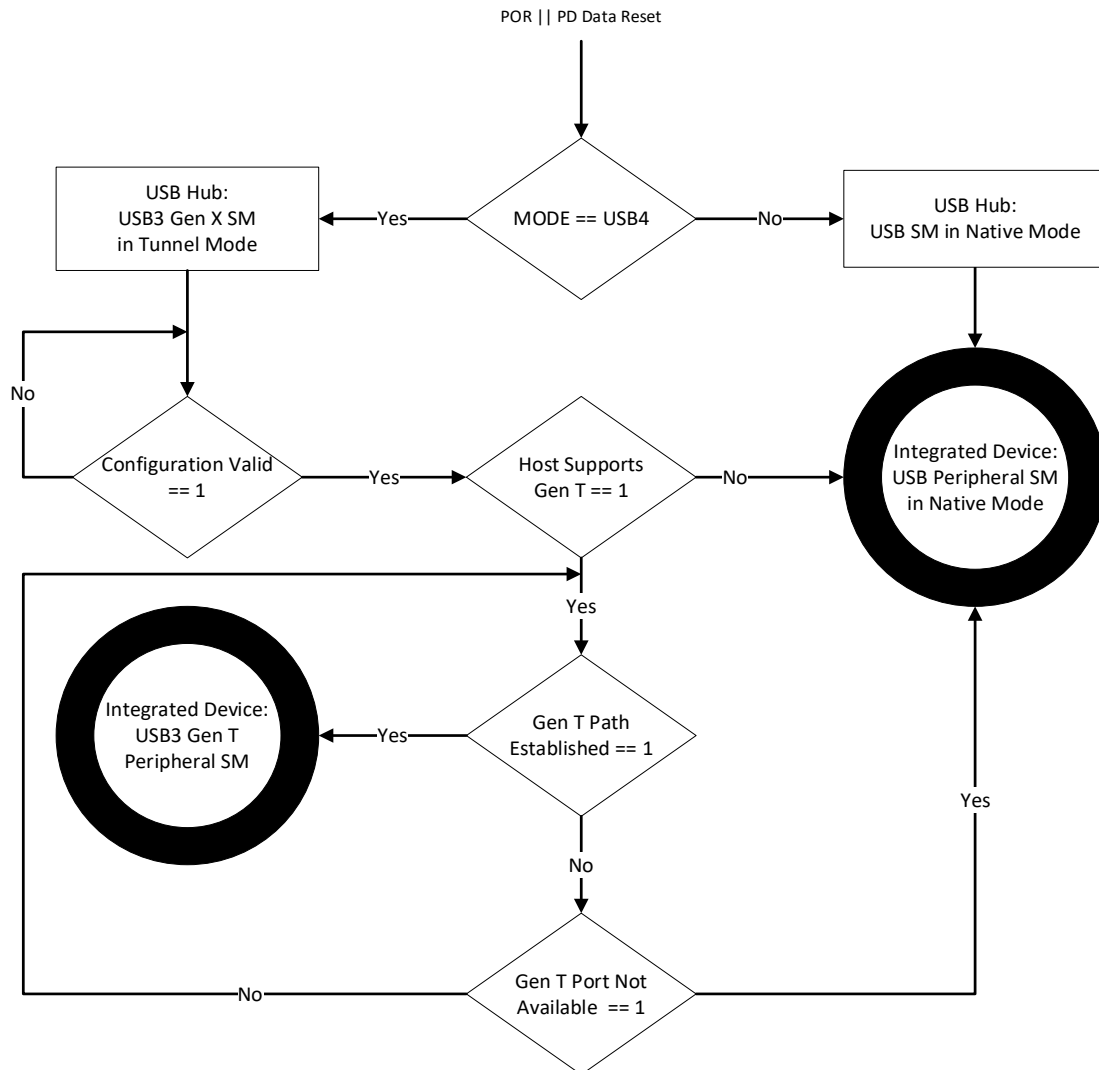
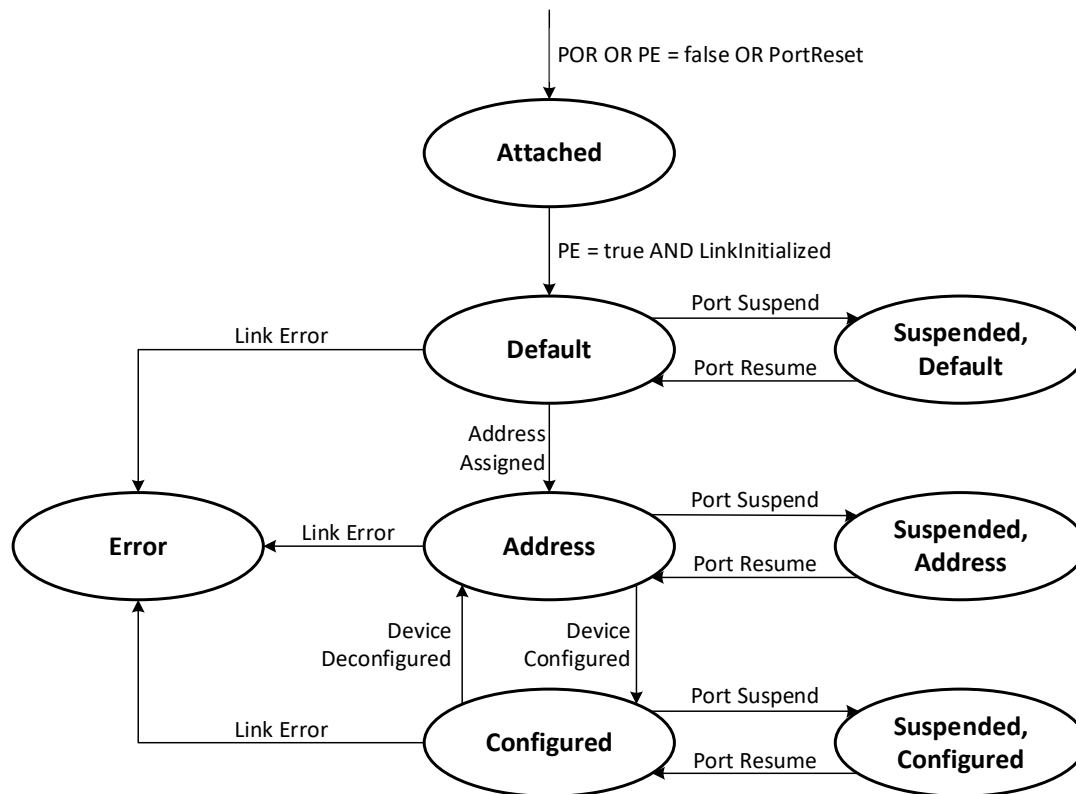
Figure 9-31. USB Peripheral Operational Device State Diagram

Figure 9-32. USB Compound Device Operational Device State Diagram

The USB2 Device State Machine (SM) for Native Mode is defined in the USB 2.0 specification, The USB3 Gen X Peripheral State Machine (SM) for both Native and Tunnel Modes is defined in USB 3.2 specification.

The USB3 Gen T Peripheral State machine is a simplified version of the existing USB3 Gen X USB Peripheral SM and is shown in Figure 9-33.

Figure 9-33. USB3 Gen T Peripheral State Diagram

When an Internal USB3 Gen T Peripheral is first powered on, it shall come up in the Attached state. The device shall stay in the Attached state until Path Established is true and the USB3 Link is initialized (*LinkInitialized* = 1b). After USB3 link initialization, the Internal USB3 Gen T Peripheral shall transition to the Default state. If the Internal USB3 Gen T Peripheral receives an *OOBM.PortReset* at any time, it shall transition to the Attached state.

The behavior in each state shall follow the requirements defined in Section 9.1 of the USB 3.2 Specification.

9.4.3.2 USB3 Gen T Device Capability Descriptor

An Internal USB3 Gen T Peripheral shall return a USB3 Gen T Device Capability Descriptor as part of its BOS Descriptor. The USB3 Gen T Device Capability Descriptor shall have the format defined in Table 9-17.

Note: This capability descriptor cannot be directly accessed with a *GetDescriptor()* or *SetDescriptor()* request.

Table 9-17. USB3 Gen T Device Capability Descriptor Format

Offset	Field	Size	Value	Description
0	<i>bLength</i>	1	Number	Size of descriptor
1	<i>bDescriptorType</i>	1	Constant	DEVICE CAPABILITY Descriptor type
2	<i>bDevCapabilityType</i>	1	Constant	Capability type: USB3_GEN_T

Offset	Field	Size	Value	Description								
3	<i>bmAttributes</i>	1	Bitmap	Bitmap encoding of supported device level features. <table><tr><th><u>Bit</u></th><th><u>Encoding</u></th></tr><tr><td>0</td><td>Reserved. Shall be set to zero.</td></tr><tr><td>1</td><td>Accurate ITP Required. A value of one in this bit location indicates that this device requires Accurate ITPs to properly function.</td></tr><tr><td>7:2</td><td>Reserved. Shall be set to zero.</td></tr></table>	<u>Bit</u>	<u>Encoding</u>	0	Reserved. Shall be set to zero.	1	Accurate ITP Required. A value of one in this bit location indicates that this device requires Accurate ITPs to properly function.	7:2	Reserved. Shall be set to zero.
<u>Bit</u>	<u>Encoding</u>											
0	Reserved. Shall be set to zero.											
1	Accurate ITP Required. A value of one in this bit location indicates that this device requires Accurate ITPs to properly function.											
7:2	Reserved. Shall be set to zero.											

9.4.3.3 SuperSpeedPlus USB Device Capability Descriptor

An Internal USB3 Gen T Peripheral shall return a SuperSpeedPlus USB Device Capability Descriptor as part of its BOS Descriptor. The SuperSpeedPlus USB Device Capability Descriptor shall have the same definition as described in the USB 3.2 Specification except for the *bmSublinkSpeedAttr* field, which shall have the format described in Table 9-18.

Table 9-18. Sublink Speed Attribute Format

Offset	Field	Size	Value	Description																																																	
12	<i>bmSublinkSpeedAttr[0]</i>	4	Bitmap	Sublink Speed Attribute. Bitmap encoding of a Sublink’s characteristics: <table><tr><th>Bit</th><th>Description</th></tr><tr><td>3:0</td><td>Sublink Speed Attribute ID (SSID). This field is an ID that uniquely identifies the speed of the sublink. Note that a maximum of 16 unique SSIDs may be defined.</td></tr><tr><td>5:4</td><td>Lane Speed Exponent (LSE). This field defines the base 10 exponent times 3, that shall be applied to the Lane Speed Mantissa (LSM) when calculating the maximum bit rate represented by this Lane Speed Attribute.<table><tr><th>LSE Value</th><th>Bit Rate</th></tr><tr><td>0</td><td>Bits per second</td></tr><tr><td>1</td><td>Kb/s</td></tr><tr><td>2</td><td>Mb/s</td></tr><tr><td>3</td><td>Gb/s</td></tr></table></td></tr><tr><td>7:6</td><td>Sublink Type (ST). This field identifies whether the Sublink Speed Attribute defines a symmetric or asymmetric bit rate. This field also indicates if this Sublink Speed Attribute defines the receive or transmit bit rate. Note that the Sublink Speed Attributes shall be paired, i.e. an Rx immediately followed by a Tx, and both Attributes shall define the same value for the SSID.<table><tr><th>Bit</th><th>Value</th><th>Description</th></tr><tr><td rowspan="2">6</td><td>0</td><td>Symmetric. Rx and Tx sublinks have the same number of lanes and operate at the same speed.</td></tr><tr><td>1</td><td>Asymmetric. Rx and Tx sublinks have different number of lanes and/or operate at different speeds.</td></tr><tr><td rowspan="2">7</td><td>0</td><td>Sublink operates in Receive mode</td></tr><tr><td>1</td><td>Sublink operates in Transmit mode</td></tr></table></td></tr><tr><td>8</td><td>Tunnel Support (TS). This field identifies if the link supports USB3 Tunnel operation. This field is valid for a Peripheral that is operating in either USB3 Gen X Mode or in USB3 Gen T Mode.</td></tr><tr><td>13:9</td><td>Reserved</td></tr><tr><td>15:14</td><td>Link Protocol (LP). This field identifies the protocol supported by the link.<table><tr><th>LP Value</th><th>Protocol</th></tr><tr><td>0</td><td>SuperSpeed</td></tr><tr><td>1</td><td>SuperSpeedPlus</td></tr><tr><td>2</td><td>USB3 Gen T</td></tr><tr><td>3</td><td>Reserved</td></tr></table></td></tr><tr><td>31:16</td><td>Lane Speed Mantissa (LSM). This field defines the mantissa that shall be applied to the LSE when calculating the maximum bit rate represented by Lane Speed Attribute.</td></tr></table>	Bit	Description	3:0	Sublink Speed Attribute ID (SSID). This field is an ID that uniquely identifies the speed of the sublink. Note that a maximum of 16 unique SSIDs may be defined.	5:4	Lane Speed Exponent (LSE). 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The valid link speeds for a USB3 Gen T Peripheral are defined in Table 9-19.

Table 9-19: USB3 Gen T Peripheral Valid Link Speeds

Active Rx Link Rate	Active Tx Link Rate	USB4 Gen Speed (tLC_AggrThreshold to use)
10 Gbps	10 Gbps	Gen 2 (Use Gen 3 tLC_AggrThreshold)
20 Gbps	20 Gbps	Gen 2 (Use Gen 3 tLC_AggrThreshold)
40 Gbps	40 Gbps	Gen 3
40 Gbps	80 Gbps	Gen 4
80 Gbps	40 Gbps	Gen 4
80 Gbps	80 Gbps	Gen 4
40 Gbps	120 Gbps	Gen 4
120 Gbps	40 Gbps	Gen 4

9.4.3.4 SuperSpeed Endpoint Companion Descriptor

An Internal USB3 Gen T Peripheral shall return a SuperSpeed Endpoint Companion Descriptor as part of its Configuration Descriptor. The SuperSpeed Endpoint Companion Descriptor shall have the same definition as described in the USB 3.2 Specification except for the *bMaxBurst* field, which shall have the format described in Table 9-20.

Table 9-20. bMaxBurst Format

Offset	Field	Size	Value	Description												
2	<i>bMaxBurst</i>	1	Number	<p>The maximum number of packets the endpoint can send or receive as part of a burst. Valid values are from 0 to 63. A value of 0 indicates that the endpoint can only burst one packet at a time and a value of 63 indicates that the endpoint can burst up to 64 packets at a time.</p> <p>For endpoints of type control this shall be set to 0.</p> <p>For endpoints of type bulk this shall be set to:</p> <table><tr><th>Speed</th><th>Minimum Burst Size</th><th>Maximum Burst Size</th></tr><tr><td>40</td><td>15</td><td>63</td></tr><tr><td>80</td><td>31</td><td>63</td></tr><tr><td>120</td><td>63</td><td>63</td></tr></table>	Speed	Minimum Burst Size	Maximum Burst Size	40	15	63	80	31	63	120	63	63
Speed	Minimum Burst Size	Maximum Burst Size														
40	15	63														
80	31	63														
120	63	63														

9.4.3.5 SuperSpeedPlus Isochronous Endpoint Companion Descriptor

An Internal USB3 Gen T Peripheral shall not return a SuperSpeed Isochronous Endpoint Companion Descriptor as part of its Configuration Descriptor. ~~if it includes an Isochronous Endpoint. The SuperSpeed Isochronous Endpoint Companion Descriptor shall have the same definition as described in the USB 3.2 Specification with the maximum value in the dwBytesPerInterval field limited to (MAX_ISO_BYTES_PER_BI_GEN1 x 2).~~

9.5 USB3 Gen T Paths

A USB3 Gen T Adapter interfaces to one or more USB3 Gen T Ports. When multiple USB3 Gen T Ports are supported, each Gen T Port has its own separate Path. A USB3 Gen T Adapter shall support a Path and implement a Path Configuration Space for each USB3 Gen T Port that it interfaces with.

A USB3 Gen T Adapter Layer assigns a unique index number to each USB3 Gen T Port that it interfaces with. This number is called the Gen T Port Index. The Gen T Port Index is used to help

route traffic to/from the various USB3 Gen T Ports and identify which DWs in the USB3 Gen T Adapter Configuration Capability map to each USB3 Gen T Port. The Gen T Port Index shall start at 0 and increment up by 1 for each additional USB3 Gen T Port that the USB3 Gen T Adapter Layer interfaces with.

When a USB3 Gen T Adapter Layer encapsulates traffic from a USB3 Gen T Port, it shall set the HopID in the resulting Tunneled Packet to $(8 + n)$, where n = the Gen T Index of the USB3 Gen T Port. When a USB3 Gen T Adapter Layer receives a Tunneled Packet with the HopID = $(8 + n)$, it shall route the payload from the Tunneled Packet to the USB3 Gen T Adapter with a Gen T Index = n .

In an SoC, a USB3 Gen T Port may be mapped to multiple USB3 Gen T Adapters and to multiple Host Routers. However, a USB3 Gen T Port can only operate with one Downstream USB3 Gen T Adapter at a time. To ensure that a Gen T Port is available for mapping to a Gen T Adapter, the Connection Manager negotiates the Gen T Port allocation with the Host Controller software.

9.5.1 Path Setup

When the *Path Enable* bit and the *Valid* bit in the USB3 Gen T Adapter Configuration Capability are set to 1b, a USB3 Gen T Adapter Layer shall indicate that Path Established is true to the corresponding USB3 Gen T Port. After the *Path Enable* bit and the *Valid* bit are set to 1b, the USB3 Gen T Adapter Layer may optionally issue USB3 Tunneled Packets to the Transport Layer.



CONNECTION MANAGER NOTE

Before setting up a USB3 Gen T Path to a USB3 Gen T Port, a Connection Manager shall request to allocate the Gen T Port by interfacing to the Host Controller software. A Connection Manager shall not set up a Path to a USB3 Gen T Port if that USB3 Gen T Port was not allocated to it.

If a Connection Manager does not set up a USB3 Gen T Path to a USB3 Gen T Port in a Device Router, it shall:

- *Set the Gen T Port Not Available bit that corresponds to that USB3 Gen T Port to 1b in the USB3 Gen T Adapter Configuration Capability.*
- *If the Gen X Adapter Coupled bit is set to 1b, set up a Gen X Path (see Section 9.3.1).*

To set up a USB3 Gen T Path, a Connection Manager shall:

1. *Set the Valid bit in the Path Configuration Space to 1b.*
2. *Configure the Active Tx Link Rate field in both the Downstream and Upstream USB3 Gen T Adapters to indicate the highest common capability between:*
 - *The local USB3 Gen T Port Maximum Tx Supported Link Rate.*
 - *The remote USB 3 Gen T Port Maximum Rx Supported Link Rate.*
 - *The USB4 Link speed that the USB3 Gen T Path traverses.*
3. *Configure the Active Rx Link Rate field in both the Downstream and Upstream USB3 Gen T Adapters to be the highest common capability between:*
 - *The local USB3 Gen T Port Maximum Rx Supported Link Rate.*
 - *The remote USB 3 Gen T Port Maximum Tx Supported Link Rate.*
 - *The USB4 Link speed that the USB3 Gen T Path traverses.*
4. *Set the Path Enable bit and the Valid bit in the USB3 Gen T Adapter Configuration Capability to 1b in both the Downstream and Upstream USB3 Gen T Adapters.*

**CONNECTION MANAGER NOTE**

When tearing down an old USB3 Path to a Gen T Port and before setting up a new USB3 Path to the same Gen T Port, a Connection Manager shall wait at least 500 ms after setting the Path Enable bit to 0b and the Valid bit to 1b. This is to allow enough time for the Internal USB3 Component port to reach the Disconnect state and the USB3 Host Controller software to be notified.

9.5.2 Path Teardown**CONNECTION MANAGER NOTE**

Before tearing down a USB3 Gen T Path, a Connection Manager shall disable the Path by setting the Path Enable bits to 0b and the Valid bits to 1b in both the Downstream and Upstream USB3 Gen T Adapter Configuration Capability.

After tearing down the USB3 Gen T Path, the Connection Manager shall request to de-allocate the Gen T Port by interfacing to the Host Controller software.

When a Device Router either detects a disconnect on an Upstream Facing Port, or a *Path Enable* bit is set to 0b and the *Valid* bit is set to 1b in the Upstream USB3 Gen T Adapter Configuration Capability, the Upstream USB3 Gen T Adapter Layer shall:

- Not issue any Tunneled Packets to the Transport Layer for that Path.
- Indicate to the corresponding USB3 Gen T Port that Path Established is false.

When a *Path Enable* bit in a Downstream USB3 Gen T Adapter (including a Downstream Port Disconnect, see Section 4.4.5.2.1) is set to 0b and the *Valid* bit is set to 1b in the USB3 Gen T Adapter Configuration Capability, the USB3 Gen T Adapter Layer shall:

- Not issue any Tunneled Packets for that Path to the Transport Layer.
- Indicate to the corresponding USB3 Gen T Port that Path Established is false.

9.6 Maximum Delay Requirements

This section defines the maximum delay for tunneled USB3 traffic through a USB4 topology. Defining the maximum delay ensures that a minimum level of performance is guaranteed.

The requirements in this section are applicable only when all of the following are true:

- The USB4 Link operates at Gen 3 or Gen 4 speeds.
- The USB3 link operates in Gen T mode or at Gen 2x2 speed.

Note: The timing parameters in this section do not include the additional delay due to another Transport Layer Packet or Ordered Set having priority in being transmitted. They also do not include the delay in transmission due to insufficient flow control credits.

9.6.1 Maximum Forward Delay Requirements (USB4 Gen X Only)

This section only applies to USB4 Hubs that are tunneling USB3 Gen X traffic.

When a USB4 Hub forwards a USB3 Data Packet from one USB-C port to another USB-C port, and both ports operate in USB4 mode, the USB4 Hub shall send the first bit of the Tunneled USB3 Data Packet within *tUSB3GenXPktFwd_DP* time after receiving the last bit of the last segment of the Tunneled USB3 Data Packet.

When a USB4 Hub forwards a USB3 ACK Packet from one USB-C port to another USB-C port, and both ports operate in USB4 mode, the USB4 Hub shall send the first bit of the Tunneled USB3 ACK Packet within *tUSB3GenXPktFwd_ACK* time after receiving the last bit of the Tunneled USB3 ACK Packet.

When a USB4 Hub forwards a USB3 Data Packet from one USB-C port to another USB-C port, and one port operates in USB3 mode while the other operates in USB4 mode, the USB4 Hub shall send the first bit of the USB3 Data Packet within *tUSB3GenXPktFwd_DP_Native* time after receiving the last bit of the USB3 Data Packet.

When a USB4 Hub forwards a USB3 ACK Packet from one USB-C port to another USB-C port, and one port operates in USB3 mode while the other operates in USB4 mode, the USB4 Hub shall send the first bit of the USB3 ACK Packet within *tUSB3GenXPktFwd_ACK_Native* from receiving the last bit of the USB3 ACK Packet.

9.6.2 Maximum Response Delay Requirements

9.6.2.1 Maximum Response Delay Requirements for USB4-Based Docks and Peripheral Devices

This section only applies to USB4-Based Docks and USB4 Peripherals that contain an embedded USB3 endpoint.

When a USB4-Based Dock or USB4 Peripheral Device receives a USB3 Data Packet that is targeted to one of its embedded USB3 Endpoints, it shall respond with an ACK Packet within *tUSB3DeviceDPtoACK* time after receiving the packet. The time is measured from reception of the last bit of the last segment of the Tunneled USB3 Data Packet to sending the first bit of the Tunneled USB3 ACK Packet.

When a USB4-Based Dock or a USB4 Peripheral Device receives a USB3 ACK Packet that is targeted to one of its embedded USB3 endpoints, it shall respond with a Data Packet within *tUSB3DeviceACKtoDP* time after receiving the packet. The time is measured from reception of the last bit of the Tunneled USB3 ACK Packet to sending the first bit of the first segment of the Tunneled USB3 Data Packet.

9.6.2.2 Maximum Response Delay Requirements for a USB4 Host

This section only applies to a USB4 Host that support USB3 Gen T Tunneling.

When a USB4 Host receives a USB3 Data Packet, it shall respond with an ACK Packet within *tUSB3HostDPtoACK* time after receiving the packet. The time is measured from reception of the last bit of the last segment of the Tunneled USB3 Data Packet to sending the first bit of the Tunneled USB3 ACK Packet.

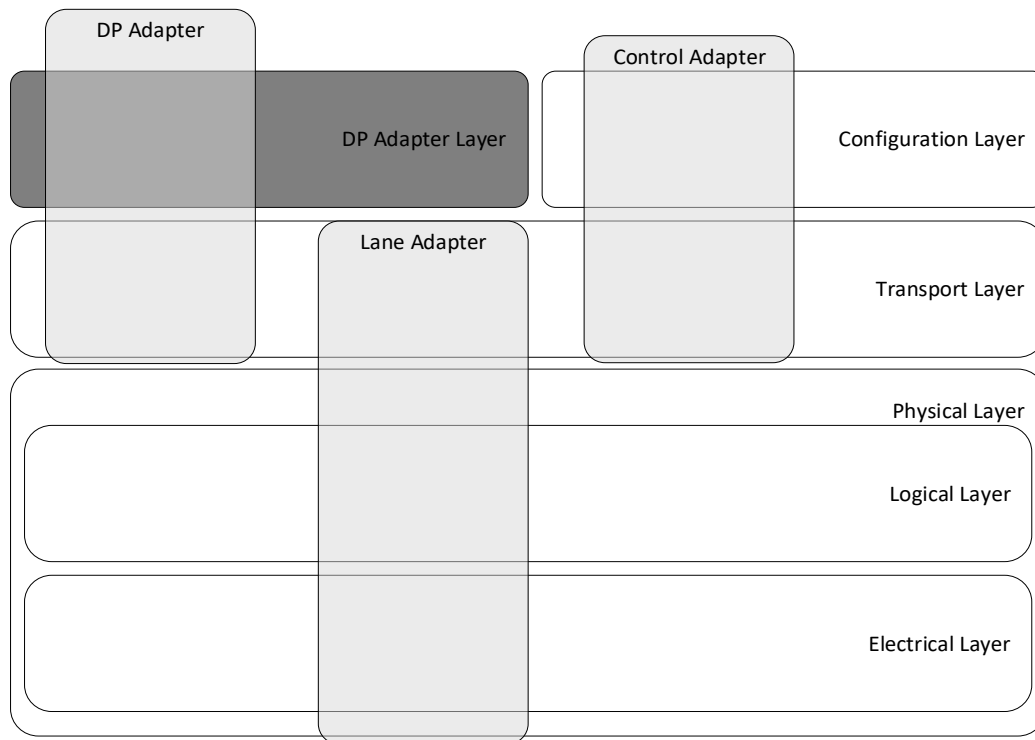
When a USB4 Host receives a USB3 ACK Packet, it shall respond with a Data Packet within *tUSB3HostACKtoDP* time after receiving the packet. The time is measured from reception of the last bit of the Tunneled USB3 ACK Packet to sending the first bit of the first segment of the Tunneled USB3 Data Packet.

9.7 Timing Parameters

Table 9-21. Timing Parameters

Name	Description	Min	Max	Units
tUSB3GenXPktFwd_DP	The maximum time between receiving a Data Packet on one USB-C port and sending it on another USB-C port when both ports operate in USB4 mode.	--	1250	ns
tUSB3GenXPktFwd_ACK	The maximum time between receiving an ACK Packet on one USB-C port and sending it on another USB-C port when both ports operate in USB4 mode.	--	1000	ns
tUSB3GenXPktFwd_DP_Native	The maximum time between receiving a Data Packet on one USB-C port and sending it on another USB-C port, when one port operates in USB3 mode and the other port operates in USB4 mode.	--	1050	ns

Name	Description	Min	Max	Units
tUSB3GenXPktFwd_ACK_Native	The maximum time between receiving an ACK Packet on one USB-C port and sending it on another USB-C port, when one port operates in USB3 mode and the other port operates in USB4 mode.	--	800	ns
tUSB3DeviceDPtoACK	For an internal USB3 peripheral device in a USB4-Based Dock or a USB4 Peripheral Device, the maximum time between receiving a Data Packet and sending an ACK Packet.	--	1500	ns
tUSB3DeviceACKtoDP	For an internal USB3 peripheral device in a USB4-Based Dock or a USB4 Peripheral Device, the maximum time between receiving an ACK Packet and sending a Data Packet.	--	1500	ns
tUSB3HostDPtoACK	For a USB4 host, the maximum time between receiving a Data Packet and sending an ACK Packet.	--	1500	ns
tUSB3HostACKtoDP	For a USB4 host, the maximum time between receiving an ACK Packet and sending a Data Packet.	--	1500	ns

10 DisplayPort™ Tunneling

This chapter describes DP IN and DP OUT Adapters, which tunnel DP traffic over the USB4® Fabric. This chapter only applies to USB4 products that implement DisplayPort Source or Sink.

A USB4 Host shall support DP tunneling. A Host Router shall contain at least one DP IN Adapter and may optionally contain one or more DP OUT Adapters.

A USB4 Hub shall support DP Tunneling. A USB4 Hub shall contain at least one DP OUT Adapter and may optionally contain one or more DP IN Adapters.

Note: The DP OUT Adapter in a USB4 Hub is to enable a DisplayPort Sink connected on a Downstream Facing Port (or non-USB display connector if USB4 Hub is a USB4-Based Dock), See the USB Type-C Specification for more details.

A USB4 Peripheral Device may optionally support DP Tunneling. If a USB4 Peripheral Device supports DP Tunneling, it shall contain at least one DP Adapter.

Table 10-1. DisplayPort Feature Requirements

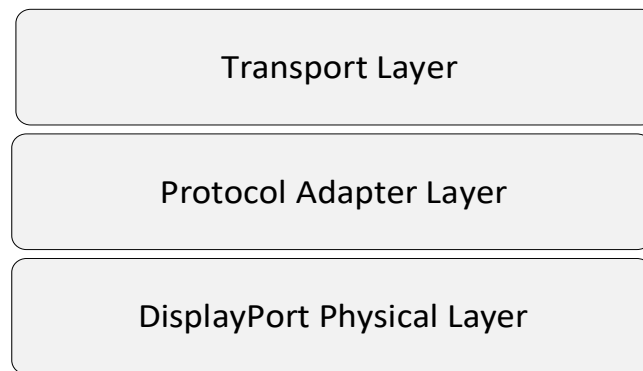
Feature/Attribute	Requirement
8b/10b Link Rate	Minimum: RBR (1.62Gbps)
UHBR	Optional
Lane Count	Minimum: 1 Lane
SST	Required
8b/10b MST	Optional
LTTPR Revision	20h
BW Allocation Mode	Required
DPRX Discovery	Required

Feature/Attribute	Requirement
SDP Split	Optional for a DP IN Adapter that is integrated with a DPTX that is not supporting SDP Split Required for all other DP Adapters
DSC	Required if UHBR is supported
8b/10b FEC	Required if DSC or Panel Replay Optimization are supported
Panel Replay Optimization	Optional
DPTX Discovery	Optional
ALPM	Optional

10.1 DP Adapter Protocol Stack

Figure 10-1 shows the protocol stack layers for a DP Adapter.

Figure 10-1. DP Adapter Protocol Stack Layers



10.1.1 Transport Layer

A DP IN Adapter and a DP OUT Adapter both implement a Transport Layer as described in Chapter 5.

10.1.2 Protocol Adapter Layer

The Protocol Adapter Layer in a DP IN Adapter encapsulates Main-Link data and AUX channel transactions into Tunneled Packets for transmission over the USB4 Fabric. It also reconstructs AUX channel transactions from Tunneled Packets received over the USB4 Fabric.

The Protocol Adapter Layer in a DP OUT Adapter reconstructs Main-Link data and AUX channel transactions from Tunneled Packets received over the USB4 Fabric. It also encapsulates AUX channel transactions into Tunneled Packets for transmission over the USB4 Fabric.

10.1.3 DP Physical Layer

A DP Adapter shall either implement the DisplayPort Physical Layer as defined in the DisplayPort Specification or shall implement its functional equivalent (e.g. DP Adapter is connected to a DPRX or a DPTX as part of an SoC).

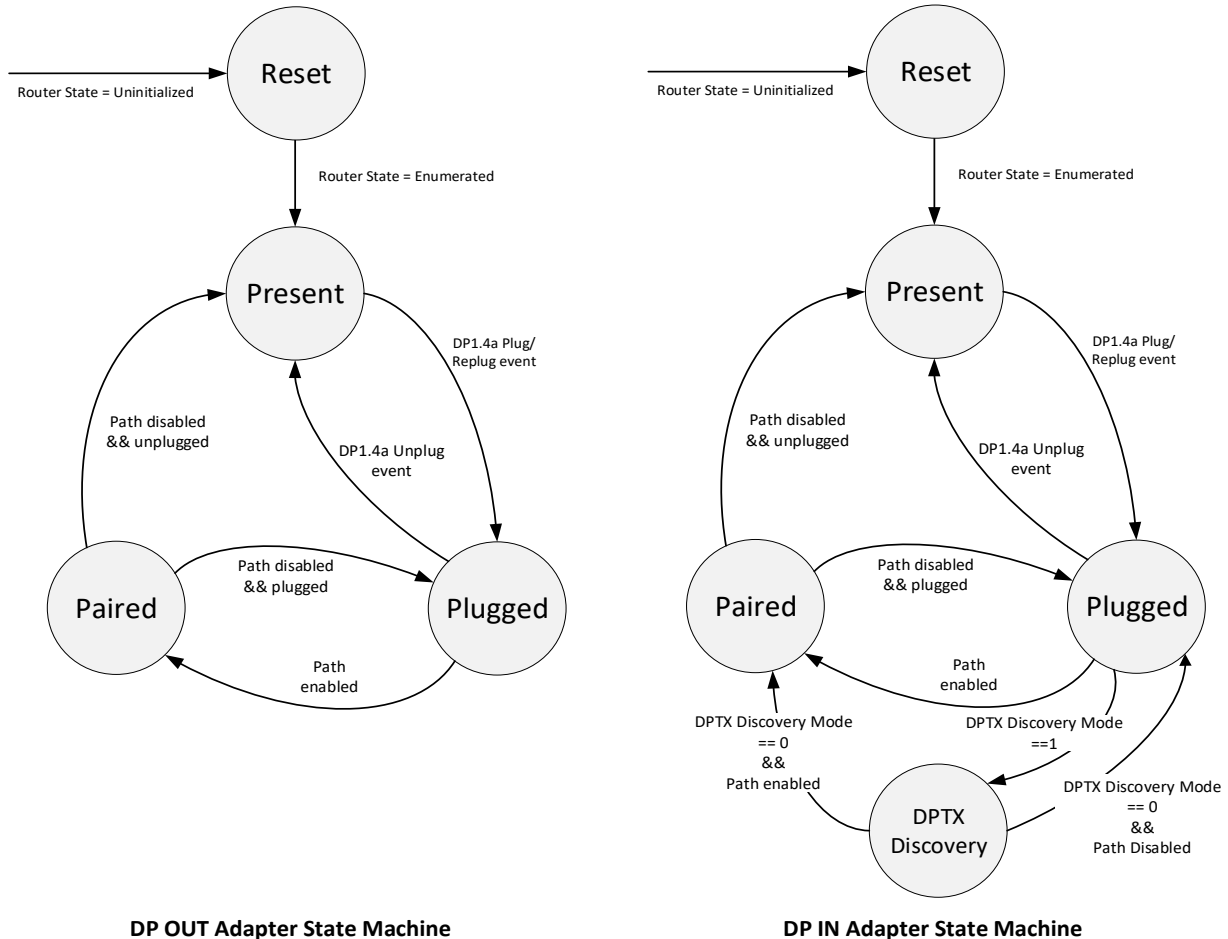
A DP IN Adapter which does not implement a Physical Layer shall generate a stream of DisplayPort Tunneled Packets as if a Physical Layer exists. This is to ensure that a DP OUT Adapter can properly reconstruct the DisplayPort Physical stream.

10.2 DP Adapter States

A DP IN Adapter and a DP OUT Adapter follow the state machine shown in Figure 10-2.

Note: A DP IN Adapter uses upstream device detection as defined in the DisplayPort Specification to determine when a Plug, Replug or Unplug event occurs. A DP OUT Adapter uses the hot plug detection method defined in the DisplayPort Specification to determine when a Plug, Replug or Unplug event occurs.

Figure 10-2. DP Adapter State Machines



10.2.1 Reset

A DP Adapter enters this state when the Router with the DP Adapter enters the Uninitialized state.

While in the Reset state, a DP Adapter shall set all Configuration Spaces to their default values. A DP IN Adapter shall drive HPD signal low. A DP OUT Adapter shall not apply DP_PWR.

A DP Adapter exits this state when the Router with the DP Adapter transitions to the Enumerated state.

10.2.2 Present

A DP Adapter enters this state upon any of the following conditions:

- The DP Adapter is in the Reset state and the Router with the DP Adapter is in the Enumerated state.
- The DP Adapter is in the Plugged state and an Unplug event occurs as defined in the DisplayPort Specification.

- The DP Adapter is in the Paired state and both of the following are true:
 - Either the AUX Path is disabled (*AE* bit is 0b) or the Video Path is disabled (*VE* bit is 0b).
 - The DP Adapter is unplugged as defined in the DisplayPort Specification.

While in the Present state, a DP Adapter shall set its Adapter Configuration Spaces to their default values. A DP IN Adapter shall drive HPD signal low. A DP OUT Adapter shall apply DP_PWR.

A DP Adapter exits this state upon a Plug or Replug event. Plug and Replug events are defined in the DisplayPort Specification.

10.2.3 Plugged

A DP Adapter enters this state upon any of the following conditions:

- A Plug or Replug event occurs as defined in the DisplayPort Specification.
- The AUX Path is disabled (*AE* bit is 0b), the Video Path is disabled (*VE* bit is 0b), and the DP Adapter is plugged as defined in the DisplayPort Specification.

A DP IN Adapter that supports DPTX Discovery transitions to this state from the DPTX Discovery state when the *DPTX Discovery Mode* bit is set to 0b and the DP Paths are disabled (*AE* bit is 0b or *VE* bit is 0b).

A DP IN Adapter exits this state upon any of the following conditions:

- An Unplug event as defined in the DisplayPort Specification.
- Both the AUX Path and Video Path are enabled (*AE* bit is 1b and *VE* bit is 1b).

A DP IN Adapter that supports DPTX Discovery exits this state and enters the DPTX Discovery state when the *DPTX Discovery Mode* bit is set to 1b.

A DP OUT Adapter and a DP OUT AUX Adapter exit this state upon any of the following conditions:

- An Unplug event as defined in the DisplayPort Specification.
- The AUX Path is enabled (i.e. the *AE* bit is set to 1b).

While in the Plugged state, a DP IN Adapter shall drive HPD signal low.

10.2.4 Paired

A DP IN Adapter transitions to this state from the Plugged state when both the AUX Path and Video Path are enabled (*AE* bit is 1b and *VE* bit is 1b). A DP OUT Adapter and a DP OUT AUX Adapter transition to this state from the Plugged state when the AUX Path is enabled (i.e. the *AE* bit is set to 1b).

A DP IN Adapter that supports DPTX Discovery transitions to this state from the DPTX Discovery state when the *DPTX Discovery Mode* bit is set to 0b and the DP Paths are enabled (*AE* bit is 1b and *VE* bit is 1b).

While in this state, a DP Adapter may send and receive Tunneled Packets over the USB4 Fabric.

A DP Adapter exits this state after the AUX Path is disabled (*AE* bit is 0b) or the Video Path is disabled (*VE* bit is 0b).

When a DP Adapter exit this state, it shall set its Adapter Configuration Spaces to their default values.

10.2.5 DPTX Discovery (DP IN Adapter Only)

A DP IN Adapter that supports DPTX Discovery transitions to this state from the Plugged state when the *DPTX Discovery Mode* bit is set to 1b.

A DP IN Adapter that supports DPTX Discovery exits this state when the *DPTX Discovery Mode* bit is set to 0b:

- If the DP Paths are enabled (*AE* bit is 1b and *VE* bit is 1b), the DP Adapter shall transition to Paired state.
- If the DP Paths are disabled (*AE* bit is 0b or *VE* bit is 0b), the DP Adapter shall transition to Plugged state.

While in this state, a DP IN Adapter behaves as defined in Section 10.8.2.1.

10.3 Interfaces**10.3.1 DisplayPort**

A DP Adapter shall support three modes of operation:

- LTTPR Non-Transparent – LT-tunable PHY Repeater (Non-Transparent Mode).
- LTTPR Transparent – LT-tunable PHY Repeater (Transparent Mode).
- Non-LTTPR – Non-LT-tunable PHY Repeater.

DisplayPort link training is executed over the tunnel in one of three ways:

- DPTX Managed, Sequential Link Training – In this method, the DPTX is aware and manages the link training of the two DisplayPort links: (1) the link between the DPTX and the DP IN Adapter and (2) the link between the DP OUT Adapter and the DPRX. Link training is done sequentially, where the upstream link (1) is trained first and the downstream link (2) is trained second. This method of link training is used when operating in LTTPR Non-Transparent mode. See Section 10.4.10.1.
- Autonomous, Concurrent Link Training – In this method, the DPTX does not manage link training between the DP OUT Adapter and the DPRX. Instead, it manages only the link training to the DP IN Adapter. The DP OUT Adapter manages the link training to DPRX in parallel to the link training between the DPTX and DP IN Adapter. The DP IN Adapter indicates upstream link training completion only after it is notified of the downstream link training completion by the DP OUT Adapter, ensuring the end-to-end link training completion by the time the DPTX exits the link training sequence. This method of link training is used when operating in Non-LTTPR and LTTPR Transparent modes. See Section 10.4.10.2.

Note: DP Tunneling may not operate correctly when conducting DisplayPort Link training in Non-LTTPR and LTTPR Transparent modes, in case all the below conditions are met:

- *At least one LTTPR is located between the DPTX and the DP IN Adapter.*
- *The DPTX applies SSC.*

The above limitation is due to a potential underrun at the DP OUT Adapter buffer which starts storing data on a non-SSC clock and later transitions to an SSC clock.

- DPTX Managed, Concurrent Link Training – In this method, the DPTX manages the overall link training process, which consists of link training initiation, transitioning between the different link training phases, and link training completion. The EQ DONE and CDS phases are performed concurrently and managed by each DFP per DP link. This method of link training is used when operating in 128b/132b LTTPR mode. See Section 10.4.10.3.

Aux Transaction handling has two major aspects to attend when executed over the tunnel:

- AUX Transaction initiation operates in two ways:
 - DPTX Only – In this mode only DPTX initiates AUX Transactions. This mode is used when operating in LTTTPR Non-Transparent mode. It is also used in LTTTPR Transparent mode when not in the process of Link Training.
 - DPTX and DP OUT Adapter – In this mode both, the DPTX and the DP OUT Adapter, are initiating AUX Transactions. A DP OUT Adapter mainly initiate AUX Transactions as part of the autonomous and concurrent Link Training Process. This mode is used when operating in:
 - Non-LTTTPR, see Section 10.4.4.2.3
 - LTTTPR Transparent Link Training, see Section 10.4.4.3.3
 - 128b/132b LTTTPR Link Training, see Section 10.4.10.3.
- Timeout and DEFER usage:
 - Allowed – A DP IN Adapter uses timeout to govern the AUX Link and uses AUX DEFER when timeout expires. This mode is used when operating in:
 - Non-LTTTPR mode, see Section 10.4.4.2.1.
 - LTTTPR Transparent, when addressing internal DPCD addresses, see Section 10.4.4.3.1.
 - 128b/132b LTTTPR Link Training, see Section 10.4.10.3.
 - Disallowed – A DP IN Adapter does not activate a timeout for AUX Responses, will not send DEFER and will not gate AUX Responses coming from DPRX. This mode is used when operating in LTTTPR Non-Transparent mode and LTTTPR Transparent when addressing noninternal DPCD addresses, see Section 10.4.4.3.1.

Table 10-2 summarizes the above modes of operations.

Table 10-2. DisplayPort Modes of Operation Over DisplayPort Tunneling

Mode	Link Training	AUX Transaction Initiation	AUX DEFER Usage
Non-LTTTPR	Autonomous, Concurrent	DPTX and DP OUT Adapter	Allowed
LTTTPR Transparent	Autonomous, Concurrent	DPTX and DP OUT Adapter	Addressing internal DPCD: Allowed Addressing noninternal DPCD: Disallowed
LTTTPR Non-Transparent	DPTX Managed, Sequential	DPTX Only	Disallowed
128b/132b LTTTPR	DPTX Managed, Concurrent	Intra AUX Hop enabled: DPTX and DP OUT Adapter Intra AUX Hop disabled: DPTX only	Intra AUX Hop enabled: allowed

			Intra AUX Hop disabled: disallowed
--	--	--	---------------------------------------

After reset, a DP Adapter shall operate in Non-LTTPR mode. A DP Adapter shall transition between the three modes as described in Section 10.4.6.1. A DP Adapter shall transition to Non-LTTPR mode upon exit from the Paired state.

Unless otherwise stated, the requirements in this chapter apply to DP Adapters in all three modes.

10.3.1.1 LTTPR Non-Transparent

A DP IN Adapter shall implement LTTPR UFP. A DP OUT Adapter shall implement LTTPR DFP. LTTPR UFP and LTTPR DFP are defined in the DisplayPort Specification.

10.3.1.2 Non-LTTPR

A DP IN Adapter shall implement Non-LTTPR Non-Transparent UFP. A DP OUT Adapter shall implement Non-LTTPR Non-Transparent DFP. In Non-LTTPR mode, unlike LTTPR mode, the DPTX is unaware of the existence of additional DP Links. From the DPTX point of view, each operation appears to be carried out as if the DPRX is directly attached to the DPTX. Non-LTTPR behavior is defined for AUX Handling in Section 10.4.4.2, Link Training in Section 10.4.10.2, and Connection Manager Discovery in Section 10.3.4.

10.3.1.3 LTTPR Transparent

Operating in LTTPR Transparent mode (i.e. handling AUX transactions and performing Link Training) is the same as operating in Non-LTTPR mode with the following exceptions:

- The timeouts and timers are different
- The DP IN Adapter does not send AUX DEFER as is the case with LTTPR Non-Transparent mode and does not gate AUX Transactions (see Section 10.4.4.2.2) except during autonomous, concurrent Link Training operation

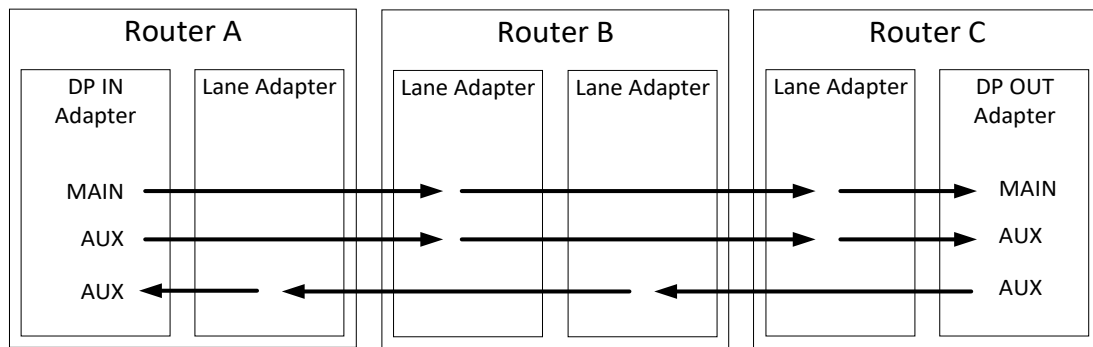
10.3.2 Programming Model

10.3.2.1 Adapter Configuration Space

A DP Adapter implements an Adapter Configuration Space as defined in Section 8.2.2.

10.3.2.2 Path Configuration Space

A DP Adapter shall implement a Path Configuration Space as defined in Section 8.2.3. As shown in Figure 10-3, a DP Adapter shall support one MAIN-Link Path, one AUX Ingress Path, and one AUX Egress Path. The AUX Ingress Path of the DP IN Adapter corresponds to the AUX Egress Path of the DP OUT Adapter and the AUX Egress Path of the DP IN Adapter corresponds to the AUX Ingress Path of the DP OUT Adapter.

Figure 10-3. DP Adapter Path Directions**10.3.3 Hot Plug and Hot Removal Events****10.3.3.1 DP OUT Adapter**

When a DP OUT Adapter detects a Plug Event (as defined in the DisplayPort Specification), it shall:

- Send a Hot Plug Event Packet with the *UPG* bit set to 0b as described in Section 6.8 within tDPPlug.
- Set the *Plugged* bit to 1b.

When a DP OUT Adapter detects an Unplug Event (as defined in the DisplayPort Specification), it shall:

- Send a Hot Plug Event Packet with the *UPG* bit set to 1b as described in Section 6.8 within tDPPlug.
- Set the *Plugged* bit to 0b.

10.3.3.2 DP IN Adapter

A Router shall send a Hot Plug Event Packet as described in Section 6.8 within tDPPlug of when both of the following are true:

- A DP IN Adapter detects a Source (as defined in the DisplayPort Specification).
- The DP IN Adapter that detected the Plug Event has sufficient DP stream resources available to support a DP stream.

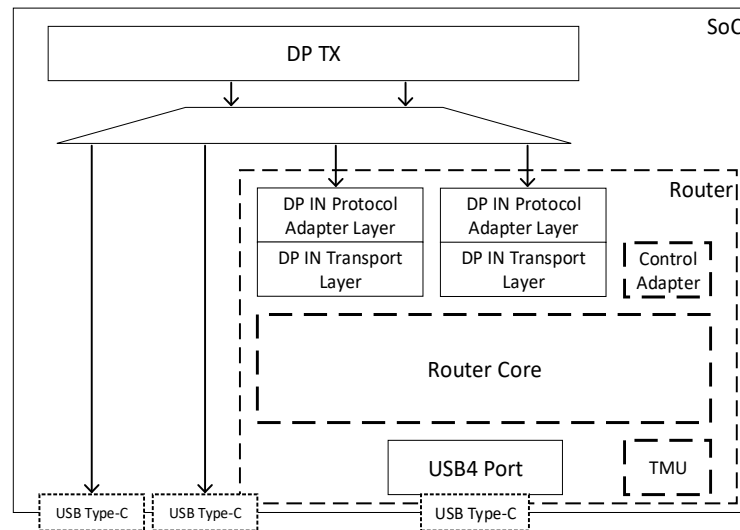
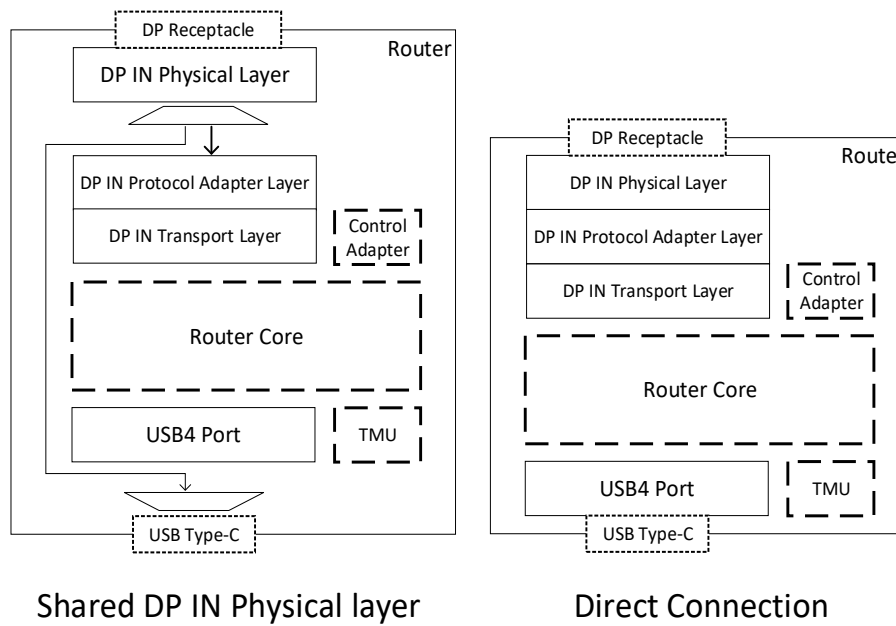
A Router shall send a Hot Plug Event Packet with the *UPG* bit set to 1b as described in Section 6.8 within tDPPlug of when either of the following are true:

- A DP IN Adapter detects the removal of a Source (as defined in the DisplayPort Specification).
- The Router has freed the DP stream resources allocated to the DP IN Adapter such that the DP IN Adapter can no longer support a DP stream.

DP stream resources allocation are managed by the Connection Manager using the DP Stream Resource Allocation Commands defined below in Section 10.3.3.2.1.

10.3.3.2.1 DP Stream Resource Allocation

Figure 10-4 shows three examples of how a DP stream resource can map to a DP IN Adapter within a Router.

Figure 10-4. DP Stream Resource Mapping Examples

A Router shall support the DP Stream Resource Commands listed in Table 10-3.

Table 10-3. DP Stream Resource Allocation Commands

Name	Purpose	Reference
QUERY_DP_RESOURCE	Queries a Router to determine whether a DP IN Adapter has sufficient DP stream resource availability for DP Tunneling.	Section 8.3.1.1.1
ALLOCATE_DP_RESOURCE	Causes a Router to allocate a DP stream resource to a DP IN Adapter.	Section 8.3.1.1.2
DEALLOCATE_DP_RESOURCE	Causes a Router to free a previously allocated DP stream resource.	Section 8.3.1.1.3

10.3.4 DisplayPort Over USB4 Fabric**10.3.4.1 DisplayPort Data Packet Types**

A DP Adapter encapsulates DisplayPort traffic into the Tunneled Packet types defined in this section. The Tunneled Packet types for DP Adapters are defined in Table 10-4 and Table 10-5. The Tunneled Packets types defined in Table 10-4 shall only be used for the AUX Path. The Tunneled Packet Types defined in Table 10-5 shall only be used for the Main-Link Path.

Table 10-4. AUX Path Tunneled Packet Types

PDF	Type	Reference
0h	AUX Packet	Section 10.3.4.2.1
1h	HPD Status Packet	Section 10.3.4.2.2
2h	SET_CONFIG Packet	Section 10.3.4.2.3
3h	ACK Packet	Section 10.3.4.2.4
4h-Dh	Reserved	--
Eh	PM Packet	Section 10.4.15.1
Fh	Reserved	--

Table 10-5. Main-Link Path Tunneled Packet Types

PDF	Type	Reference
0h	Reserved	
1h	SST Video Data Packet	Section 10.5.1.1
2h	SST Blank Start Packet	Section 10.5.1.3
3h	SST Main Stream Attribute Packet	Section 10.5.1.2
4h	SST Secondary Stream Packet	Section 10.5.1.4
5h	DP Clock Sync Packet	Section 10.6.1.3
6h	Multi Stream Packet	Section 10.5.2.3
7h	FEC Decode Packet	Section 10.5.3
8h	128b/132b LLCp Packet	Section 10.5.3.1
9h	128b/132b Control and Data Packet	Section 10.5.3.3.1
Ah	128b/132b Data Packet	Section 10.5.3.3.2
Bh	DP Link Control Packet	Section 10.3.4.3.1
Ch-Dh	Reserved	--
Eh	PM Packet	Section 10.4.15.2
Fh	Reserved	--

If a DP Adapter receives a Tunneled Packet on the AUX Path with a PDF value other than 0 to 3, it shall discard the Tunneled Packet and shall not send any Packets in response.

If a DP OUT Adapter receives a Tunneled Packet on the Main-Link Path with a PDF value other than 1 to Bh, it shall discard the Tunneled Packet and shall not send any Packets in response.

10.3.4.2 AUX Path Packets

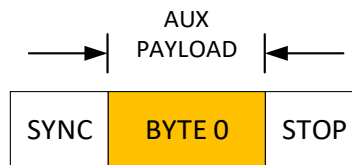
A DP Adapter Layer uses the HopID values in the *AUX Tx HopID* and *AUX Rx HopID* and fields in the Protocol Adapter Configuration Capability to identify AUX Path Packets. When generating an AUX Path Packet, a DP Adapter Layer shall put the value in the *AUX Tx HopID* field into the *HopID* field of the Tunneled Packet Header. When a DP Adapter Layer receives a Tunneled Packet with a HopID that is equal to the *AUX Rx HopID* field, it shall treat that packet as an AUX Path Packet.

10.3.4.2.1 AUX Packet

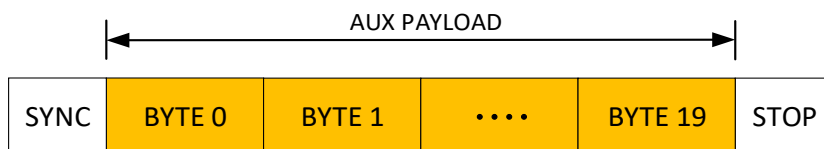
The DisplayPort AUX channel is a half-duplex, bi-directional channel. It is used to carry configuration messages. Configuration messages on the AUX channel use a request/response transaction format. The DisplayPort Specification requires each AUX channel transaction to be framed by <SYNC> and <STOP> symbols. Figure 10-5 shows the cases of the minimum and maximum sized AUX transactions.

Figure 10-5. AUX Channel Framing

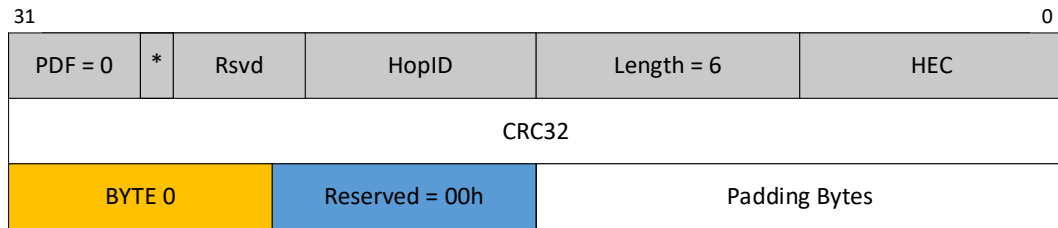
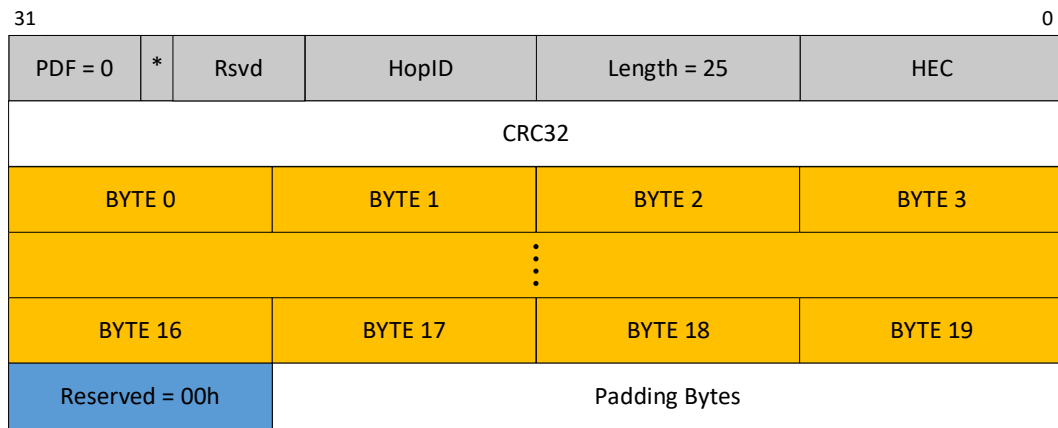
A) Minimum Size Aux Transaction



B) Maximum Size Aux Transaction



AUX Packets are used to forward AUX channel request and reply commands across the USB4 Fabric. Both command types, I2C-Over-AUX Transaction and DisplayPort Transaction, are supported. An AUX Packet shall have the format shown in Figure 10-6.

Figure 10-6. AUX Packet Format**A) Minimum Size Aux Packet****B) Maximum Size Aux Packet**

* SupplD

The Tunneled Packet Header for an AUX Packet shall have the *PDF* field set to 0.

AUX Packet payload shall contain the following:

- **CRC:** See Section 10.3.4.2.1.1.
- **AUX Payload:** Shall contain the bytes contained between the <SYNC> and <STOP> framing bytes of a DisplayPort AUX transaction. The number of bytes in this field varies between 1 and 20.
- **Reserved:** Shall be one byte set to 00h.

10.3.4.2.1.1 CRC

The CRC32 computation in an AUX Packet shall be based on the following CRC:

- Width: 32
- Poly: 1EDC 6F41h
- Init: FFFF FFFFh
- RefIn: True
- RefOut: True
- XorOut: FFFF FFFFh

The CRC32 protects the AUX Payload. The CRC32 is computed over 21 bytes regardless of the size of the AUX payload. If the AUX Payload is less than 21 bytes in length, a DP Adapter shall add the required number of zero-padding bytes for the computation of the CRC. The padding

bytes shall not be transmitted in the AUX Packet. The CRC32 shall be generated by the DP Adapter that creates the AUX Packet and shall be checked by the DP Adapter that receives the AUX Packet. A DP Adapter that receives an AUX Packet with a CRC error shall drop that packet.

Figure 10-7 shows an example of an AUX Packet with CRC32 calculated over 6 bytes of actual data.

Figure 10-7. AUX Packet Example

AUX ACK - 4 Bytes Read Respond

31					0
PDF = 0	*	Rsvd	HopID	Length = 10	HEC
CAh		5Ch	3Bh	C4h	
00h		14h	0Ah	C1h	
80h		Reserved = 00h	Padding Bytes		

* SupplD

10.3.4.2.2 HPD Packets

This packet is used by a DP OUT Adapter to notify a DP IN Adapter of a Plug, Re-Plug, or Unplug HPD event. An HPD Packet shall have the format shown in Figure 10-8.

Figure 10-8. HPD Packet Format

31					0
PDF = 1	*	Rsvd	HopID	Length = 4	HEC
P	Reserved				ECC

* SupplD

The *PDF* field in the header shall be set to 1 and the *Length* field shall be 4.

HPD Packet payload shall contain the following:

- **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the HPD Packet payload. See Section 5.1.2.3 for calculation.
- **Reserved [30:8]**: Shall be set to 0.
- **Plug (P) Flag [Bit 31]**: Shall be set to 0 if the HPD signal is low for more than 2 ms. Shall be set to 1 if the HPD signal is high.

A DP OUT Adapter sends an HPD Packet when it detects a Plug, Replug, or Unplug event (see Section 10.4.3). A DP OUT Adapter may also send an HPD Packet to the DP IN Adapter periodically.

When a DP IN Adapter receives an HPD Packet, it shall check the *ECC* field of the packet payload. The DP IN Adapter shall correct single-bit errors in the HPD Tunneled Packet payload. If an uncorrectable error is detected, the HPD Packet shall be dropped. Otherwise the DP IN Adapter shall:

- Generate a Plug/Re-plug HPD event if the *P Flag* in the HPD Packet payload is set to 1b.
- Generate an Unplug HPD event if the *P Flag* in the HPD Packet payload is set to 0b.
- Acknowledge the HPD Packet by sending an ACK Packet to the DP OUT Adapter within tDPAckResponse of receiving the HPD Packet.

If a DP OUT Adapter does not receive an ACK Packet with the *Type* field set equal to 8h within tDPAckTimeout of sending an HPD Packet, it may perform Link-Init as described in Section 10.4.13.

10.3.4.2.3 SET_CONFIG Packet

This packet is used to transport configuration commands between two DP Adapters. There are two versions of the SET_CONFIG Packet. Each version contains the same header, but the payload varies. Section 10.3.4.2.3.1 describes the format for a Version 1 SET_CONFIG Packet. Section 10.3.4.2.3.2 describes the format for a Version 2 SET_CONFIG Packet. Section 10.3.4.2.3.3 describes how SET_CONFIG Packets are processed.

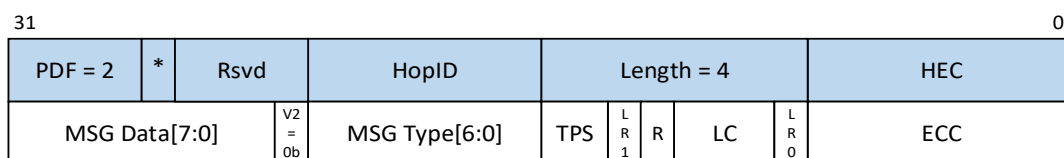
If both DP Adapters support Version 2 of the USB4 Specification (DP_COMMON_CAP.Protocol Adapter Version is 5h), then the DP Adapters shall use the Version 2 SET_CONFIG Packet. Otherwise, the DP Adapters shall use the Version 1 SET_CONFIG Packet.

The *PDF* field in the header of a SET_CONFIG Packet shall be set to 2 and the *Length* field shall be 4.

10.3.4.2.3.1 Version 1 SET_CONFIG Packet

A Version 1 SET_CONFIG Packet shall have the format show in Figure 10-9.

Figure 10-9. Version 1 SET_CONFIG Packet Format



* SupplD

A Version 1 SET_CONFIG Packet payload shall contain the following:

- **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the SET_CONFIG Packet payload. See Section 5.1.2.3 for calculation.
- **Link Rate 0 (LR0) [8]**: This field is used in combination with the *Link Rate 1 (LR1)* field as defined below.
- **Lane Count (LC) [11:9]**: This field shall specify the selected lane count according to the following encodings:
 - 000b: Link Down
 - 001b: 1 Lane
 - 010b: 2 Lanes
 - 100b: 4 Lanes
 All other values are reserved.

- **Reserved [12]:** This field shall be set to 1b by sender and ignored by receiver.
- **Link Rate 1 (LR1) [13]:** This field is used in combination with the *Link Rate 0 (LR0)* field where $LR = \{LR1, LR0\}$. The LR value shall specify the selected Link rate according to the following encodings:
 - 00b: 1.62 Gbps/lane
 - 01b: 2.70 Gbps/lane
 - 10b: 5.40 Gbps/lane
 - 11b: 8.10 Gbps/lane
 This field is only valid when the *Lane Count* field is greater than 000b.
- **Training Pattern Support (TPS) [15:14]:** This field shall specify the supported TPS which can be used in EQ Phase in Non-LTTPR and LTTPR Transparent link training.
 - **TPS3 Support [14]:**
 - 0b: TPS3 is not supported
 - 1b: TPS3 is supported
 - **TPS4 Support [15]:**
 - 0b: TPS4 is not supported
 - 1b: TPS4 is supported
- **MSG Type [22:16]:** This field specifies the MSG type of the SET_CONFIG Packet. This field shall carry one of the MSG Type values listed in Table 10-6.
- **Version 2 (V2) [23]:** This bit specifies the format of the SET_CONFIG Packet. This bit shall be set to 0b.
- **MSG Data [31:24]:** This field holds the MSG Data value that is associated with the specific MSG Type. The MSG Data shall match the MSG Type of the packet as set forth in Table 10-6.

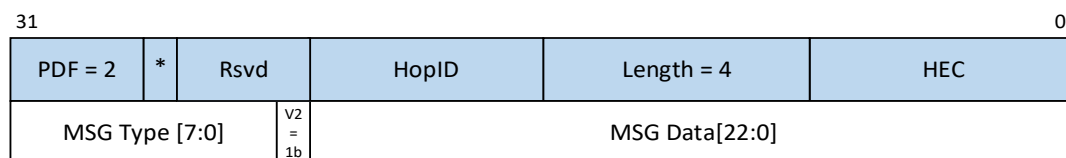
A DP IN Adapter shall set the *LC* and *LR* fields in all Version 1 SET_CONFIG Packets to be the same as the last 8B10B_SET_LINK SET_CONFIG Packet it sent. The exception to this rule is a 8B10B_SET_LINK SET_CONFIG Packet, which may alter those values as defined in Section 10.4.10.1.1 and Section 10.4.10.2.1.

A DP OUT Adapter shall set the *LC* and *LR* fields in all Version 1 SET_CONFIG Packets to the same values as in the last 8B10B_SET_LINK SET_CONFIG Packet it received.

10.3.4.2.3.2 Version 2 SET_CONFIG Packet

A Version 2 SET_CONFIG Packet shall have the format show in Figure 10-10.

Figure 10-10. Version 2 SET_CONFIG Packet Format



* SupplD

A Version 2 SET_CONFIG Packet payload shall contain the following:

- **MSG Data [22:0]:** This field holds the MSG Data value that is associated with the specific MSG Type. The MSG Data shall match the MSG Type of the packet as set forth in Table 10-6.

- **Version 2(V2) [23]:** This bit specifies the format of the SET_CONFIG Packet. This bit shall be set to 1b.
- **MSG Type [31:24]:** This field specifies the MSG type of the SET_CONFIG Packet. This field shall carry one of the MSG Type values listed in Table 10-6.

10.3.4.2.3.3 SET_CONFIG Packet Processing

The different SET_CONFIG Packet MSG types are listed in Table 10-6.

Table 10-6. SET_CONFIG Message Types

MSG Type	Type Value	Direction	MSG Data	Reference
8b10b_SET_LINK	0x01	Both	[0] – DP Link Training Mode 0b: Autonomous, concurrent (applicable to Non-LTTPR and LTTPR Transparent) 1b: DPTX-managed, sequential (applicable to LTTPR Non-Transparent) [7:1] – Reserved Version 2: [9:8] – Link Rate (LR) [12:10] – Lane Count (LC) [13] – TPS3 Support [14] – TPS4 Support [22:15] – Reserved <i>Note: The Version 2 definitions of the LR, LC, TPS3 Support and TPS4 Support fields are identical to those for the Version 1 SET_CONFIG Packet payload.</i>	Section 10.4.10 Section 10.4.12
8b10b_STATUS_TRAINING_FAIL	0x02	OUT to IN	[0] – LANE0_CHANNEL_EQ_DONE [1] – LANE0_SYMBOL_LOCKED [2] – LANE1_CHANNEL_EQ_DONE [3] – LANE1_SYMBOL_LOCKED [4] – LANE2_CHANNEL_EQ_DONE [5] – LANE2_SYMBOL_LOCKED [6] – LANE3_CHANNEL_EQ_DONE [7] – LANE3_SYMBOL_LOCKED Version 2: [22:8] – Reserved	Section 10.4.10.2
8b10b_STATUS_LOST_CONNECTION	0x03	OUT to IN	[7:0] – Reserved Version 2: [22:8] – Reserved	Section 13.8.2
SET_PHY_TEST_MODE	0x05	IN to OUT	[7:0] – Reserved Version 2: [22:8] – Reserved	Section 10.4.14
SET_DOWNSPREAD	0x07	IN to OUT	[7:0] Value written to DPCD 00107h Sent only by DP IN Adapter with DP_LOCAL_CAP.Protocol Adapter Version lower than 5.	Section 10.4.7
SET_POWER	0x08	IN to OUT	[2:0] – Power state as written/read to/from DPCD 600h [7:3] – Reserved Version 2: [22:8] – Reserved	Section 10.4.11 Section 13.8.5

MSG Type	Type Value	Direction	MSG Data	Reference
SET_MFDP	0x09	Both	[0] – MFDP Enable 0: MFDP Disabled 1: MFDP Enabled [7:1] – Reserved Version 2: [22:8] – Reserved	Section 10.4.5
SET_FEC_READY	0x0A	Both	[0] – Ready bit as written to DPCD 120h 0: Disable 1: Enable [7:1] – Reserved Version 2: [22:8] – Reserved	Section 10.4.9
SET_SINK_COUNT	0x0C	Both	[5:0] – SINK_COUNT The value return by reading DPCD 200h [7:6] – Reserved Version 2: [22:8] – Reserved	Section 10.4.6.3 Section 13.8.4
IRQ	0x0D	OUT to IN	[7:0] – Reserved	Section 10.4.3.3
SET_STREAM_MODE	0x0F	Both	[0] – Mode 0: SST Mode 1: MST Mode [7:1] – Reserved Version 2: [22:8] – Reserved	Section 10.4.8
SET_AUX_INIT	0x12	Both	[0] – 1b [7:1] – Reserved Version 2: [22:8] – Reserved	Section 10.4.5
SET_CMN_DPRX	0x13	IN to OUT	[7:0] – DPRX DPCD Revision 10h: DPCD r1.0 11h: DPCD r1.1 12h: DPCD r1.2 13h: DPCD r1.3 14h: DPCD r1.4a All other values are Reserved Version 2: [22:8] – Reserved	Section 10.4.6.2
SET_LTTTPR_MODE	0x17	IN to OUT	[0] – LTTTPR_Mode 0: LTTTPR Transparent 1: LTTTPR Non-Transparent [7:1] – Reserved Version 2: [10:8] – Downstream_LTTTPRs [11] – Downstream_LTTTPRs_Valid [22:12] – Reserved	Section 10.4.6.1
8b10b_SET_TRAINING	0x18	IN to OUT	[7:0] – Training Stage (TS) 0h: Training Done with DPRX 1h: TPS1 2h: TPS2 3h: TPS3 7h: TPS4 FFh: Training Done with LTTTPR Non-Transparent UFP All other values are Reserved Version 2: [22:8] – Reserved	Section 10.4.10.1

MSG Type	Type Value	Direction	MSG Data	Reference
8b10b_SET_VSPE	0x19	IN to OUT	[1:0] – Voltage Swing Level. [2] – Max Swing Reached [4:3] – Pre-emphasis Level. [5] – Max Pre Emphasis Reached [7:6] – Reserved Version 2: [22:8] – Reserved	Section 10.4.10.1
8b10b_STATUS_CR_DONE	0x1D	OUT to IN	[0] – CR_DONE0 for Lane 0 [1] – CR_DONE1 for Lane 1 [2] – CR_DONE2 for Lane 2 [3] – CR_DONE3 for Lane 3 [6:4] – Reserved [7] – Phase: 0b: Status at end of CR_DONE Phase 1b: Status at end of EQ Phase Version 2: [22:8] – Reserved	Section 10.4.10.2
128b132b_SET_LINK	0x21	IN to OUT	[7:0] – LINK_BW_SET 00h = Link Down 01h = 10Gbps/lane (UHBR10) 02h = 20Gbps/lane (UHBR20) 04h = 13.5Gbps/lane (UHBR13.5) All other values are Reserved [11:8] – LANE_COUNT_SET 00h = Link Down 01h = One lane (lane 0 only) 02h = Two lanes (lanes 0 and 1 only) 04h = Four lanes (lanes 0, 1, 2, and 3) All other values are Reserved [22:12] – Reserved	Section 10.4.10.4
128b132b_EQ_DONE	0x22	OUT to IN	[0] – Local EQ_DONE Succeeded 0b = Local EQ_DONE phase exited and all active lanes did not report LANEx_CHANNEL_EQ_DONE = 1b 1b = Local EQ_DONE phase exited and all active lanes reported LANEx_CHANNEL_EQ_DONE = 1b [1] – 128b/132b_DPRX_EQ_INTER_LANEALIGN_DONE 0b = EQ_DONE phase ended with a failure 1b = EQ_DONE phase ended successfully [2] – 128b/132b_LT_FAILED 0b = EQ_DONE phase ended successfully 1b = EQ_DONE phase ended with failure [22:3] – Reserved	Section 10.4.10.4
128b132b_CDS	0x23	IN to OUT	[22:0] – Reserved	Section 10.4.10.4
128b132b_CDS_DONE	0x24	OUT to IN	[22:0] – Reserved	Section 10.4.10.4
128b132b_SWITCH_TO_1BIT_CDI	0x25	IN to OUT	[22:0] – Reserved	Section 10.4.10.4
128b132b_SWITCH_TO_1BIT_CDI_DONE	0x26	OUT to IN	[22:0] – Reserved	Section 10.4.10.4

MSG Type	Type Value	Direction	MSG Data	Reference
128b132b_LT_ABORT	0x27	IN to OUT	[22:0] – Reserved	Section 10.4.10.4
128b132b_LT_ABORT_DONE	0x28	OUT to IN	[22:0] – Reserved	Section 10.4.10.4
AUX_PATH_CLX	0x30	IN to OUT	[0] – S/W 0 – Wake indication 1 – Sleep indication [22:1] – Reserved	Section 10.4.15
CABLE_DISCOVERY	0x31	Both	[1:0] – UHBR10_20_Support 00b – No UHBR supported or unknown 01b – UHBR10 supported 10b – UHBR10 and UHBR20 supported 11b – Reserved [2] – UHBR13.5 Support 0b – Not supported 1b – Supported [3] – Reserved [6:4] – Cable Type 000b – Unknown cable type 001b – Passive cable 010b – Active LRD cable 011b – Active Re-timer cable 100b – 111b – Reserved [22:7] – Reserved	Section 10.4.5.2

After a DP Adapter sends a SET_CONFIG Packet, it shall wait for an ACK Packet with the *Type* field equal to 0h. After receiving an ACK Packet with the *Type* field set to 0h, the DP Adapter shall wait tDPSetConfigGap before sending the next SET_CONFIG Packet.

When a DP Adapter receives a Version 1 SET_CONFIG Packet, it shall check the *ECC* field of the packet payload. The DP Adapter shall correct single-bit errors in the Version 1 SET_CONFIG Packet payload. If an uncorrectable error is detected, the Version 1 SET_CONFIG Packet shall be dropped. Otherwise, the DP Adapter shall respond with an ACK Packet with the *Type* field equal to 0h. The ACK Packet shall be sent within tDPAckResponse of receiving the SET_CONFIG Packet. If a DP Adapter does not receive an ACK Packet with the *Type* field equal to 0h within tDPAckTimeout of sending a SET_CONFIG Packet, it may issue Link-Init as described in Section 10.4.13.

A DP Adapter that receives a SET_CONFIG Packet with a value in the *Type* field that is not listed in Table 10-6 shall respond with an ACK packet with the *Type* field equal to 0h.

10.3.4.2.4 ACK Packet

An ACK Packet is used to acknowledge receipt of an HPD or SET_CONFIG Packet. An ACK Packet shall have the format shown in Figure 10-11.

Figure 10-11. ACK Packet Format

* SupplD

The *PDF* field in the header shall be set to 3 and the *Length* field shall be 4.

ACK Packet payload shall contain the following:

- **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the ACK Packet payload. See Section 5.1.2.3 for calculation.
- **Reserved [27:8]**: Shall be set to 0.
- **Type [31:28]**: Shall be set to 8h to acknowledge the receipt of a HPD Packet. Shall be set to 0h to acknowledge the receipt of a SET_CONFIG Packet. All other values are reserved.

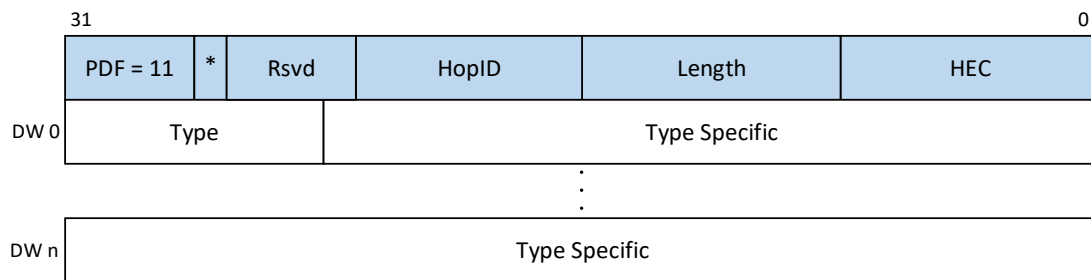
10.3.4.3 Main-Link Path Packets

A DP Adapter Layer uses the HopID values in the *Video HopID* field in the Protocol Adapter Configuration Capability to identify Main-Link Path Packets. When generating a Main-Link Path Packet, a DP IN Adapter Layer shall put the value in the *Video HopID* field into the *HopID* field of the Tunneled Packet Header. When a DP OUT Adapter Layer receives a Tunneled Packet with a HopID that is equal to the *Video HopID* field, it shall treat that packet as a Main-Link Path Packet.

Main-Link Path Packets are described in detail in Section 10.5 and Section 10.6.

10.3.4.3.1 DP Link Control Packet

This packet is used by a DP IN Adapter to inform a DP OUT Adapter about DP Link events. A DP Link Control Packet shall have the format shown in Figure 10-12.

Figure 10-12. DP Link Control Packet Format

* SupplD

The *PDF* field in the header shall be set to 11.

A DP Link Control Packet payload shall contain the following:

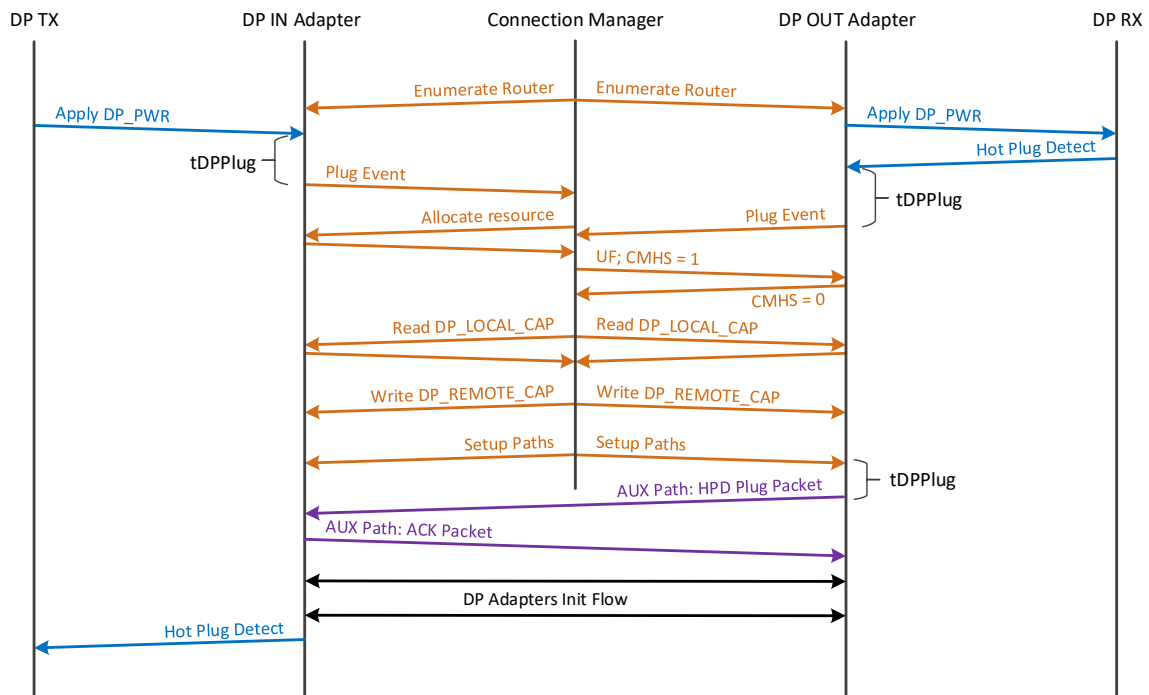
- **Type (DW 0 [31:24])**: This field specifies the type of the DP Link Control Packet. This field shall carry one of the Type values listed in Table 10-7.
- Rest of the payload is Type specific

Table 10-7. DP Link Control Packet Types

Type	Type Value	Reference
ALPM	0x01	Section 10.5.7

10.4 System Flows**10.4.1 Connection Manager Discovery**

Figure 10-13 shows the sequence of events that take place between a DP Source plug and Hot Plug Detect.

Figure 10-13. Power On to HPD Sequence**CONNECTION MANAGER NOTE**

A Connection Manager shall not pair a DP IN Adapter until after all the following occur:

- The Connection Manager has either received a Hot Plug Event Packet from the DP IN Adapter or the CM has confirmed that the DP IN Adapter is available using a QUERY_DP_RESOURCE command as described in Section 8.3.1.1.1, with the DisplayPort Number parameter equal to the DP IN Adapter Number.
- The Connection Manager has allocated a DP stream resource using an ALLOCATE_DP_RESOURCE command as described in Section 8.3.1.1.2, with a DisplayPort Number parameter equal to the DP IN Adapter Number.

A Connection Manager shall not pair a DP OUT Adapter until after either the Connection Manager has received a Hot Plug Event Packet from the DP OUT Adapter or the ADP_DP_CS_2.HPD Status is set to 1b in the DP OUT Adapter Configuration Capability field.

10.4.2 Path Configuration**10.4.2.1 Setup**

A DP OUT Adapter shall poll the DP_STATUS.CMHS field and DP_REMOTE_CAP.Protocol Adapter Version field for as long as the values in those fields are both 0. When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.Protocol Adapter Version > 0, the DP OUT Adapter shall do the following:

- If DP_REMOTE_CAP.Protocol Adapter Version was set to non-zero value while DP_STATUS_CTRL.CMHS remained zero, a DP OUT Adapter shall conclude it is a TBT3 Connection Manager and shall continue the flow as defined in Section 13.8.3.
- If DP_STATUS_CTRL.CMHS is set to 1 and DP_STATUS_CTRL.UF is zero, a DP OUT Adapter shall conclude it is a TBT3 DP IN Adapter and shall continue the flow as defined in Section 13.8.3.
- If DP_STATUS_CTRL.CMHS is set to 1 and DP_STATUS_CTRL.UF is set to one, a DP OUT Adapter shall reset DP_STATUS_CTRL.CMHS to zero. A Router shall set DP_STATUS_CTRL.CMHS to 0b within tCMHSClear time after DP_STATUS_CTRL.CMHS is set to 1b.

A DP Adapter shall set the DP_COMMON_CAP register, to reflect the lowest common capability between DP_LOCAL_CAP and DP_REMOTE_CAP fields.

After Path configuration, a Connection Manager enables the DP Adapters at both ends of the Path by setting the VE (Video Enable) and AE (Aux Enable) bits in the ADP_DP_CS_0 registers of the Protocol Adapters to 1b.

**CONNECTION MANAGER NOTE**

Before configuring a Path between DP IN and DP OUT Adapters, the Connection Manager shall perform the following steps:

1. **Available Bandwidth** – A Connection Manager calculates the available bandwidth on each USB4 Link along the entire Path, from DP IN Adapter to DP OUT Adapter. Based on the minimum available bandwidth, it concludes what DP Link can be established. Table 10-8 shows the Asynchronous Bandwidth needed for each DP link lane count and link rate.
2. **Capabilities Exchange** – A Connection Manager does the following:
 - a. Sets the DP OUT Adapter field, DP_STATUS_CTRL.UF, according to the revision supported by the paired DP IN Adapter.
 - b. Sets the DP OUT Adapter DP_STATUS_CTRL.CMHS to 1b.
 - c. Polls the DP OUT Adapter DP_STATUS_CTRL.CMHS until it is reset to zero by the DP OUT Adapter.
 - d. Reads the DP_LOCAL_CAP register of the DP IN and DP OUT Adapters at each end of the Path:
 - The Connection Manager copies the value read from the DP_LOCAL_CAP register of the DP IN Adapter to the DP_REMOTE_CAP register of the DP OUT Adapter.
 - The Connection Manager copies the value read from the DP_LOCAL_CAP register of the DP OUT Adapter to the DP_REMOTE_CAP register of the DP IN Adapter.
 - **Limit DP BW** – If available bandwidth is insufficient with respect to the required bandwidth in Table 10-8, the Connection Manager limits the DP Link, lane count and/or link rate parameters accordingly. A Connection Manager limits the DisplayPort bandwidth by writing to the DP_REMOTE_CAP.Remote Maximal Link Rate and DP_REMOTE_CAP.Remote Maximal Lane Count

fields of the DP IN Adapter. The use of this register by the DP IN Adapter is defined in Section 10.4.5.

3. **CM_ID** – A Connection Manager sets ADP_DP_CS_2.CM_ID in the DP IN Adapter to the Connection Manager index
4. **DP BW Allocation Mode** – If the Connection Manager supports DP BW Allocation Mode, it does the following:
 - a. Checks if the DP IN Adapter supports DP BW Allocation Mode by reading DP_LOCAL_CAP.DP_IN_BW_Allocation Mode Support.
 - b. If the DP IN Adapter supports DP BW Allocation Mode, the Connection Manager does the following in the DP IN Adapter Configuration Space:
 - i. Sets ADP_DP_CS_2. CM BW Allocation Mode Support to 1b.
 - ii. If the Path being set up between the two Adapters travels through the same USB4 Links as another DP Path, then it sets ADP_DP_CS_2.Group_ID to a non-zero value for all the Paths which travel through the same USB4 Links, otherwise it sets ADP_DP_CS_2.Group_ID to 0h.
 - iii. Sets ADP_DP_CS_2.NRD_Maximal_Link_Rate to the DP_LOCAL_CAP.Maximal_Link_Rate of the DP IN Adapter or DP OUT Adapter (whichever is lower).
 - iv. Sets ADP_DP_CS_2.NRD_Maximal_Lane_Count to the DP_LOCAL_CAP.Maximal_Lane_Count of the DP IN Adapter or DP OUT Adapter (whichever is lower).
 - v. Sets ADP_DP_CS_2.Estimated BW according to Section 10.7.
 - vi. Sets ADP_DP_CS_2.Granularity to any of the valid values.
 - vii. Sets DP_STATUS.Allocated BW to 0h.
 - viii. Sets ADP_DP_CS_2.CM Ack to 0b.

A Connection Manager shall configure the Output HopID to be 8 for the segment of an Aux Path that goes from a USB4 Port to a DP IN or DP OUT Adapter. A Connection Manager shall configure the Output HopID to be 9 for the segment of a Main-Link Path that goes from a USB4 Port to a DP OUT Adapter.

After Path configuration, a Connection Manager enables the DP Adapters at both ends of the Path by setting the VE (Video Enable) and AE (Aux Enable) bits in the ADP_DP_CS_0 registers of the Protocol Adapters to 1b. The Connection Manager needs to use single Write Request to set the VE and AE bits to 1b so that they both are written at the same time.

The Connection Manager shall enable the DP IN Adapter before enabling the DP OUT Adapter.

Table 10-8. 8b/10b DisplayPort Required Bandwidth (Gbps)

Mode	4 Lanes	2 Lanes	1 Lane
HBR3 (8.1 Gbps)	25.92	12.96	6.48
HBR2 (5.4 Gbps)	17.28	8.64	4.32
HBR (2.7 Gbps)	8.64	4.32	2.16
RBR (1.62 Gbps)	5.2	2.6	1.3

Note: Bandwidth = Lane Count * Link Rate * 8/10.

Note: Bandwidth calculation assumes max utilization over the DP Link and does not account for blanking and stuffing symbol removal.

10.4.2.2 Teardown

When the *ADP_DP_CS_0.AE* bit and the *ADP_DP_CS_0.VE* bit are both set to 0, a DP Adapter shall set all the fields in its DP Adapter Configuration Capability to their default values.



CONNECTION MANAGER NOTE

*Before tearing down a Path between two DP Adapters, the Connection Manager shall disable the DP Adapters on both ends of the Path by setting the *ADP_DP_CS_0.VE* (Video Enable) and *ADP_DP_CS_0.AE* (Aux Enable) bits to 0b in register of each DP Adapter. The Connection Manager shall use single Write Request to set the VE and AE bits to 0b so that they both are written at the same time.*

*After tearing down a DP Path, the Connection Manager releases the DP stream resource, using a *DEALLOCATE_DP_RESOURCE* command as defined in Section 8.3.1.1.3, with a *DisplayPort Number* parameter equal to the DP IN Adapter Number being released.*

*If only one DP IN Adapter remains in a *Group_ID*, a Connection Manager sets the DP IN Adapter *Group_ID* to 0h.*

10.4.3 HPD Event Propagation

The DisplayPort Specification defines three kinds of Hot Plug Detect (HPD) events:

- IRQ – The Sink device sends an Interrupt Request to the Source device.
- Unplug – The Sink device is no longer attached to the Source device.
- Plug/Re-plug – The Sink device is newly attached to the Source device.

HPD events are transported across the USB4 Fabric from the DP OUT Adapter to the DP IN Adapter. Plug/Re-plug and Unplug events are transported using HPD Packets. IRQ events are transported using SET_CONFIG Packets.

10.4.3.1 HPD Plug

After a Path is set up between a DP OUT Adapter and a DP IN Adapter per 10.4.2.1, the DP OUT Adapter shall send an HPD Packet with the *P Flag* set to 1b. Upon receiving an HPD Packet with the *P Flag* set to 1b, the DP IN Adapter shall respond with an ACK Packet, execute the DP Adapter Init flow as defined in Section 10.4.5, and then drive HPD signal high on the DisplayPort interface.

After the DP IN Adapter drives HPD high, both DP Adapters shall be ready to handle AUX transactions.

10.4.3.2 HPD Unplug

A DP OUT Adapter detects unplug of a DPRX as defined in the DisplayPort Specification. Upon unplug detection, the DP OUT Adapter shall send an HPD Packet with the *P Flag* set to 0b to the DP IN Adapter. The DP IN Adapter shall respond with an ACK Packet and drive the HPD signal low.

When the HPD signal is low, a DP OUT Adapter shall monitor the HPD signal (as defined by the DisplayPort Specification) to detect a replug. It may also disable its Main-Link transmitters.

When the HPD signal is low, a DP IN Adapter may disable its DP Link receiver.

10.4.3.3 IRQ

A DP OUT Adapter detects an IRQ as defined in the DisplayPort Specification. Upon IRQ detection, a DP OUT Adapter shall send a SET_CONFIG Packet of MSG type IRQ to the DP IN Adapter. However, if Link training is in process or it just ended, a DP OUT Adapter shall wait *tIRQDelay* after it sent a SET_CONFIG Packet to the DP IN Adapter (reporting that Link training is completion) before sending the IRQ SET_CONFIG Packet.

A DP IN Adapter that receives a SET_CONFIG Packet of MSG type IRQ shall respond with an ACK Packet and drive the IRQ event (according to the DisplayPort Specification) towards the DPTX.

10.4.3.4 HPD Delay Requirements

Section 3.6.8.2 of the DisplayPort Specification defines the delay from detection of an HPD unplug or HPD IRQ event by the DP OUT Adapter to the start of the event's generation by the DP IN Adapter on the DisplayPort HPD signal. HPD event detection is defined in Section 5.1.4 of the DisplayPort Specification. Table 10-9 defines the maximum propagation delay through the DP Adapters that shall be used for HPD Events.

Table 10-9. HPD Event Propagation Delay Requirements

	HPD Unplug Max Delay (μs)	HPD IRQ Max Delay (μs)	HPD Plug Max Delay (μs)
DP IN	90	90	300
DP OUT	90	90	90

The propagation delay through the DP OUT Adapter shall be measured from when the event is detected by the DP OUT Adapter to when the last bit of the corresponding packet, SET_CONFIG or HPD, is sent over the AUX Path. The propagation delay does not include the time it takes the Connection Manager to establish the AUX Path.

The propagation delay through the DP IN Adapter shall be measured from when the last bit of an HPD Event Packet, SET_CONFIG or HPD, arrives at the DP IN Adapter to when event is driven on the HPD signal.

A DP OUT Adapter shall send HPD packet with the *P Flag* set to 1b within tDPPlug of transitioning to the Paired state.

10.4.3.5 Manual HPD Control

A Connection Manager uses the *HPDC* and *HPDS* fields to control how a DP IN Adapter drives the DisplayPort HPD signal.

- When HPDC transitions from 0b to 1b, a DP IN Adapter shall drive the DisplayPort HPD signal low.
- When HPDS transitions from 0b to 1b, a DP IN Adapter shall drive the DisplayPort HPD signal high.
- The DisplayPort HPD signal level shall be set according to the most recent event, whether it is HPDS set, HPDC set, IRQ SET_CONFIG Packet or HPD Packet.

Note: If a DP IN Adapter receives an AUX Request before it receives an HPD Packet with a P Flag set to 1b, it may silently discard the AUX Request.



CONNECTION MANAGER NOTE

Router behavior is undefined if a Connection Manager does either of the following:

- *Sets the HPDS bit to 1b before setting up the DP Paths.*
- *Sets the HPDC bit to 1b before tearing down the DP Paths.*

10.4.4 AUX Request and Response Handling

10.4.4.1 LTTPR Non-Transparent Mode

This section defines the AUX Request and Response handling by DP Adapters operating in LTTPR Non-Transparent mode.

With respect to DisplayPort signals, the DP IN and DP OUT Adapters serve as UFP and DFP respectively. However, in terms of AUX Handling, the DP IN Adapter acts as both UFP and DFP. The AUX handling roles for UFP and DFP are defined in Section 3.6.6.3 of the DisplayPort Specification.

During 128b/132b DisplayPort link training, a DP Adapter shall operate in AUX Intra-Hop mode as defined in the DisplayPort Specification. Otherwise, a DP IN Adapter shall operate as defined in Section 10.4.4.1.1 and a DP OUT Adapter shall operate as defined in Section 10.4.4.1.2.

10.4.4.1.1 DP IN Adapter Requirements

Upon reception of a DisplayPort AUX request, a DP IN Adapter shall send an AUX Packet containing the request over the AUX Path. The AUX request coming from the DPTX shall not be modified by the DP IN Adapter.

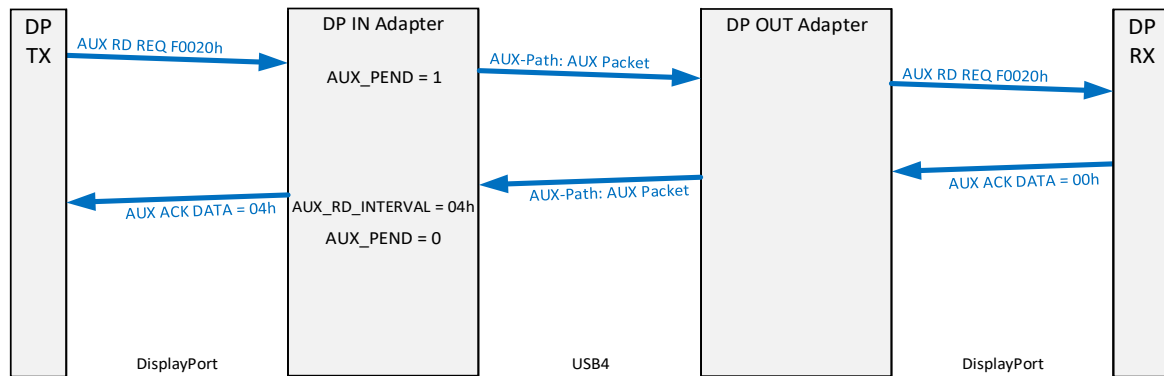
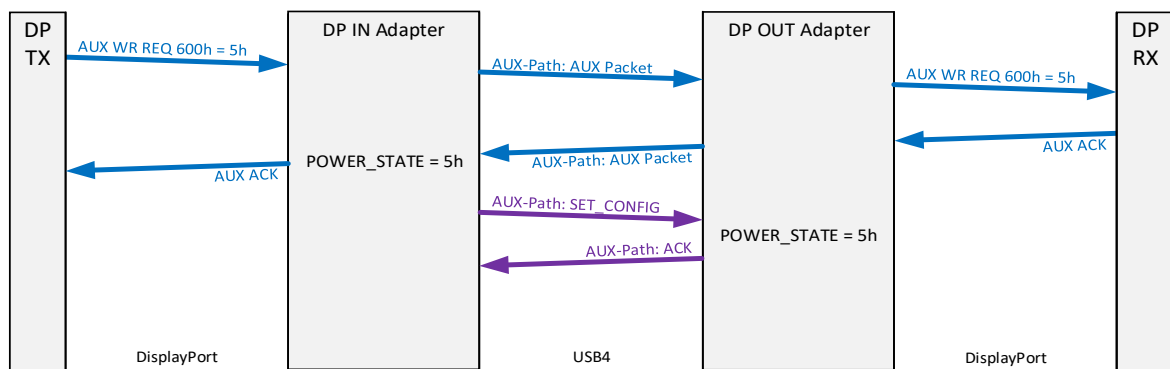
A DP IN Adapter handles three types of AUX transactions:

- Target
 - Includes AUX transactions which target the LTTPR or *LT-tunable PHY Repeater DPCD Capability and ID* field (Table 3-91 in the DisplayPort Specification).
 - Figure 10-14 shows an example of a Target transaction that is an AUX read transaction from DPCD address F0020h (TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1). The transaction becomes a Target transaction because the DP Adapters are Repeater1 in this use case example.
- Snoop
 - Includes AUX transactions which hold valuable information for the LTTPR, but do not target the LTTPR.
 - Figure 10-15 shows an example of a Snoop transaction that is an AUX write transaction to DPCD address 00600h (SET_POWER). The transaction becomes a Snoop transaction because the power state is of interest to the LTTPR. The DP IN Adapter follows with a SET_CONFIG Packet of type SET_POWER.
- Pass-Through
 - Includes AUX transactions which are irrelevant to the LTTPR operation.

For Pass-Through transactions, there is no additional action required by the DP IN Adapter.

For Target transactions, the DP IN Adapter shall set the AUX_PEND flag and take the appropriate action when the request comes back. See Section 3.6.6.3.3 of the DisplayPort Specification for how to set the AUX_PEND flag and what action to take when the request comes back.

When a DP IN Adapter updates the DP OUT Adapter as the result of a Snoop or Target transaction, it shall perform the update only after receiving an AUX Response and before sending the AUX ACK response to the DPTX. This rule applies for all cases except a SET_CONFIG Packet of type SET_VSPE. For a SET_CONFIG Packet of type SET_VSPE, the SET_CONFIG Packet is sent before receiving an AUX Response. Updating the DP OUT Adapter shall be done by sending SET_CONFIG Packets to the DP OUT Adapter.

Figure 10-14. Target AUX Transaction Flow**Figure 10-15. Snoop AUX Transaction Flow****10.4.4.1.2 DP OUT Adapter Requirements**

A DP OUT Adapter shall convert an incoming AUX Packet received from the USB4 Fabric into a DisplayPort AUX request. The content of the request shall not be modified by the DP OUT Adapter.

A DP OUT Adapter shall convert an incoming DisplayPort AUX response into an AUX Packet and send it on the AUX Path. The content of the response shall not be changed by the DP OUT Adapter.

10.4.4.2 Non-LTTPR Mode

This section defines how a DP Adapter, operating in Non-LTTPR mode, handles AUX Requests and Responses. A DP IN Adapter shall implement AUX Replier. A DP OUT Adapter shall implement AUX Requester.

10.4.4.2.1 AUX Timeout Timers

The AUX Response Timeout timer in a DP IN Adapter shall be set to 300 μ s.

The AUX Reply Timeout timer in a DP OUT Adapter shall be set to 400 μ s.

10.4.4.2.2 DP IN Adapter Requirements

A DP IN Adapter that receives an AUX Request shall classify the AUX Transaction as one of the three following types:

1. Internal AUX Transaction – AUX Request which targets only DPCD addresses that are defined as internal in Table 10-10.

2. External AUX Transaction – AUX Request which targets only DPCD addresses that are not defined as internal in Table 10-10.
3. Combined AUX Transaction – AUX Request which targets both Internal and External DPCD addresses. The AUX Response is initially generated by the DPRX and altered by the DP IN Adapter.

Note: A DP IN Adapter may assume that an AUX Write Request is not classified as a Combined Aux Transaction.

Table 10-10. DPCD Internal Addresses

Functionality	Address	Name
Link Training Control	00100h	LINK_BW_SET
	00101h	LANE_COUNT_SET
	00102h ¹	TRAINING_PATTERN_SET
	00103-6h ¹	TRAINING_LANE _x _SET
Link Status ¹	00202h	LANE0_1_STATUS
	00203h	LANE2_3_STATUS
	00204h	LANE_ALIGN_STATUS_UPDATED
	00205h ²	SINK_STATUS
	00206h	ADJUST_REQUEST_LANE0_1
	00207h	ADJUST_REQUEST_LANE2_3
	0200Ch	LANE0_1_STATUS_ESI
	0200Dh	LANE2_3_STATUS_ESI
	0200Eh	LANE_ALIGN_STATUS_UPDATED_ESI
	0200Fh ²	SINK_STATUS_ESI
Link Quality Control	0010Bh	LINK_QUAL_LANE0_SET
	0010Ch	LINK_QUAL_LANE1_SET
	0010Dh	LINK_QUAL_LANE2_SET
	0010Eh	LINK_QUAL_LANE3_SET
	0010Fh	LINK_SQUARE_PATTERN_num_+_1
DP Tunneling over USB4	E0000h – E00FFh	DP Tunneling over USB4 field DPCDs
Notes: 1. Link Status DPCD registers, TRAINING_PATTERN_SET, and TRAINING_LANE _x _SET are Internal only during Link Training phase. Link Training phase starts when DPTX writes TRAINING_PATTERN_SELECT to a non-zero value and ends when it writes zero to TRAINING_PATTERN_SELECT. 2. When a DPTX reads addresses 00205h and 0200Fh during link training, a DP IN Adapter shall respond with value of 0h.		

For Internal AUX Transactions, a DP IN Adapter shall not send the AUX Request downstream and shall self-generate the AUX Response.

For External and Combined AUX Transactions, a DP IN Adapter shall send the AUX Request downstream to the DP OUT Adapter. If the AUX Response does not arrive on time, the DP IN Adapter shall generate an AUX DEFER before the AUX Response timer expires. Response timer expiration is defined in the DisplayPort Specification.

When a DP IN Adapter updates the DP OUT Adapter as the result of an External or Combined transaction, it shall perform the update only after receiving an AUX Response and before sending the AUX ACK response to the DPTX. This rule applies for all cases except when receiving the first

AUX Request to the *LT-tunable PHY Repeater DPCD Capability and ID* field. Upon reception of the first AUX Request to the *LT-tunable PHY Repeater DPCD Capability and ID* field, the DP IN Adapter sends a SET_CONFIG Packet of type SET_LTTTPR_MODE without waiting for an AUX Response. The update shall be done by sending SET_CONFIG Packets to the DP OUT Adapter.

A DP IN Adapter shall not send an AUX Request to a DP OUT Adapter while the AUX Reply to the preceding AUX Request is outstanding.

DP IN Adapter shall increment AUX_REQ_CNTR by 1 on every received AUX request from DPTX and shall reset to zero on transition to IDLE state.

Figure 10-16 shows the Non-LTTTPR DP IN Adapter AUX handling state machine.

Figure 10-16. DP IN Adapter AUX Handling State Machine

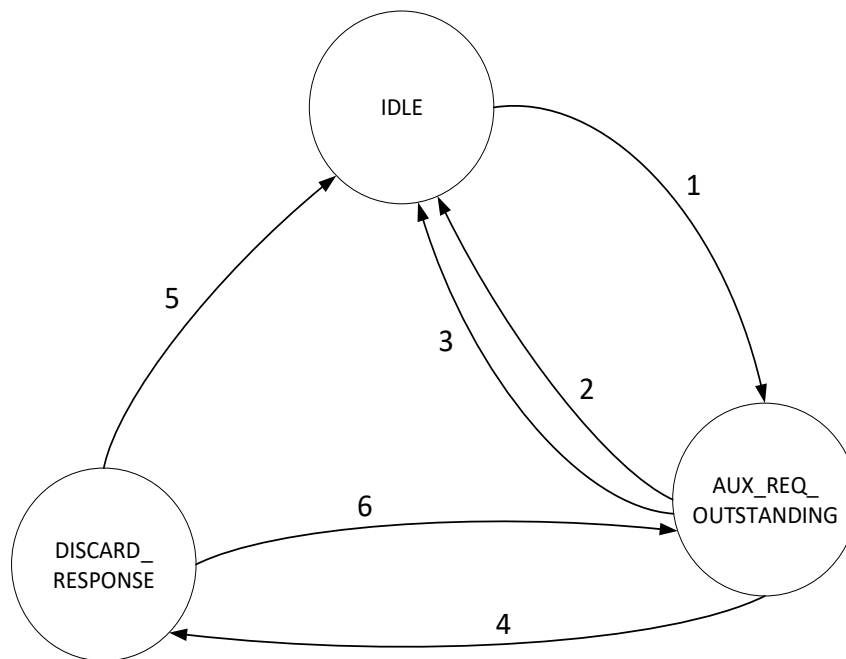


Table 10-11. DP IN Adapter AUX Handling State Machine

Number	Current State	Next State	Condition	Action
1	IDLE	AUX_REQ_OUTSTANDING	DP IN Adapter received an AUX Request.	If AUX Request is for an Internal AUX Transaction, DP IN Adapter shall process Request. If AUX Request is not for an Internal AUX Transaction, DP IN Adapter send Request downstream.
2	AUX_REQ_OUTSTANDING	IDLE	DP IN Adapter has an AUX Response available and DP IN Adapter is in Talk Mode as defined in the DisplayPort Specification.	DP IN Adapter shall send the AUX Response and reset AUX_REQ_CNTR to zero.

Number	Current State	Next State	Condition	Action
3	AUX_REQ_OUTSTANDING	IDLE	DP IN Adapter received SET_CONFIG (SET_AUX_INIT) or AUX_REQ_CNTR > 2 while DP IN Adapter either does not have an AUX Response available or is not in Talk Mode as defined in the DisplayPort Specification.	DP IN Adapter shall reset AUX_REQ_CNTR to zero.
4	AUX_REQ_OUTSTANDING	DISCARD_RESPONSE	DP IN Adapter received an AUX Request that is different than the pending AUX Request and AUX_REQ_CNT < 3.	None.
5	DISCARD_RESPONSE	IDLE	DP IN Adapter received SET_CONFIG(SET_AUX_INIT) or AUX_REQ_CNTR > 2.	DP IN Adapter shall reset AUX_REQ_CNTR to zero.
6	DISCARD_RESPONSE	AUX_REQ_OUTSTANDING	DP IN Adapter has an AUX Response available.	DP IN Adapter shall discard the AUX Response, set AUX_REQ_CNTR to 1, and send the AUX Request.

10.4.4.2.3 DP OUT Adapter Requirements

A DP OUT Adapter handles two types of AUX Transactions:

- DPTX initiated.
- DP OUT Adapter initiated.

A DPTX initiated AUX Request has higher priority than a DP OUT Adapter initiated AUX Transaction.

A DP OUT Adapter that receives a DPTX initiated AUX Request while handling a DP OUT Adapter Initiated AUX Transaction, shall send the DPTX initiated AUX Request as soon as it is in Talk Mode.

10.4.4.2.3.1 DP TX Initiated AUX Transactions

A DP OUT Adapter that receives an AUX Request from a DP IN Adapter shall initiate the AUX Request as soon as it is in Talk Mode.

A DP OUT Adapter that receives an AUX Response shall send the AUX Response over the AUX Path to the DP IN Adapter.

If the AUX Reply Timer expires before an AUX Response is received, a DP OUT Adapter shall send a SET_CONFIG of type SET_AUX_INIT and shall not retry the AUX Request.

10.4.4.2.3.2 DP OUT Adapter Initiated AUX Transactions

A DP OUT Adapter initiates AUX Transactions for:

- Autonomous, concurrent Link Training.
- Down-Spread Control access, see Section 10.4.7.

10.4.4.3 LTPR Transparent Mode

This section defines how a DP Adapter, operating in LTPR Transparent mode handles AUX Requests and Responses. A DP IN Adapter shall implement AUX Replier. A DP OUT Adapter shall implement AUX Requester.

10.4.4.3.1 AUX Timeout Timers

The AUX Response Timeout timer in a DP IN Adapter shall be set to 300 μ s when the AUX Transaction is an Internal AUX Transaction. For an External and Combined AUX Transactions, the AUX Response Timeout timer in a DP IN Adapter shall not be activated.

The AUX Reply Timeout timer in a DP OUT Adapter shall be set to 3.2 ms.

10.4.4.3.2 DP IN Adapter Requirements

A DP IN Adapter that receives an AUX Request shall classify the AUX Transaction as one of the following types:

- Internal AUX Transaction – AUX Request which targets only DPCD addresses that are defined as internal in Table 10-10.
- External AUX Transaction – AUX Request which targets only DPCD addresses that are not defined as internal in Table 10-10.
- Combined AUX Transaction – AUX Request which targets both Internal and External DPCD addresses. The AUX Response is initially generated by the DPRX and altered by the DP IN Adapter.

Note: A DP IN Adapter may assume that an AUX Write Request is not classified as a Combined Aux Transaction.

For External and Combined AUX Transactions, a DP IN Adapter shall send the AUX Request downstream to the DP OUT Adapter.

When a DP IN Adapter updates the DP OUT Adapter as the result of an External or Combined transaction, it shall perform the update only after receiving an AUX Response and before sending the AUX ACK response to the DPTX. The update shall be done by sending SET_CONFIG Packets to the DP OUT Adapter.

A DP IN Adapter shall not:

- Generate AUX DEFER, unless it is an Internal AUX Transaction.
- Gate any External or Combined AUX Request sent by the DPTX.
- Gate any AUX Response sent by the DPRX.

Note: DPTX enabling LTPR Transparent mode shall support AUX Reply Timeout of 3.2 ms as described in the DisplayPort Specification. Once DPTX enables LTPR Transparent mode, it is the responsibility of DPTX to manage the AUX Requests and AUX Responses, not DP IN Adapter.

10.4.4.3.3 DP OUT Adapter Requirements

A DP OUT Adapter handles two types of AUX Transactions:

- DPTX initiated.
- DP OUT Adapter initiated.

A DPTX initiated AUX Request has higher priority than a DP OUT Adapter initiated AUX Transaction.

A DP OUT Adapter that receives a DPTX initiated AUX Request while handling a DP OUT Adapter Initiated AUX Transaction, shall send the DPTX initiated AUX Request as soon as it is in Talk Mode.

10.4.4.3.3.1 DPTX Initiated AUX Transactions

A DP OUT Adapter that receives an AUX Request from a DP IN Adapter shall initiate the AUX Request as soon as it is in Talk Mode.

A DP OUT Adapter that receives an AUX Response shall send the AUX Response over the AUX Path to the DP IN Adapter.

If the AUX Reply Timer expires before an AUX Response is received, a DP OUT Adapter shall send a SET_CONFIG of type SET_AUX_INIT and shall not retry the AUX Request.

10.4.4.3.3.2 DP OUT Adapter Initiated AUX Transactions

A DP OUT Adapter initiates AUX Transactions for:

- Autonomous, concurrent Link Training.
- Down-Spread Control access, see Section 10.4.7.

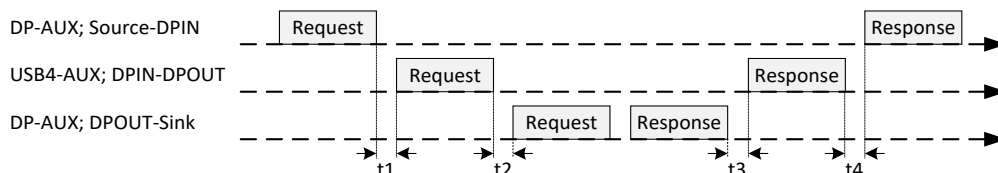
10.4.4.4 AUX Delay Requirements

Table 10-12 defines the maximum delay allowed for a DP Adapter, per direction of a transaction. Figure 10-17 correlates the delay requirements to an AUX transaction sequence. The DP-to-USB4 Fabric delay shall be measured from the time the last bit arrives at the DP Adapter from the DisplayPort interface to the time when the first bit is sent to the USB4 Fabric. USB4 Fabric-to-DP delay shall be measured from the time when the last bit of the AUX Packet arrives at the DP Adapter to the time when the first bit is sent to the DisplayPort Interface, assuming the DP Adapter is in Talk Mode.

Table 10-12. AUX Delay Requirements

Direction of Transport	Max Delay (μ s)
DP IN: DP to USB4 Fabric (t_1)	tDPAUXDelayIn
DP OUT: USB4 Fabric to DP (t_2)	tDPAUXDelayOut
DP OUT: DP to USB4 Fabric (t_3)	tDPAUXDelayOut
DP IN: USB4 Fabric to DP (t_4)	tDPAUXDelayIn

Figure 10-17. AUX Timing



10.4.4.5 Aggregated DisplayPort Capabilities

A DP IN Adapter shall update its DP_LOCAL_CAP and DP_COMMON_CAP registers if it receives an AUX Read Response that has lower parameter values than the registers currently contain. Before transmitting the AUX Read Response, the DP IN Adapter shall update the AUX Read Response to reflect the aggregated DisplayPort Capabilities as shown in Table 10-13.

Table 10-13. Aggregated DisplayPort Capabilities

DPCD Register (Address)	DPCD Field Name	DisplayPort Capability
DPCD_REV (0000h / 02200h)	Major Revision Number	max{12h, min [Downstream response, DP_COMMON_CAP.Maximal DPCD Rev.]}
MAX_LINK_RATE (00001h / 02201h)	MAX_LINK_RATE	Minimum of downstream response and DP_COMMON_CAP.8b10b Maximal Link Rate.
MAX_LANE_COUNT (00002h / 02202h / F0004h)	MAX_LANE_COUNT	Minimum of downstream response and DP_COMMON_CAP.Maximal Lane Count. If MFDP Mode is set, then Maximum is 2.
	POST_LT_ADJ_REQ_SUPPORTED	If in LTTPR Non-Transparent mode, this field is unchanged. Else set to zero.
	TPS3_SUPPORTED	Downstream response bit AND DP_COMMON_CAP.8b10b TPS3 Capability bit.
DP_TUNNELING_MAX_LINK_RATE (E0028h)	DP_TUNNELING_MAX_LINK_RATE	If DP BW Allocation Mode was enabled, set to Minimum of: <ul style="list-style-type: none"> Maximum of DPRX response for MAX_LINK_RATE And ADP_DP_CS_2.NRD_Maximal_Link_Rate Else set to 0h.
DP_TUNNELING_MAX_LANE_COUNT (E0029h)	DP_TUNNELING_MAX_LANE_COUNT	If DP BW Allocation Mode was enabled, set to Minimum of: <ul style="list-style-type: none"> Maximum of DPRX response for MAX_LANE_COUNT And ADP_DP_CS_2.NRD_Maximal_Lane_Count Else set to 0h.
MAX_DOWNSPREAD (00003h / 02203h)	NO_AUX_TRANSACTION_LINK_TRAINING	Set to zero.
	TPS4_SUPPORTED	Downstream response bit AND DP_COMMON_CAP.8b10b TPS4 Capability bit.
TRAINING_AUX_RD_INTERVAL (0000Eh / 0220Eh)	TRAINING_AUX_RD_INTERVAL	If in LTTPR Non-Transparent mode, this field is unchanged. Else, the downstream response is either unchanged or the DP IN Adapter may increase the value. Note that per the DisplayPort Specification, the maximum value for this field is 4h.
MSTM_CAP (00021h)	MST_CAP	Downstream response bit AND DP_COMMON_CAP.8b10b MST Capability bit.
DSC_SUPPORT (00060h)	DSC Support	Downstream response bit AND NOT(DP_COMMON_CAP.DSC Not Supported bit).
FEC_CAPABILITY (00090h)	FEC_CAPABLE	Downstream response bit AND NOT(DP_COMMON_CAP.8b10b FEC Not Supported bit).
DPRX_FEATURE_ENUMERATION_LIST (02210h)	GTC_CAP	Set to zero.
	SST_SPLIT_SDP_CAP	Downstream response bit AND DP_COMMON_CAP.Secondary Split Capability bit.

DPCD Register (Address)	DPCD Field Name	DisplayPort Capability
PHY_REPEATER_CNT (F0002h)	PHY_REPEATER_CNT	If DP_COMMON_CAP.LTTPR Not Supported is set to 1 then set to zero. If DP_COMMON_CAP.LTTPR Not Supported is set to 0 then respond as an LTTPR according to the DisplayPort Specification.
MAIN_LINK_CHANNEL_CODING_CAP (00006h/02206h)	128b/132b_SUPPORTED	Set to 0b
128b/132b_SUPPORTED_LINK_RATES (02215h)	10Gbps/Lane Support	Set to 0b
	20Gbps/Lane Support	Set to 0b
	13.5Gbps/Lane Support	Set to 0b
DP_TUNNELING_MAIN_LINK_CHANNEL_CODING (E002Bh)	128b/132b SUPPORTED	DPRX response for 128b/132b_SUPPORTED bit (DPCD 00006h/02206h) AND DP_COMMON_CAP.128b/132b Link Layer & 10Gbps/Lane Support bit.
DP_TUNNELING_128b/132b_LINK_RATE (E002Ch)	10Gbps/Lane Support	DPRX response for 10Gbps/Lane Support bit (DPCD 02215h) AND DP_COMMON_CAP.128b/132b Link Layer & 10Gbps/Lane Support bit.
	20Gbps/Lane Support	DPRX response for 20Gbps/Lane Support bit (DPCD 02215h) AND DP_COMMON_CAP.20Gbps/Lane Support bit.
	13.5Gbps/Lane Support	DPRX response for 13.5Gbps/Lane Support bit (DPCD 02215h) AND DP_COMMON_CAP.13.5Gbps/Lane Support bit.
MAIN_LINK_CHANNEL_CODING_PHY_REPEATER (F0006h)	128b/132b SUPPORTED	If DP Adapters are the nearest LTTPR to the DPRX then set to DP_COMMON_CAP.128b/132b Link Layer & 10Gbps/Lane Support bit. Else Downstream response bit AND DP_COMMON_CAP.10Gbps/Lane Support bit.
PHY_REPEATER_128b/132b_RATES (F0007h)	10Gbps/Lane Support	If DP Adapters are the nearest LTTPR to the DPRX then set to DP_COMMON_CAP.128b/132b Link Layer & 10Gbps/Lane Support bit. Else Downstream response bit AND DP_COMMON_CAP.128b/132b Link Layer & 10Gbps/Lane Support bit.
	20Gbps/Lane Support	If DP Adapters are the nearest LTTPR to the DPRX then set to DP_COMMON_CAP.20Gbps/Lane Support bit. Else Downstream response bit AND DP_COMMON_CAP.20Gbps/Lane Support bit
	13.5Gbps/Lane Support	If DP Adapters are the nearest LTTPR to the DPRX then set to DP_COMMON_CAP.13.5Gbps/Lane Support bit. Else Downstream response bit AND DP_COMMON_CAP.13.5Gbps/Lane Support bit.
DP_TUNNELING_CAPABILITIES (E000Dh)	Panel Replay Tunneling Optimization Support	DP_COMMON_CAP.Panel Replay Tunneling Optimization Support.
LT_TUNABLE_PHY_REPEATER_FIELD_DATA_STRUCTURE_REV (F0000h)	Revision Number	If DP_COMMON_CAP.Protocol Adapter Version equals 5h: If DP Adapters are the nearest LTTPR to the DPRX then set to 20h else set to Min{20h, Downstream response}. Else set to 14h.
LTTPR_ADVANCED_LINK_POWER_MANAGEMENT_CAPABILITIES (F0009h)	AUX-LESS ALPM_CAP	If the DP Adapters are the nearest LTTPR to the DPRX then set to DP_COMMON_CAP.ALPM Support bit. Else set to Downstream response bit AND DP_COMMON_CAP.ALPM Support bit.

10.4.4.6 DPCD DP Tunneling over USB4

When a DP IN Adapter receives an AUX Request targeting the DP Tunneling over USB4 field DPCDs, it shall respond with its internal data.

A DP IN Adapter shall set the *DP Tunneling Support* bit to 1b in the DP_TUNNELING_CAPABILITIES DPCD (Address E00Dh bit offset 0).

10.4.5 DP Adapters Init Flow

A DP IN Adapter in the Paired state shall do the following after receiving a first HPD Packet with the *P flag* set to 1b:

- Update MFDP Mode inner variable according to Section 10.4.5.1.
- Send a SET_CONFIG Packet of type SET_AUX_INIT.
- If the DP_COMMON_CAP.*Protocol Adapter Version* field equals 5, complete the DP Cable Discovery handshake as defined in Section 10.4.5.2.1.

The DP IN Adapter shall not drive HPD high on the DisplayPort Interface until after it performs the steps above.

10.4.5.1 Multi-Function DP

If any of the DisplayPort connections are Multi-Function (as defined in the DisplayPort Alt Mode Specification), a DP IN Adapter sets an internal MFDP Mode flag to 1b. Otherwise the internal MFDP Mode flag is set to 0b. Section 10.4.4.5 describes how the MFDP Mode flag is used.

If a DP IN Adapter is not connected as part of a Multi-Function (as defined in the DisplayPort Alt Mode Specification), it shall send a SET_CONFIG Packet of type SET_MFDP with the *MFDP Enable* bit set to 0b. Otherwise it may send a SET_CONFIG Packet of type SET_MFDP with the *MFDP Enable* bit set to 1b.

A DP OUT Adapter which receives a SET_CONFIG Packet of type SET_MFDP shall respond with a SET_CONFIG Packet of type SET_MFDP within tDPInit. If the DP OUT Adapter is connected as part of Multi-Function as defined in the DisplayPort Specification, then the *MFDP Enable* bit shall be set to 1b, otherwise it shall be set to 0b.

10.4.5.2 DP Cable Discovery

10.4.5.2.1 DP Cable Discovery Handshake

The DP cable discovery handshake consist of the following sequence:

1. A DP IN Adapter shall send a SET_CONFIG Packet of type CABLE_DISCOVERY to the DP OUT Adapter. The *Cable Type* field in the SET_CONFIG Packet is set to 0h.
2. A DP OUT Adapter that receives a SET_CONFIG Packet of type CABLE_DISCOVERY shall respond with a SET_CONFIG Packet of type CABLE_DISCOVERY. The *Cable Type* field in the SET_CONFIG Packet shall indicate which type of DP cable the DP OUT Adapter discovered on its connector. The *UHBR10_20_Support* and *UHBR13.5_Support* fields in the SET_CONFIG Packet shall indicate the UHBR support the DP OUT Adapter discovered on its connector. The DP OUT Adapter shall send the SET_CONFIG Packet within tDPInit after receiving the SET CONFIG Packet from the DP IN Adapter.
3. After receiving the SET_CONFIG Packet of type CABLE_DISCOVERY from the DP OUT Adapter, the DP IN Adapter shall save the *Cable Type* field as DP OUT Adapter Cable Type.

10.4.5.2.2 DP Cable Discovery AUX Handling

As part of the DP Cable Discovery, a DPTX reads the DPCD CABLE_ATTRIBUTES_UPDATED_BY_DPRX register (address 02217h) and then writes to the DPCD CABLE_ATTRIBUTES_UPDATED_BY_DPTX register (address 00110h).

When the DPTX reads from DPCD address 02217h, a DP IN Adapter shall do the following:

- Save the AUX Response *Cable Type* field as the DPRX Cable Type.
- Set the *Cable Type* field in the AUX Response to the same cable type that the DP IN Adapter discovered on its connector.
- Set the *UHBR10_20 Capability* field in the AUX Response to the highest common capability between the AUX Response *UHBR10_20 Capability* field it received from DPRX and the *UHBR10_20 Capability* that the DP IN Adapter discovered on its connector.
- Set the *UHBR13.5 Capability* bit in the AUX Response to the logical AND between the AUX Response *UHBR13.5 Capability* bit it received from DPRX and the *UHBR13.5 Capability* that the DP IN Adapter discovered on its connector.

When the DPTX writes to DPCD address 00110h, a DP IN Adapter shall do the following:

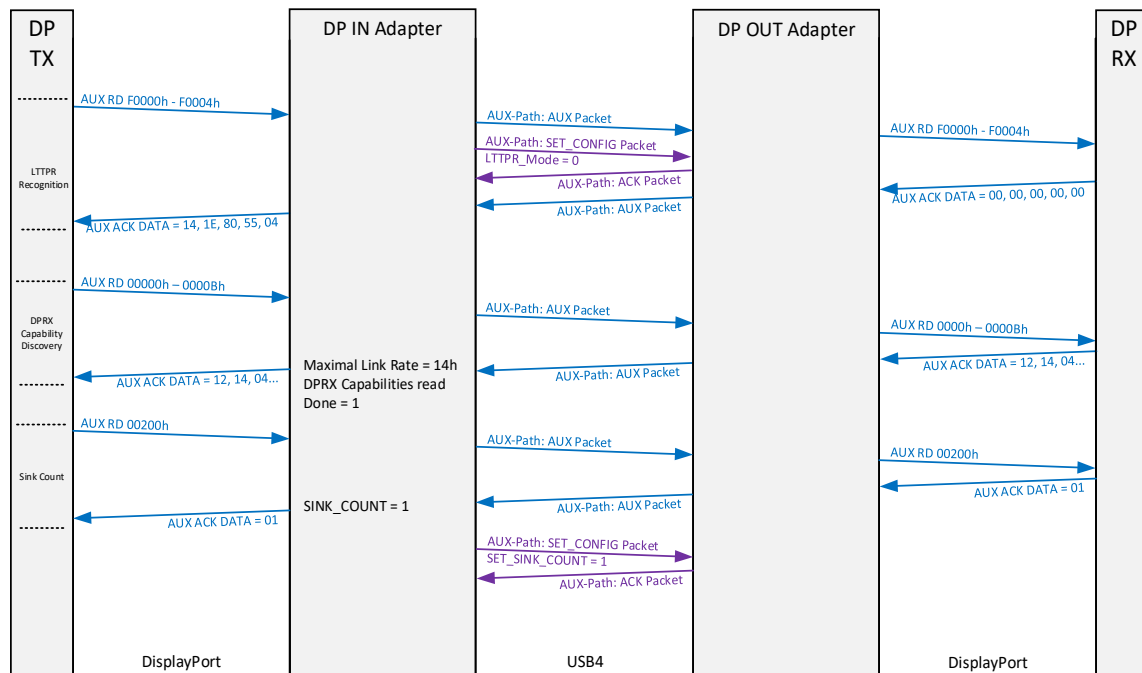
- Save the *Cable Type* field in the AUX Request as the DPTX Cable Type.
- Set the *Cable Type* field in the AUX Request according to the following rules:
 - If the saved DPRX Cable Type is not 000b (unknown cable type), then set the *Cable Type* field to the saved DPRX Cable Type.
 - Else, if the DP IN Adapter received a SET_CONFIG Packet of type CABLE_DISCOVERY, then set the *Cable Type* field to the saved DP OUT Adapter Cable Type.
 - Else, set the *Cable Type* field to 000b.

When DPTX reads from DPCD address 00110h, a DP IN shall set the *Cable Type* field in the AUX Response to the saved DPTX Cable Type.

10.4.6 Source Discovery

According to the DisplayPort Specification, upon HPD Plug detection the DPTX executes the following steps:

- LTTPR recognition.
- DPRX Capabilities read.
- Sink Count read.

Figure 10-18. Example DP Source Discovery Sequence**10.4.6.1 LTPR Recognition and Modes Change**

A DPTX performs an AUX read from the *LT-tunable PHY Repeater DPCD Capability and ID* field to discover the presence, count and capabilities of any downstream LTPR. A DP IN Adapter shall modify the resulting AUX read response as defined in Section 10.4.4.5.

This action of AUX read from LT-tunable PHY Repeater DPCD registers by DPTX prompts DP Adapter to transition from Non-LTPR mode to LTPR mode. Upon transition to LTPR mode, DP Adapter is in LTPR Transparent mode by default. DPTX may prompt the transition to LTPR Non-Transparent mode and back to LTPR Transparent mode by setting PHY_REPEATER_MODE register at DPCD F0003h, 55h for LTPR Transparent mode and AAh for LTPR Non-Transparent mode.

If DP_COMMON_CAP.LTPR Not Supported is set to 1b, a DP Adapter shall operate only in Non-LTPR mode. Otherwise it transitions between the three operation modes according to Table 10-14.

Table 10-14. DP Adapter Operation Mode Transitions

Mode	DP IN Adapter	DP OUT Adapter
Non-LTPR	Adapter has exited the Paired State	Adapter has exited the Paired State or Adapter received a SET CONFIG Packet of type SET_AUX_INIT
LTPR Transparent	Adapter receives first AUX Request to the <i>LT-tunable PHY Repeater DPCD Capability and ID</i> field or Adapter receives an AUX ACK for the change of the PHY_REPEATER_MODE to Transparent mode (55h)	Adapter received a SET CONFIG Packet of type SET_LTPR_MODE with LTPR_Mode set to 0b
LTPR Non-Transparent	Adapter receives an AUX ACK for the change of the PHY_REPEATER_MODE to Non-Transparent mode (AAh)	Adapter received a SET CONFIG Packet of type SET_LTPR_MODE with LTPR_Mode set to 1b

When a DP IN Adapter is operating in Non-LTTPR mode and it receives the first AUX Request to the *LT-tunable PHY Repeater DPCD Capability and ID* field, it shall:

1. Transition to LTTPR Transparent mode.
2. Send a SET CONFIG Packet of type SET_LTTPR_MODE with LTTPR_Mode set to 0b.
3. Complete the AUX Transaction operating in LTTPR Transparent mode.

A DP IN Adapter shall do the following before transitioning from LTTPR Non-Transparent mode to LTTPR Transparent mode:

- Complete the AUX Transaction according to the current operation mode.
- Send a SET CONFIG Packet of type SET_LTTPR_MODE with LTTPR_Mode set to 0b.

A DP IN Adapter shall do the following before transitioning from LTTPR Transparent mode to LTTPR Non-Transparent mode:

- Complete the AUX Transaction according to the current operation mode.
- Send a SET CONFIG Packet of type SET_LTTPR_MODE with LTTPR_Mode set to 1b.

When DPCD address F0002h is read by a DPTX, a DP IN Adapter shall determine and save the number of LTTPRs located downstream. For example, if the *PHY_REPEATER_CNT* field in the AUX Response is 20h (before it changes it to 10h) then the number of downstream LTTPRs saved by the DP IN Adapter is 3.

If the *DP_COMMON_CAP.Protocol Adapter Version* equals 5, a DP IN Adapter shall follow the rules below when setting the *Downstream LTTPRs* field and *Downstream_LTTPRs_Valid* bit in a SET_CONFIG Packet of type SET_LTTPR_MODE:

- If DPTX has read F0002h since HPD was asserted, then set the *Downstream LTTPRs* field to the saved downstream LTTPRs value and set the *Downstream_LTTPRs_Valid* bit to 1b.
- Else, set the *Downstream LTTPRs* field to 0h and the *Downstream_LTTPRs_Valid* bit to 0b.

10.4.6.2 DPRX Capabilities Read

The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall:

1. Snoop the read response and record the values of the *DPCD_REV*, *MAX_LINK_RATE*, *MAX_LANE_COUNT*, *TPS3_SUPPORTED* and *TPS4_SUPPORTED* fields located at DPCD addresses 00000h/02200h, 00001h/02201h, 00002h/02202h and 00003h/02203h respectively.
2. Update the *Maximal DPCD Rev*, *Maximal Link Rate*, *Maximal Lane Count*, *8b10b TPS3 Capability* and *8b10b TPS4 Capability* fields in the DP_LOCAL_CAP and DP_COMMON_CAP registers to reflect the lowest common capabilities between the existing values of those registers and the recorded values from step 1.
3. Send a SET_CONFIG Packet of type SET_CMN_DPRX with MSG Data equal to the snooped DPCD_REV which reflects the DPRX DPCD_REV.
4. Set the *DPRX Capabilities Read Done* field in the DP_COMMON_CAP register to 1b. Note that this field is set to 1b regardless of whether or not the values in the *Maximal Link Rate* and *Maximal Lane Count* fields in Step 2 were changed.

Note: A DP IN Adapter may delay the setting of the *DPRX Capabilities Read Done* bit to 1b, in order to integrate the additional information read by the DPTX from the *Extended Receiver Capability* region. The *Extended Receiver Capability* region is located at DPCD addresses 02200h-02203h.

This process enables the Connection Manager to know when to read the modified capabilities and recalculate the maximal Bandwidth that may be consumed by this DP Link.

10.4.6.3 Sink Count Read

When DPCD addresses 00200h or 02002h are read by the DPTX, a DP IN Adapter shall snoop the read response and record the value of the `SINK_COUNT`. When the recorded `SINK_COUNT` value is zero, the DP IN Adapter shall send a `SET_CONFIG` Packet of type `SET_SINK_COUNT`, reflecting the recorded value.

When a DP OUT Adapter receives a `SET_CONFIG` Packet of type `SET_SINK_COUNT` with the `SINK_COUNT` value equal to zero, the DP OUT Adapter shall:

- Report an Unplug event as defined in Section 10.3.3.
- Set the `ADP_DP_CS_2.HPD Status` to 0b in the *DP OUT Adapter Configuration Capability* field.

While a DP OUT Adapter is Unplugged and has the `ADP_DP_CS_2.HPD Status` set to 0b in the *DP OUT Adapter Configuration Capability* field, it shall do the following upon IRQ detection:

- Report a Plug event as defined in Section 10.3.3.
- Set the `ADP_DP_CS_2.HPD Status` to 1b in the *DP OUT Adapter Configuration Capability* field.

10.4.7 Down-Spread Control

A DP OUT Adapter that receives a `SET_CONFIG` Packet of type `SET_DOWNSPREAD` shall initiate an AUX write request to DPCD address 00107h with the value received in the `MSG Data` of the `SET_CONFIG` Packet.

10.4.8 Stream Mode Set

If the DPTX writes to DPCD address 00111h, a DP IN Adapter shall snoop the write request and record the value of the `MST_EN` bit. A DP IN Adapter shall send a `SET_CONFIG` Packet of type `SET_STREAM_MODE`, reflecting the recorded value of the `MST_EN` bit when a new recorded `MST_EN` value is different than the previous value.

The `MST_EN` default value at the DP Adapters shall be as defined in the DisplayPort Specification.

A DP OUT Adapter that receives a `SET_CONFIG` Packet of type `SET_STREAM_MODE` shall respond with a `SET_CONFIG` Packet of type `SET_STREAM_MODE`, to signify the acknowledgment of the mode change. The value of the *MSG Data* field in the return packet has no meaning and shall be ignored by the DP IN Adapter.

10.4.9 DSC and FEC Enable

DSC capability discover, configuration and enabling flows are carried over AUX transaction, which are Pass-Through transactions for the DP Adapters. Handling the control DSC symbol is described in Section 10.5.1.1.

If the DPTX writes to DPCD address 00120h, a DP IN Adapter shall snoop the write request and record the values of the `FEC_READY`, `FEC_ERROR_COUNT_SEL`, and `LANE_SELECT` fields. A DP IN Adapter shall send a `SET_CONFIG` Packet of type `SET_FEC_READY`, reflecting the recorded value of the `FEC_READY` bit when a new recorded `FEC_READY` value is different than the previous value.

The `FEC_READY` default value at the DP Adapters shall be as defined in the DisplayPort Specification.

A DP OUT Adapter that receives a `SET_CONFIG` Packet of type `SET_FEC_READY` shall respond with a `SET_CONFIG` Packet of type `SET_FEC_READY` within `tDPInit`, to signify the acknowledgment of the mode change. The value of the *MSG Data* field in the return packet has no meaning and shall be ignored by the DP IN Adapter.

FEC can be enabled or disabled by the DPTX using FEC_DECODE_EN and FEC_DECODE_DIS symbol sequences as defined in Section 10.5.4.

10.4.10 DP Link Training

10.4.10.1 8b/10b LTTTPR Non-Transparent

The DP IN and DP OUT Adapters shall follow the LTTTPR Non-Transparent link training as defined in the DisplayPort Specification while noting the following points:

- DP IN as UFP and DFP – As described in Section 10.4.4, the DP IN Adapter serves as UFP and DFP for AUX handling, therefore it updates the DP OUT Adapter with the different stages of the LTTTPR Non-Transparent link training through SET_CONFIG Packets.
- Training Patterns – Training Patterns are not carried over the USB4 Fabric.

10.4.10.1.1 DP IN Adapter Requirements

- A DP IN Adapter acts as the UFP of LTTTPR and trains its LTTTPR receiver as defined in the DisplayPort Specification.
- When a DP Source trains the downstream DP Links, it alternates between all possible training patterns, including TPS1. Therefore, after DP Link training is finished on the UFP, a DP IN Adapter shall maintain symbol lock and lane alignment in its receiver while DPTX trains the rest of downstream DP Links.
- A DP IN Adapter shall send a SET_CONFIG Packet of type 8B10B_SET_LINK after DPTX writes TPS1 to the DP IN Adapter TRAINING_PATTERN_SET_PHY_REPEATERx DPCD register. The SET_CONFIG packet shall have the following values:
 - LC = LANE_COUNT_SET value written by DPTX.
 - LR = LINK_BW_SET value written by the DPTX.
 - MSG Data = 1b, representing DP Link Training Mode = LTTTPR Non-Transparent.
- A DP IN Adapter shall send a SET_CONFIG Packet of type SET_TRAINING with TS = 0xFF after DPTX writes 0x0 to the DP IN Adapter TRAINING_PATTERN_SET_PHY_REPEATERx DPCD register.
- When a DP IN Adapter receives the AUX ACK for the DPCD AUX Write of 0x0 to the DPRX TRAINING_PATTERN_SET DPCD register, it shall first send a SET_CONFIG Packet of type SET_TRAINING with TS = 0x0 and then send the AUX ACK to the DPTX.
- After DP Link training is finished on the UFP, a DP IN Adapter shall detect a Training pattern on its receiver. After detecting the Training pattern, the DP IN Adapter shall send a single corresponding SET_CONFIG Packet of type SET_TRAINING for every change in Training pattern. The TS field shall be equal to the detected Training pattern as defined in Table 10-6.
- A DP IN Adapter shall send SET_CONFIG Packet of Type SET_VSPE when DPTX writes the TRAINING_LANE0_SET or TRAINING_LANE0_SET_PHY_REPEATERx DPCD register of the next downstream receiver. The MSG Data field shall carry the value in the write request. The SET_VSPE SET_CONFIG Packet shall be sent by the DP IN Adapter before sending the AUX Request Packet.
- A DP Adapter shall have higher priority generating and parsing SET_CONFIG packets over AUX Transaction.
- A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true:
 - The DP IN Adapter internal status indicates that link training has ended successfully.
 - The DP IN Adapter sent at least nine DP Clock Sync Packets after it sent the SET_CONFIG Packet of type 8B10B_SET_LINK.

10.4.10.1.2 DP OUT Adapter Requirements

- A DP OUT Adapter that receives a SET_CONFIG Packet of Type 8B10B_SET_LINK with the *DP Link Training Mode* bit set to 1b shall start its internal Symbol clock PLL according to the *Link Rate* field, and start the Lifetime Counter as defined in Section 10.6.1.2.
- A DP OUT Adapter that receives a SET_CONFIG Packet of Type SET_TRAINING with the *TS* field equal to 1, 2, 3 or 7 shall transmit TPS1, TPS2, TPS3 or TPS4 accordingly.
- A DP OUT Adapter that receives a SET_CONFIG Packet of Type SET_TRAINING with the *TS* field equal to 0 may transition to transmit IDLE pattern according to the DisplayPort Specification or continue transmitting the same TPS it is currently transmitting.
- A DP OUT Adapter shall set its Voltage Swing (VS) and Pre-Emphasis (PE) levels for all enabled lanes upon receiving a SET_CONFIG Packet of type SET_VSPE. The VS and PE levels shall be according to the MSG Data. The DP OUT Adapter shall transition on the 10-bit symbol boundary when:
 - Transitioning from one training pattern to another training pattern.
 - Transitioning to IDLE sequence after DP Link training is done.

10.4.10.1.3 DP Link Training Example

The DP Link Training process in this section describes a system which, from the DisplayPort point of view, consists of DPTX, DPRX and one LTTTPR in LTTTPR Non-Transparent mode. The DPRX's maximum supported link rate is HBR2, and it does not support TPS4. The DPTX establishes a DP Link of 2 lanes at HBR2 link rate.

10.4.10.1.3.1 LTTTPR – CR_DONE Phase

Figure 10-19 shows a sequence of events that starts from DP Link training initiation and gets the LTTTPR to achieve CR_DONE:

1. DP Link Training Start
 - As defined in the DisplayPort Specification, the DPTX starts the DP Link training with a write to DPRX's LINK_BW_SET and LANE_COUNT_SET.
 - The DP IN Adapter snoops that transaction to record the Training parameters.
2. TPS1 Initiate
 - DPTX starts transmitting TPS1.
 - DPTX writes TPS1 to TRAINING_PATTERN_SET_PHY_REPEATER1 and Level0 to Voltage Swing and Pre-emphasis at TRAINING_LANE_x_SET_PHY_REPEATER1.
 - The DP IN Adapter alters the AUX NACK response to an AUX ACK response.
3. DP OUT Adapter Initiation
 - A DP IN Adapter sends SET_CONFIG Packet of type 8B10B_SET_LINK, carrying the DP Link training parameters and *DP Link Training Mode* = 1b.
 - The DP OUT Adapter starts its Symbol clock PLL according to the received *Link Rate* field and starts the Lifetime Counter.
4. CR Status
 - DPTX reads LTTTPR's status from LANE0_1_STATUS & ADJUST_REQUEST_LANE0_1.
 - The DP IN Adapter alters the AUX response according to its internal CR_DONE state. In this example, it achieves CR_DONE on both Lanes.

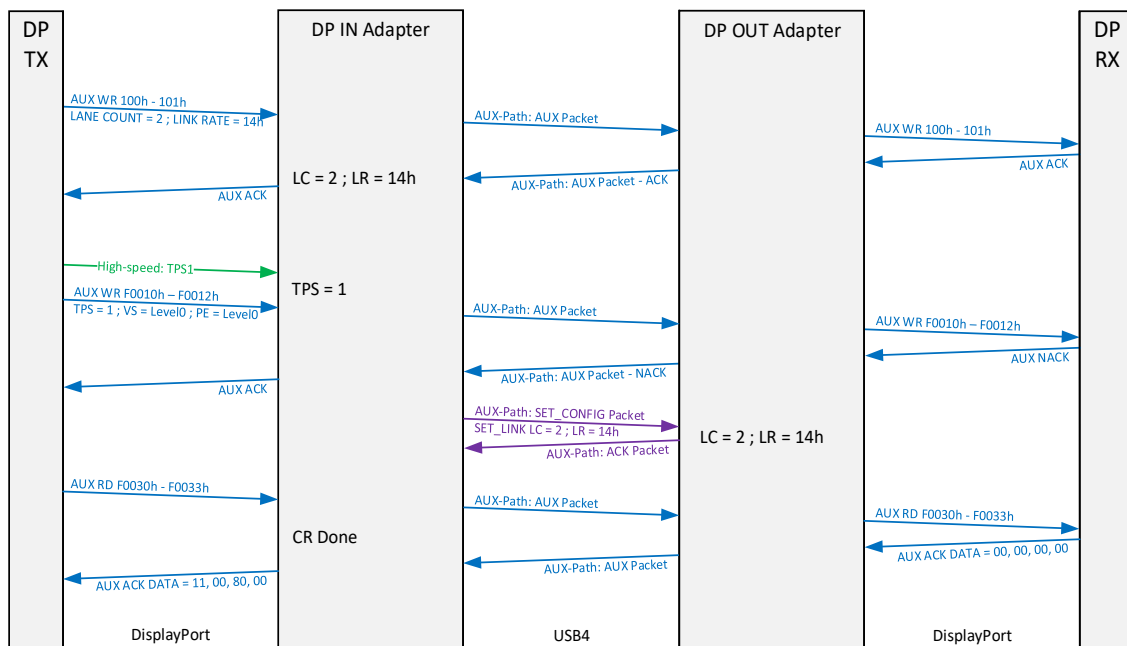
Figure 10-19. DP Link Training – LTTPR CR_DONE**10.4.10.1.3.2 LTTPR – EQ Phase**

Figure 10-20 shows a sequence of events that starts from DPTX Transmit TPS4 and ends as DPTX finishes LTTPR EQ phase:

1. TPS4 Initiate
 - DPTX starts transmitting TPS4.
 - DPTX writes TPS4 to TRAINING_PATTERN_SET_PHY_REPEATER1 and Level0 to Voltage Swing and Pre-emphasis at TRAINING_LANE_x_SET_PHY_REPEATER1.
2. EQ Status
 - The DP IN Adapter achieves equalization, symbol lock and lanes alignment.
 - The DP IN starts its Lifetime Counter.
 - DPTX reads LTTPR's status from LANE0_1_STATUS, LANE_ALIGN_STATUS_UPDATED & ADJUST_REQUEST_LANE0_1.
 - The DP IN Adapter alters the AUX response according to:
 - Its internal EQ_DONE, SYMBOL_LOCK & LANE_ALIGNMENT states.
 - It sent at least nine DP Clock Sync Packets.
 - In this example, it achieves EQ_DONE, SYMBOL_LOCK & LANE_ALIGNMENT on both Lanes and was able to send at least nine DP Clock Sync Packets.
3. End LTTPR Training
 - DPTX writes 0x0 to TRAINING_PATTERN_SET_PHY_REPEATER1 signifying that DP Link training between the DPTX and the UFP of the LTTPR is done.
 - A DP IN Adapter sends a SET_CONFIG Packet of type SET_TRAINING with a TS field = 0xFF.

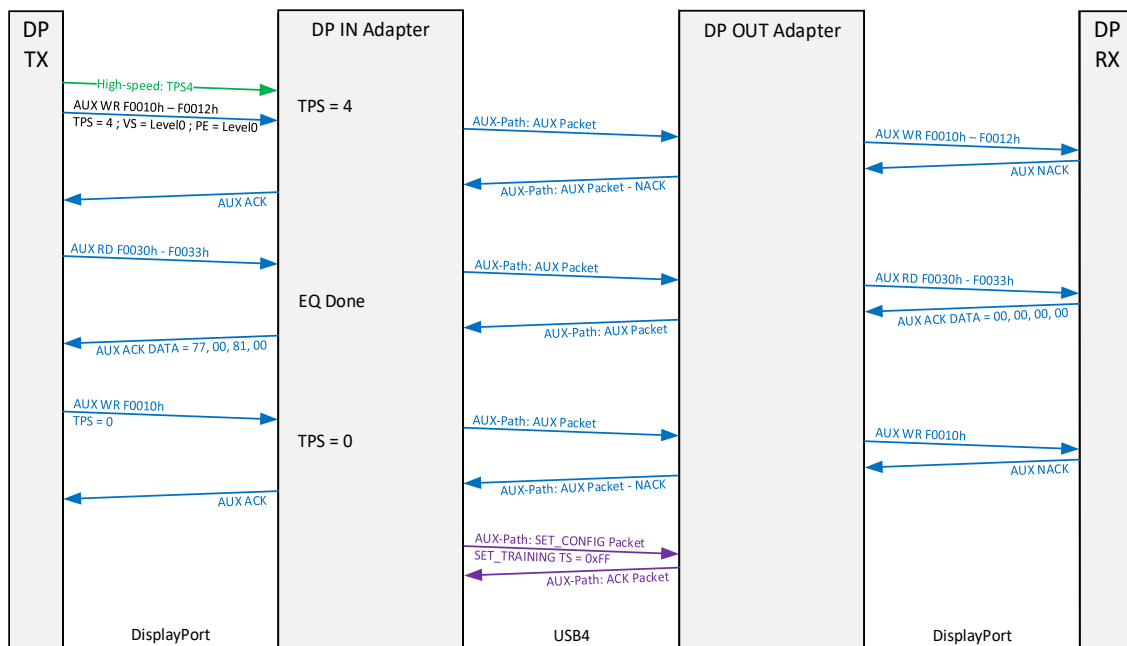
Figure 10-20. DP Link Training – LTPR – EQ Phase**10.4.10.1.3.3 DPRX – CR_DONE Phase**

Figure 10-21 shows a sequence of events which starts from transition to TPS1 across all DP Links, tunes the voltage swing, and ends when DPRX achieves CR_DONE:

1. DP OUT Adapter Transmit enable
 - DPTX switches from transmitting TPS4 to transmitting TPS1.
 - A DP IN Adapter detects TPS1 and sends SET_CONFIG Packet of type SET_TRAINING with a TS field = 0x1.
 - A DP OUT Adapter enables and configures its transmitters according to the received SET_CONFIG Packets. In this example, the DP OUT Adapter enables 2 Lanes at a bit rate of HBR2, transmitting TPS1.
 - DPTX writes TPS1 to TRAINING_PATTERN_SET and Level0 to Voltage Swing and Pre-emphasis at TRAINING_LANE0_SET to DPRX.
2. DPRX CR Status
 - DPTX reads DPRX's status from LANE0_1_STATUS & ADJUST_REQUEST_LANE0_1.
 - DPRX, in this example, responds with CR not done and a request for Voltage swing Level2.
3. Voltage swing setting
 - DPTX responds to DPRX's request with a write of Level2 for Voltage swing.
 - A DP IN Adapter snoops the AUX write transaction and sends SET_CONFIG Packet of type SET_VSPE holding the value of the AUX write request value written to DPCD 00103h, in this example Voltage swing 2.
 - A DP OUT Adapter sets its transmitter levels according to the SET_CONFIG SET_VSPE Packet.
4. DPRX CR Status
 - DPTX reads DPRX's status from LANE0_1_STATUS, LANE_ALIGN_STATUS_UPDATED & ADJUST_REQUEST_LANE0_1.

- DPRX, in this example, responds with CR done.

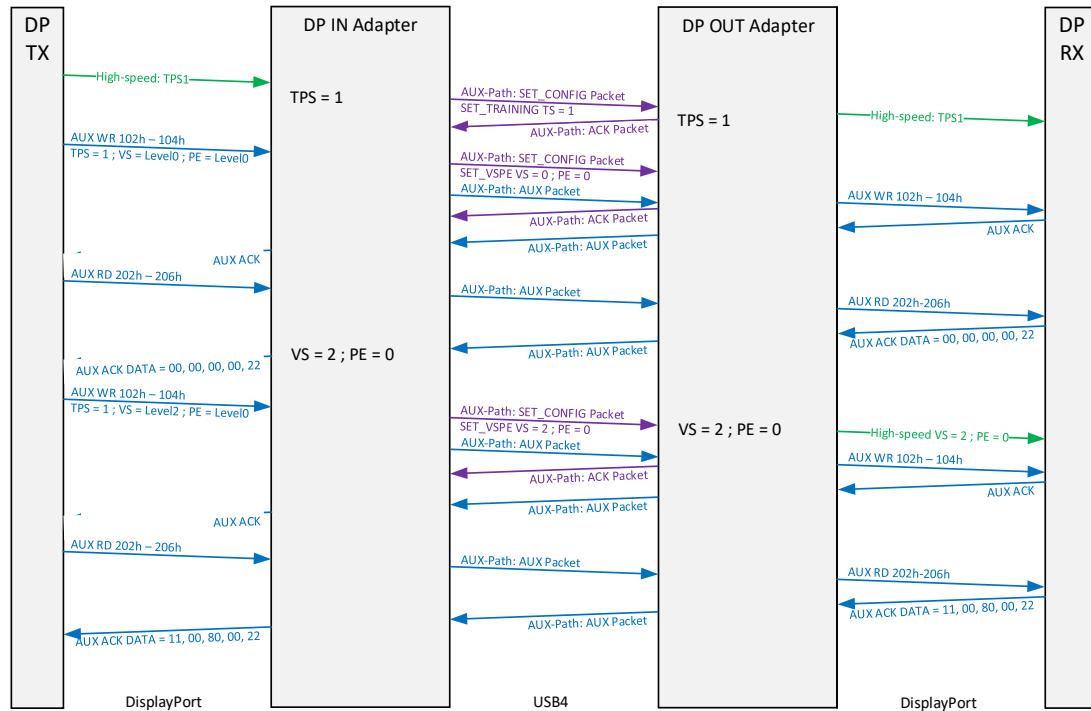
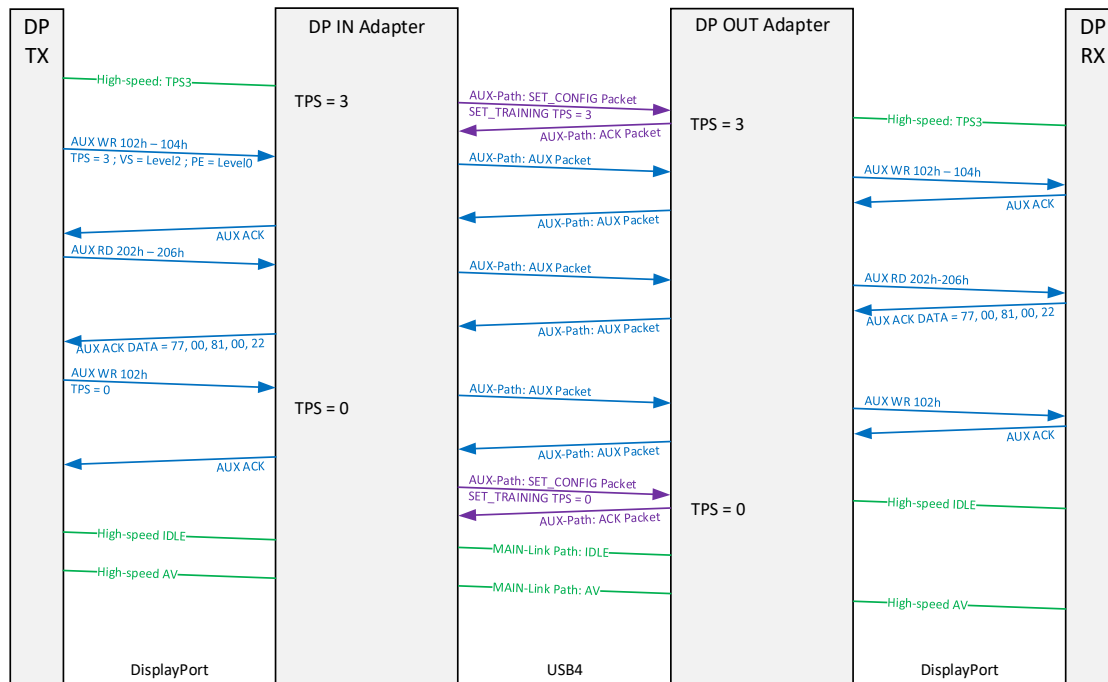
Figure 10-21. DP Link Training – DPRX – CR_DONE Phase**10.4.10.1.3.4 DPRX – EQ Phase**

Figure 10-22 shows a sequence of events which starts by transitioning to TPS3 and Completing EQ phase and ends with the completion of the whole DP Link Training process.

1. TPS3 transition
 - DPTX switch from transmitting TPS1 to transmitting TPS3.
 - A DP IN Adapter detects TPS3 and sends SET_CONFIG Packet of type SET_TRAINING with *TS* field = 0x3.
 - The DP OUT Adapter switches from transmitting TPS1 to transmitting TPS3.
 - DPTX writes TPS3 to TRAINING_PATTERN_SET and Level2 to Voltage Swing and Level0 Pre-emphasis at TRAINING_LANE_x_SET.
2. EQ Status
 - DPTX reads DPRX's status from LANE0_1_STATUS, LANE_ALIGN_STATUS_UPDATED & ADJUST_REQUEST_LANE0_1.
 - DPRX, in this example, achieves EQ_DONE, SYMBOL_LOCK & LANE_ALIGNMENT on both lanes.
3. DP Link Training End
 - DPTX writes 0x0 to TRAINING_PATTERN_SET signifying that DP link training between the DPTX and the DPRX, including the LTTPr, is done.
 - A DP IN Adapter sends SET_CONFIG of type SET_TRAINING with *TS* field = 0x0.
 - A DP OUT Adapter switches from transmitting TP3 to transmitting IDLE pattern as defined in the DisplayPort Specification.
 - DPTX switches from transmitting TPS3 to transmitting IDLE.
 - A DP IN Adapter detects the end of the link training and upon receiving SR it starts tunneling the high speed data over the Main-Link Path.

- A DP OUT Adapter switches from the self-generated IDLE pattern to the high speed tunnel data coming over the Main-Link Path.

Figure 10-22. DP Link Training – DPRX – EQ Phase

10.4.10.2 8b/10b Non-LTTPR and 8b/10b LTTPR Transparent

When a DPTX performs link training, either in 8b/10b Non-LTTPR or in 8b/10b LTTPR Transparent modes, it trains the DP IN Adapter receiver – it is unaware of the second DisplayPort link being trained by the DP OUT Adapter. The two DisplayPort links are trained simultaneously. The DP IN Adapter aggregates the status from each link when responding to the DPTX.

A DP Adapter shall perform DisplayPort link training according to the DisplayPort Specification with the modifications and requirements defined in Section 10.4.10.2.1 and Section 10.4.10.2.2.

10.4.10.2.1 DP IN Adapter Requirements

A DP IN Adapter shall send a SET_CONFIG Packet of type 8B10B_SET_LINK after DPTX writes TPS1 to the DP RX TRAINING_PATTERN_SET DPCD register. The SET_CONFIG packet shall have the following values:

- LC = LANE_COUNT_SET value written by DPTX.
- LR = LINK_BW_SET value written by the DPTX.
- TPS = Reflects TPS3 and TPS4 support as indicated in the DP_COMMON_CAP register.
- MSG Data = 0b, representing *DP Link Training Mode* = Non-LTTPR and LTTPR Transparent modes.

A DP IN Adapter shall respond to a status read of LANEx_CR_DONE as follows:

- If a SET_CONFIG Packet of type STATUS_CR_DONE was not received since link training started, set the *LANEx_CR_DONE* bits to 0b.
- If a SET_CONFIG Packet of type STATUS_CR_DONE was received since link training started, set the *LANEx_CR_DONE* bits to be the internal DP IN Adapter status for a lane ANDed with the relevant bit present in the last received SET_CONFIG MSG Data.

A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true:

- The DP IN Adapter internal status indicates link training has ended successfully.
- The DP IN Adapter received a SET_CONFIG Packet of type 8B10B_SET_LINK, carrying the same *LC* and *LR* fields that it sent to the DP OUT Adapter when link training was initiated.
- The DP IN Adapter sent at least nine DP Clock Sync Packets after it received a SET_CONFIG Packet of type STATUS_CR_DONE.

While the conditions (as defined in this section) for successful link training are not met, a DP IN Adapter shall respond to a status read of INTERLANE_ALIGN_DONE, LANEx_CHANNEL_EQ_DONE and LANEx_SYMBOL_LOCKED as follows:

- If a SET_CONFIG Packet of type STATUS_TRAINING_FAIL was received since link training started, set the following bits:
 - *INTERLANE_ALIGN_DONE* shall be set to 0b.
 - *LANEx_CHANNEL_EQ_DONE* is equal to the DP IN internal status ANDed with *LANEx_CHANNEL_EQ_DONE* that was received as MSG Data by the STATUS_TRAINING_FAIL.
 - *LANEx_SYMBOL_LOCKED* is equal to the DP IN internal status ANDed with *LANEx_SYMBOL_LOCKED* that was received as MSG Data by the STATUS_TRAINING_FAIL.
- Else, a DP IN Adapter shall use one or more of the methods below to indicate to DPTX that link training has not completed successfully yet.
 - Set *INTERLANE_ALIGN_DONE* to 0b.
 - Set *LANEx_CHANNEL_EQ_DONE* to 0b for any of the active lanes.
 - Set *LANEx_SYMBOL_LOCKED* to 0b for any of the active lanes.

Note: Which indication(s) to negate is implementation specific.

10.4.10.2.2 DP OUT Adapter Requirements

A DP OUT Adapter receiving a SET_CONFIG Packet of type 8B10B_SET_LINK, with *LC* field other than 0h shall:

- Initiate link training with the target Link Rate and Lane Count received from the 8B10B_SET_LINK Packet.
- Link training proceeds according to the DisplayPort Specification except that a DP OUT Adapter that concludes that it needs to either reduce the Link Rate or Lane Count shall treat it as link training failure and shall not reduce the Link Rate or Lane Count.

A DP OUT Adapter which finishes the Clock Recovery Sequence (as defined in the DisplayPort Specification) shall send a SET_CONFIG Packet of type 8b10b STATUS_CR_DONE, reflecting the LANEx_CR_DONE statuses of the active lanes. The *Phase* field shall be set to 0b.

If at the end of the EQ phase, link training is not successful and a DP OUT Adapter detects that the DP receiver has lost Clock Recovery on one or more of the active lanes, it shall send a SET_CONFIG Packet of type 8b10b STATUS_CR_DONE, reflecting the new LANEx_CR_DONE statuses of the active lanes. The *Phase* field shall be set to 1b.

If link training fails for a reason other than lost Clock Recovery, a DP OUT Adapter shall send a SET_CONFIG Packet of type STATUS_TRAINING_FAIL. The MSG Data shall be set as follows:

- LANEx_CHANNEL_EQ_DONE is equal to the value of the last read from *LANEx_CHANNEL_EQ_DONE* field in DPRX.
- LANEx_SYMBOL_LOCKED is equal to the value of the last read from *LANEx_SYMBOL_LOCKED* field in DPRX.

If link training finishes successfully, a DP OUT Adapter shall send a SET_CONFIG Packet of type 8B10B_SET_LINK, with the same *LC* and *LR* fields it received from the DP IN Adapter when link training was initiated. The DP OUT Adapter may then either transition to transmitting IDLE pattern (including SR) for both MST and SST DP Links or keep transmitting the same TPS it is currently transmitting.

10.4.10.3 128b/132b LTTTPR

The DP IN and DP OUT Adapters follow the 128b/132b link training as defined in the DisplayPort 2.1 Specification, acting as a single LTTTPR, with the following exceptions:

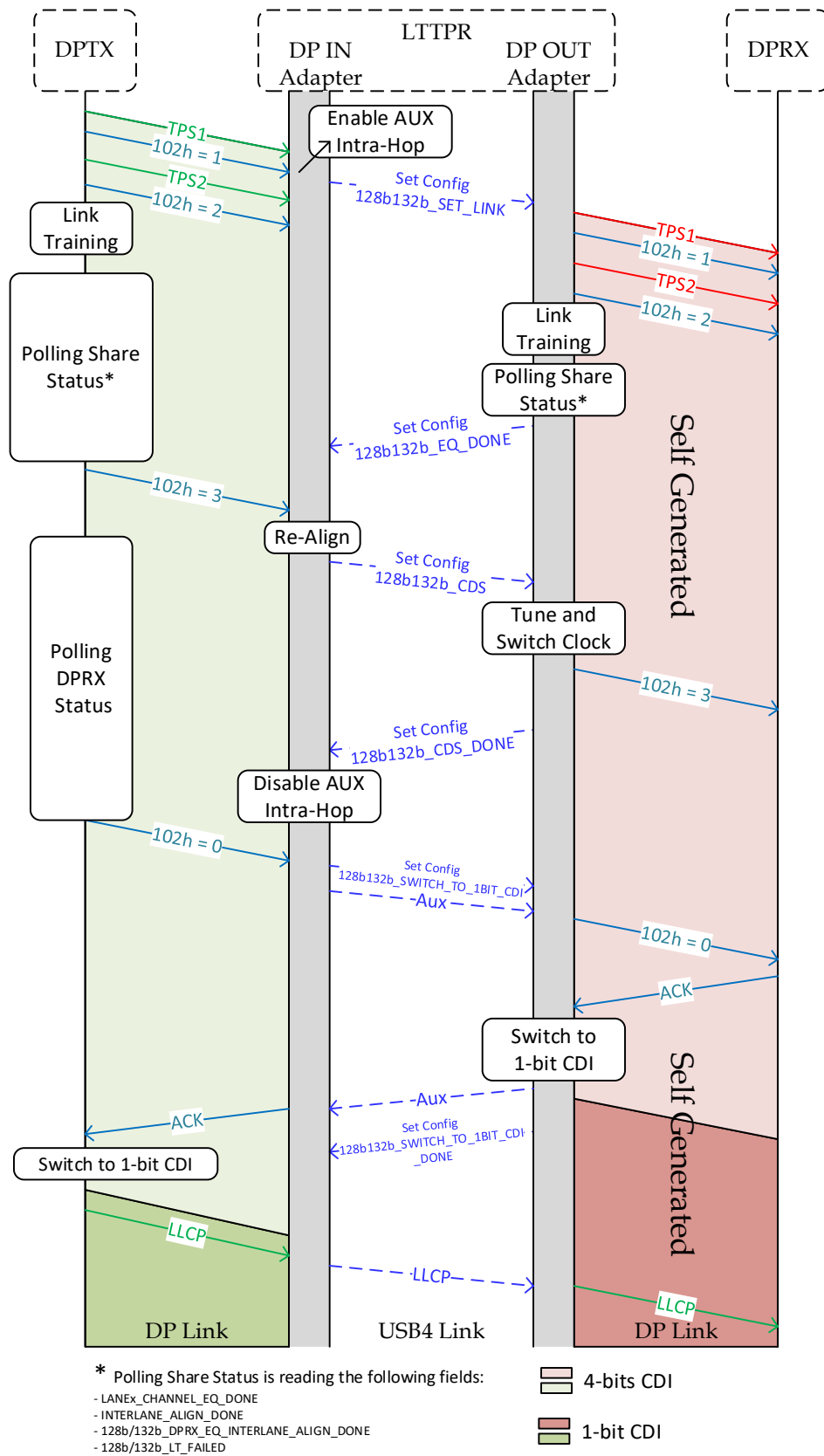
- The following 128b/132b link constructs are not tunneled:
 - 128b/132b_TPS1.
 - 128b/132b_TPS2.
 - PHY SYNC Symbols.
- Data switch doesn't occur during the CDS phase.

A DP IN Adapter shall act as the upstream facing port of the LTTTPR, according to the DisplayPort Specification. The additional requirements for a DP IN Adapter are listed in Section 10.4.10.3.1.

A DP OUT Adapter shall act the downstream facing port of the LTTTPR, according to the DisplayPort Specification. The additional requirements for a DP OUT Adapter are listed in Section 10.4.10.3.2.

Figure 10-23 illustrates a successful 128b/132b link training process.

Figure 10-23. 128b/132b Link Training Process



10.4.10.3.1 DP IN Adapter Requirements

- 128b/132b link training starts when a DPTX writes 01h to DPCD address 00102h and the MAIN_LINK_CHANNEL_CODING_SET is equal to 02h. When 128b/132b link training starts, a DP IN Adapter shall:
 - Respond with an AUX ACK.
 - Switch to operate in an AUX Intra-Hop mode, as defined by the DisplayPort Specification.
 - Set 128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE to 0b.
 - Set 128b/132b_LT_FAILED to 0b.
 - Send a SET_CONFIG Packet of type 128b132b_SET_LINK. The *MSG Data* of the SET_CONFIG packet shall have the following values:
 - LANE_COUNT_SET = LANE_COUNT_SET value written by DPTX.
 - LINK_BW_SET = LINK_BW_SET value written by the DPTX.
- A DP IN Adapter shall set the *128b/132b_LT_FAILED* bit to 1b if one of the following conditions are true, otherwise it shall be set to 0b:
 - The DP IN Adapter completed the EQ_DONE phase unsuccessfully.
 - A SET_CONFIG Packet of type 128b132b_EQ_DONE was received with the *128b/132b_LT_FAILED* bit set to 1b in the *MSG Data*.
- A DP IN Adapter shall set the *128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE* bit to 1b if all the following conditions are true, otherwise it shall be set to 0b:
 - The DP IN Adapter completed the EQ_DONE phase successfully.
 - A SET_CONFIG Packet of type 128b132b_EQ_DONE was received with the *128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE* bit set to 1b in the *MSG Data*.
- When a DPTX writes 03h to DPCD address 00102h and the MAIN_LINK_CHANNEL_CODING_SET is equal to 02h, a DP IN Adapter relocks on the link clock and realigns on the 128/132_TPS2, as defined in the DisplayPort Specification. When the DP IN Adapter completes realigning on the 128/132_TPS2, it shall:
 - Send a SET_CONFIG Packet of type 128b132b_CDS.
 - Start sending DP Clock Sync Packets.
- When a DP IN Adapter receives a SET_CONFIG Packet of type 128b132b_CDS_DONE, it shall disable the AUX Intra-Hop mode.
- When a DPTX writes 0h to DPCD address 00102h, the AUX Intra-Hop is disabled, and the link is still operating in 4-Bits CDI, it means that link training is ending successfully. A DP IN Adapter shall perform the following in order:
 1. Send a SET_CONFIG Packet of type 128b132b_SWITCH_TO_1BIT_CDI.
 2. Send the AUX Write request:
 - After sending the SET_CONFIG Packet of type 128b132b_SWITCH_TO_1BIT_CDI, a DP IN Adapter is ready to start converting DisplayPort 128b/132b Link Layer symbols into Tunneled Packets as defined in Section 10.5.3. A DP IN Adapter shall start converting DisplayPort 128b/132b Link Layer symbols into Tunneled Packets when it receives the first LLCP Link Layer Symbol.

Link Training is aborted as follows:

- When a DPTX writes 0h to DPCD address 00102h and the AUX Intra-Hop is enabled, a DP IN Adapter shall send a SET_CONFIG Packet of type 128b132b_LT_ABORT.
- When a DP IN Adapter receives a SET_CONFIG Packet of type 128b132b_LT_ABORT_DONE, it shall disable the AUX Intra-Hop mode.

10.4.10.3.2 DP OUT Adapter Requirements

Note: During 128b/132b DP Link Training, a DP OUT Adapter generates its own AUX Transactions. It stops generating AUX Transactions after DP Link Training is complete.

- When a DP OUT Adapter receives a SET CONFIG Packet of type 128b132b_SET_LINK, it shall start the 128b132 EQ_DONE link training phase as defined by the DisplayPort specification:
 - The DP OUT Adapter shall set the link rate to be equal to the *LINK_BW_SET* field it received in the *MSG Data* of the SET CONFIG Packet.
 - The DP OUT Adapter shall set the lane count to be equal to the *LANE_COUNT_SET* field it received in the *MSG Data* of the SET CONFIG Packet.
- A DP OUT Adapter completes the EQ_DONE phase when one of the two conditions are met:
 - Failure: The read value from the *128b/132b_LT_FAILED* bit is 1b.
 - Success: EQ_DONE phase ends successfully and the read value from the *128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE* bit is 1b.
- When a DP OUT Adapter completes the EQ_DONE phase it shall send a SET CONFIG Packet of type 128b132b_EQ_DONE with the following *MSG Data*:
 - *Local EQ_DONE Succeeded* – If all activate lanes reported *LANEx_CHANNEL_EQ_DONE* = 1b then set this bit to 1b, else set this bit to 0b.
 - *128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE* – Shall be set to 1b in case of EQ_DONE phase ended successfully, else shall be set to 0b.
 - *128b/132b_LT_FAILED* – Shall be set to 0b in case of EQ_DONE phase ended successfully, else shall be set to 1b.
- When a DP OUT Adapter receives a SET CONFIG Packet of type 128b132b_CDS it shall do the following:
 1. Start adjusting the PLL frequency as described in Section 10.6.
 2. Ensure, in an implementation specific manner, that within eight PLL frequency adjustments the link symbol clock frequency difference between its own and the DPTX is such that buffer overflow and buffer underrun is avoided.
 3. Write 03h to DPCD address 00102h and receive an AUX ACK.
 - A DP OUT Adapter shall not self-generate any more AUX Transactions after receiving the AUX ACK.
 4. Send a SET CONFIG Packet of type 128b132b_CDS_DONE.

Note: A DP OUT Adapter does not perform a data switch as part of the CDS phase.

- When a DP OUT Adapter receives a SET CONFIG Packet of type 128b132b_SWITCH_TO_1BIT_CDI, it shall parse the next AUX Response:
 - If the response is an AUX ACK, a DP OUT Adapter shall do the following:
 1. Transition from 128b/132_TPS2 to normal operation at the next PHY Sync symbol.
 2. Send the AUX ACK.
 3. Send a SET CONFIG Packet of type 128b132b_SWITCH_TO_1BIT_CDI_DONE.

When a DP OUT Adapter receives a SET CONFIG Packet of type 128b132b_LT_ABORT it shall do the following steps:

1. Terminate the link training process as defined in the DisplayPort Specification.
2. If an AUX transaction is ongoing, wait for its completion.
3. Send a SET CONFIG Packet of type 128b132b_LT_ABORT_DONE

10.4.10.4 Transition to High Speed Tunnel

A DP IN Adapter shall start converting DisplayPort Main-Link Symbols into Tunneled Packets and sending those Packets over the Main-Link Path when all the following are true:

- Link Training has completed successfully.
- For an 8b/10b DP Link: The DP IN Adapter received an SR.
- For a 128b/132b DP Link: The DP IN Adapter received an LLCp.

A DP OUT Adapter transitions from sending IDLE pattern or TPS to reconstructing the DisplayPort Main-Link symbols according to Section 10.5.4.2.

Note: The rules for sending Clock Sync Packets are defined in Section 10.6. DP Clock Sync Packets are not gated by receiving an SR from DPTX.

10.4.11 Power States Set

When DPTX writes to DPCD address 00600h, a DP IN Adapter shall snoop the write request and record the value of the *SET_POWER_STATE* field. A DP IN Adapter shall send a SET_CONFIG Packet of type SET_POWER, reflecting the recorded value in the following cases:

- A first DPCD write of address 00600h after an HPD Plug event.
- The new recorded SET_POWER_STATE is different than the previous value.

The SET_POWER_STATE default value at the DP Adapters is defined in the DisplayPort Specification.

If the SET_POWER_STATE is 2h or 5h, a DP IN Adapter may choose to initiate the DP Main-Link disable flow defined in Section 10.4.12.

The Low Power state enables both DP Adapters to save power according to the SET_POWER_STATE of the DPRX. The means by which the DP Adapters may save power are implementation specific and outside the scope of this specification.

10.4.12 DP Main-Link Disable

A DP IN Adapter may disable its Main-Link receivers and send a Main-Link disable message in the following events:

- The DP IN Adapter experiences excessive disparity or symbol error which results in the clearing of *LANEx_SYMBOL_LOCKED* and *INTERLANE_ALIGNED_DONE* bits.

If *MAIN_LINK_CHANNEL_CODING_SET* is equal to 01h, then the Main-Link disable message is a SET_CONFIG Packet of type 8b10b_SET_LINK with the *Link Rate* and *Lane Count* fields set to zero. Otherwise, it is a SET_CONFIG Packet of type 128b132b_SET_LINK with the *LINK_BW_SET* and *LANE_COUNT_SET* fields set to zero.

A DP OUT Adapter which receives a Main-Link disable message shall disable its transmitters.

Note: It is expected that the system recovers from a DP-Link failure as follows:

1. *DPRX experiences a DP Link failure and sends an IRQ.*
2. *DPTX reads the DP-Link status and discovers the DP-Link failure.*
3. *DPTX retrains the DP-Link.*

10.4.13 Link-Init

A Link-Init action may be triggered by:

- Connection Manager sets the *SWLI* bit in ADP_DP_CS_2 register to 1b.
- ACK Packet timeout expires.

Upon Link-Init activation, a DP IN Adapter shall turn off its DisplayPort receivers and stop any transmission of Tunneled Packets over the Main-Link Path until the end of the next successful Link training, as defined in Section 10.4.10.3.

Upon Link-Init activation, a DP OUT Adapter shall turn off its DisplayPort transmitters.

Note: It is expected that the system recovers from a DP-Link failure as follows:

1. *DPRX experiences a DP-Link failure and sends an IRQ.*
2. *DPTX reads the DP-Link status and discovers the DP-Link failure.*
3. *DPTX retrains the DP-Link.*

10.4.14 DP PHY Testability

The method for testing the PHY layer in a DP IN Adapter is defined in Section 10.4.14.1. The method for testing the PHY layer DP OUT Adapter is defined in Section 10.4.14.2.

10.4.14.1 DP IN Adapter PHY Layer Testing

The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort PHY CTS with the changes listed below.

- Before entering DP IN PHY Test Mode:
 - Connect a Router with a DP OUT Adapter and a DPRX. Both the DP OUT Adapter and the DPRX need to support the Link Rate and Lane Count required by the test.
 - Verify that a DP Link is established.
- Entering DP IN PHY Test Mode:
 - The DP IN Adapter shall enter DP IN PHY Test Mode when the DPTX writes a non-zero value to LINK_QUAL_LANE_x_SET in the DPCD registers.
- While in DP IN PHY Test Mode:
 - The DP IN Adapter shall keep the Hot Plug Detect signal high.
 - The DP IN Adapter shall respond to all AUX transactions related to the PHY layer testing.
- Exiting DP IN PHY Test Mode:
 - The DP IN Adapter shall exit DP IN PHY Test Mode when the DPTX initiates DP Link Training.

10.4.14.2 DP OUT Adapter PHY Layer Testing

The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort PHY CTS with the changes listed below.

- Before entering DP OUT PHY Test Mode:
 - Connect a Router with a DP IN Adapter and a DPTX. Both the DP IN Adapter and the DPTX need to support the test required Link Rate and Lane Count.
 - Verify that a DP Link is established.
- Entering DP OUT PHY Test Mode:
 - When the DPTX reads the following sequence, the DP IN Adapter shall send a SET_CONFIG Packet of Type SET_PHY_TEST_MODE and enter DP OUT PHY Test Mode:
 - AUTOMATED_TEST_REQUEST is set to 1b (DPCD 00201h or 02003h bit 1)
 - PHY_TEST_PATTERN is set to 1b (DPCD 00218h bit 3)
 - The DP OUT Adapter shall enter DP OUT PHY Test Mode when it receives a SET_CONFIG Packet of type SET_PHY_TEST_MODE.
- While in DP OUT PHY Test Mode:
 - The DP OUT Adapter shall act as the DPTX under test.
 - The DP OUT Adapter shall send HPD Packet with Plug Flag set to 0b.
 - The DP IN Adapter shall not forward any AUX Transactions to the DP OUT Adapter.
- Exiting DP OUT PHY Test Mode
 - Upon a DPRX HPD signal de-assertion:
 - The DP OUT Adapter shall exit DP OUT PHY Test Mode.
 - The Connection Manager tears down the DP Paths, causing both of the DP Adapters to enter the Present State.

10.4.15 CLx Support**10.4.15.1 AUX Paths****10.4.15.1.1 CLx Entry**

A DP IN Adapter initiates the removal of a CL1 objection on the AUX Paths by performing an AUX Path sleep handshake. The AUX Path sleep handshake shall only be performed if the DP_COMMON_CAP.Protocol Adapter Version is equal 5. A DP IN Adapter shall not initiate an AUX Path sleep handshake while it is waiting for an AUX Response from the DP OUT Adapter.

A DP IN Adapter may initiate the AUX Path sleep handshake by performing the following steps:

1. A DP IN Adapter sends a SET_CONFIG Packet of type AUX_PATH_CLX with S/W bit set to 1b.
2. If the DP_COMMON_CAP.ALPM Support bit is 1b and the *USB4 CL1 Granted through ALPM* bit in the DPCD Tunnel POWER MANAGEMENT CONFIGURATION (address E0032h bit 0) is set to 1b, a DP IN Adapter shall send a PM Packet with the *CLx State* field set to 01b over the AUX Path.

A DP OUT Adapter that receives a SET_CONFIG Packet of type AUX_PATH_CLX with *S/W* bit set to 1b shall:

1. Send the ACK Packet for the SET_CONFIG Packet.
2. Send a PM Packet with the *CLx State* field set to 01b over the AUX Path within tDPAUXSleepHS.

10.4.15.1.2 CLx Exit

If a DP IN Adapter initiates an AUX Path sleep handshake and does not send a SET_CONFIG Packet over the AUX Path after completing the handshake, then upon reception of an AUX Request, the DP IN Adapter shall send a SET_CONFIG Packet of type AUX_PATH_CLX with the *S/W* bit set to 0b. The following rules determine when the SET_CONFIG Packet shall be sent:

- If the DP IN Adapter sent a PM Packet with the *CLx State* field set to 01b as part of the last AUX Path sleep handshake, then it shall send the SET_CONFIG Packet within tDPAUXtoWAKE after receiving the end of the AUX_SYNC pattern of the AUX Request.
- Else it shall send the SET_CONFIG Packet within tDPAUXDelayIn after receiving the complete AUX Request.

In order to meet the above timing, a DP IN Adapter may send the SET_CONFIG Packet of type AUX_PATH_CLX with the *S/W* bit set to 0b without waiting tDPSetConfigGap time after the prior SET_CONFIG Packet.

10.4.15.2 Main-Link Path

10.4.15.2.1 ALPM Flow

A DP IN Adapter shall send a PM Packet with the *CLx State* field set to 01b over the Main-Link Path during the ALPM sleep sequence flow as described in Section 10.5.7.2.

A DP IN Adapter initiates exit from CLx during ALPM wake sequence flow as described in Section 10.5.7.3.

10.4.15.2.2 Inactive Main-Link

A DP IN Adapter may send a PM Packet with the *CLx State* field set to 01b over the Main-Link Path when the DP Main-Link is inactive.

A DP IN Adapter triggers an exit from CLx during DP Link training, when the first DP Clock Sync Packet is sent.

10.5 High Speed Tunneling

A DP IN Adapter converts DisplayPort Main-Link Symbols into Tunneled Packets. A DP OUT Adapter reconstructs the DisplayPort Main-Link Symbols received in Tunneled Packets.

128b/132b Tunneling, 8b/10b SST, and 8b/MST Tunneling share the following base concepts:

- The Main-Link Symbol clock generated by the DP OUT Adapter corrects any drift with respect to the DP IN Adapter Main-Link Symbol recovered clock. The total number of cycles over time is identical.
- FEC RS parity symbols are not packed into Tunneled Packets. A DP IN Adapter performs FEC Decoding while a DP OUT Adapter performs FEC Encoding.
- HDCP is supported. Encryption and decryption are not performed.
- A DP IN Adapter minimizes the delay between the time a Main-Link Tunneled Packets is ready to the time it is sent to the Transport Layer.

8b/10b MST and 8b/10b SST Tunneling share the following base concepts:

- All Main-Link Symbols, Data and Control, generated by the DP OUT Adapter are identical to the Main-Link Symbols received by the DP IN Adapter over the DP Link.

- All Main-Link Symbols are de-serialized, 8b/10 ANSI decoded and de-scrambled by the DP IN Adapter and packed into Tunneled Packets as 8-bit data characters.
- All Main-Link Stuffing Symbols are discarded by the DP IN Adapter and reconstructed by the DP OUT Adapter. Stuffing Symbols consists of:
 - SST – Dummy Symbols during horizontal and vertical Blanking and Stuffing Symbols during Active Video.
 - MST – SF and VCPF Symbol Sequences.

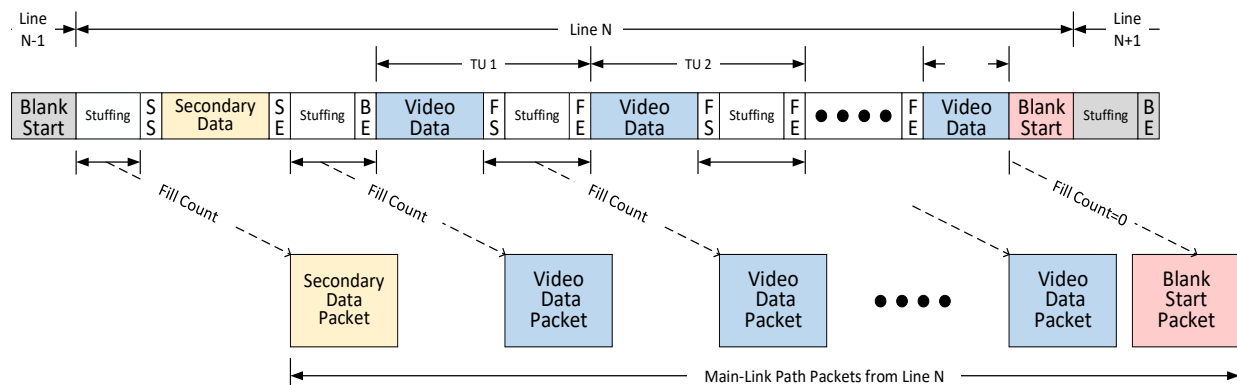
10.5.1 8b/10b SST Tunneling

The video and audio data carried over a DisplayPort SST Main-Link is organized into frames. Each frame contains several active scan lines followed by a vertical blanking period. Each scan line contains active pixel data followed by a horizontal blanking period. The active pixel data is organized into fixed-size chunks called Transfer Units. Each Transfer Unit (TU) contains active pixel data followed by Stuffing Symbols. Stuffing Symbols are also sent during the horizontal and vertical blanking periods.

When a DisplayPort SST Main-Link is mapped onto USB4, the continuous Main-Link data stream is encapsulated into Tunneled Packets. Before encapsulation, all the Stuffing Symbols (within a TU and during the blanking periods) are discarded by the DP IN Adapter. Stuffing Symbols are recreated by the DP OUT Adapter when the Main-Link data stream is extracted from the Tunneled Packets. In order to enable accurate reconstruction of the Stuffing Symbols at the DP OUT Adapter, the DP IN Adapter includes a *Fill Count* field in each Tunneled Packet. The *Fill Count* field specifies the number of Stuffing Symbols that were discarded immediately preceding the packet.

Figure 10-24 shows how a scan line is encapsulated into Tunneled Packets by a DP IN Adapter.

Figure 10-24. Main-Link SST Stream to Tunneled Packets



Note: DisplayPort Tunneling does not support Default Framing mode.

10.5.1.1 Video Data Packet

10.5.1.1.1 Transfer Unit Set

DisplayPort encodes active pixel data from a scan line into a sequence of Transfer Units. A Transfer Unit (TU) can be 32 to 64 link symbols per lane in length. If the Panel Replay feature is enabled, DisplayPort encodes dummy pixel data into Transfer Units. Tunneling of 8b/10b DP SST covers both Panel Replay operation and normal (Live Frame) operation. The length of a TU (TU_Size) is fixed by the DisplayPort source based on the selected display mode. Each TU contains active pixel data followed by zero or more Stuffing Symbols. The active pixel data in a TU can range from 1 byte to TU_Size bytes in length. The Stuffing Symbols in a TU vary as follows:

- When the number of active pixel symbols is less than (TU_Size – 2), Stuffing Symbols are delineated by Fill Start (FS) and Fill End (FE) control symbols.
- When the number of active pixel symbols is equal to (TU_Size – 2), the FS and FE control symbols are the only Stuffing Symbols present.
- When the number of active pixel symbols is equal to (TU_Size – 1), the FE control symbol is the only Stuffing Symbol present.
- When the number of active pixel symbols is equal to TU_Size, no Stuffing Symbols are present.

At the end of a scan line, the leftover pixel data symbols constitute the last TU of the scan line. The last TU of the scan line does not contain any Stuffing Symbols. The leftover pixel data symbols are followed by the Blank Start (BS) control symbol.

A DP IN Adapter shall pack the active pixel data of a TU into either one or two TU Sets. A TU Set is created by selecting a symbol from each lane of the Main-Link in a cyclic way, starting with lane 0. The packing of active pixel data into a TU Set for 4-Lane, 2-Lane and 1-Lane configurations is shown in Figure 10-25, Figure 10-26, and Figure 10-27 respectively.

Note: DisplayPort Tunneling does not support the case of a TU that holds no active pixel data.

Figure 10-25. TU Set Packing for a 4-Lane Main-Link

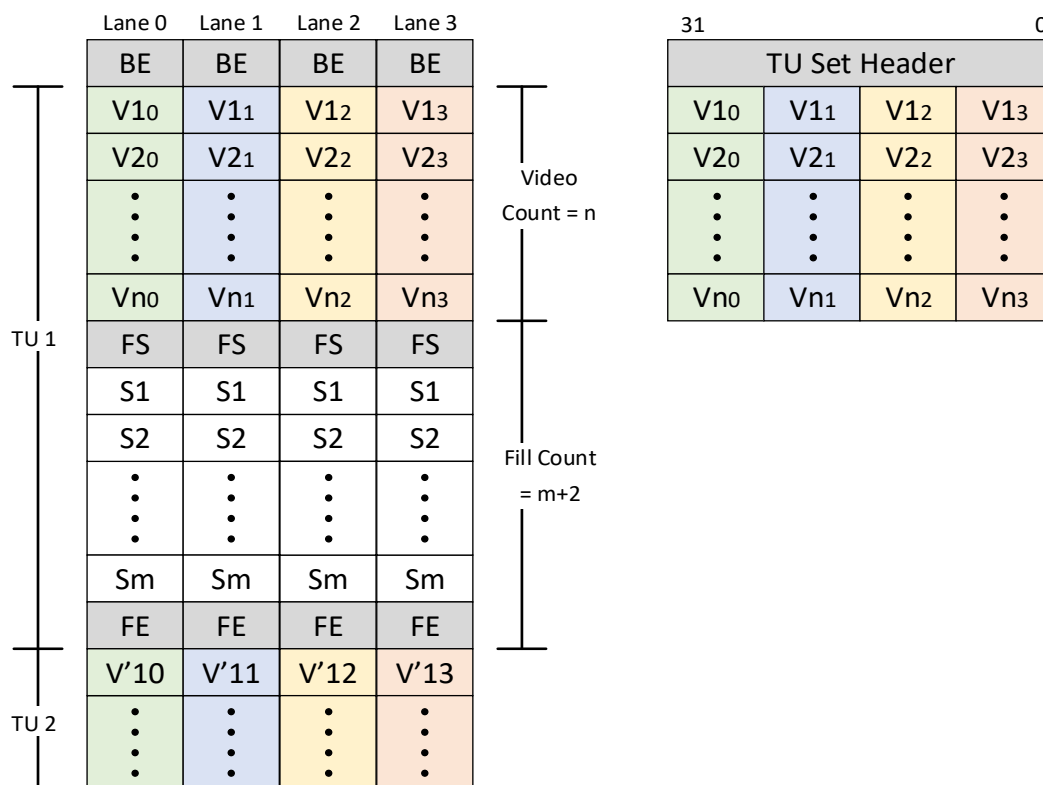


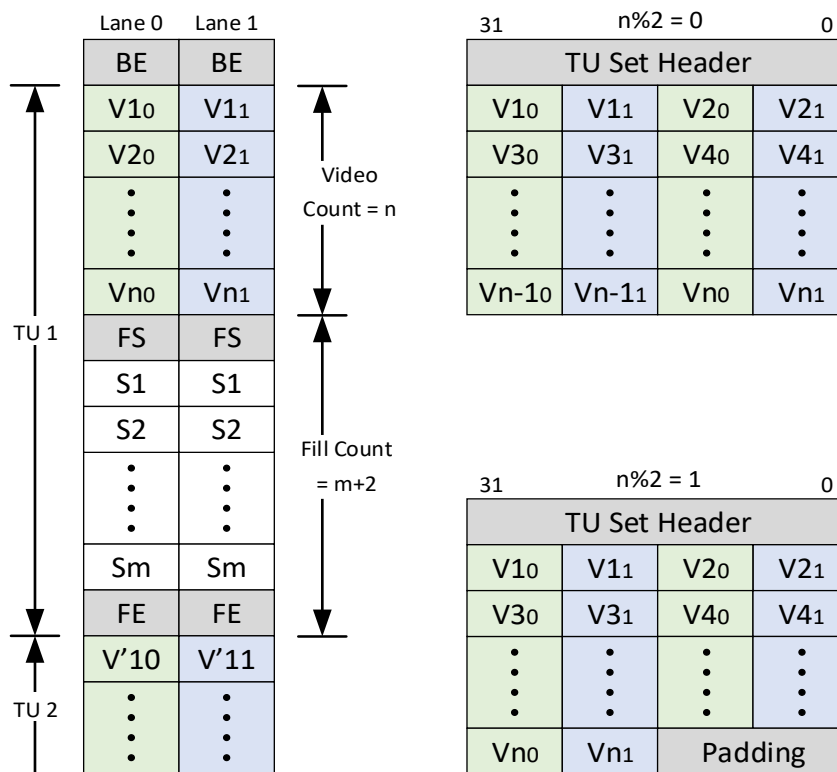
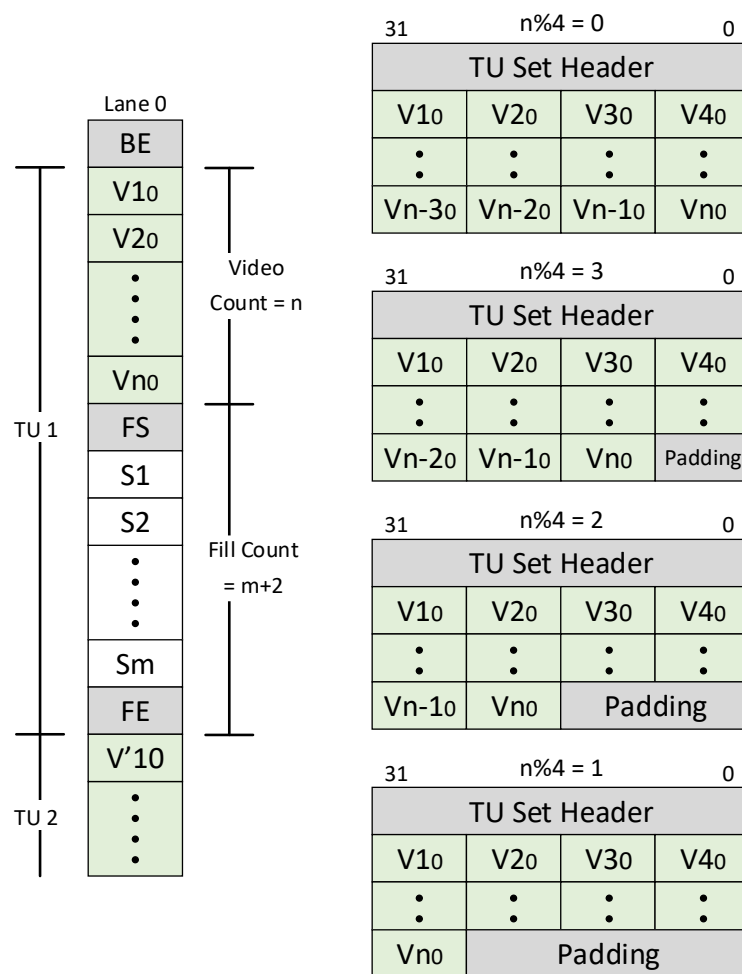
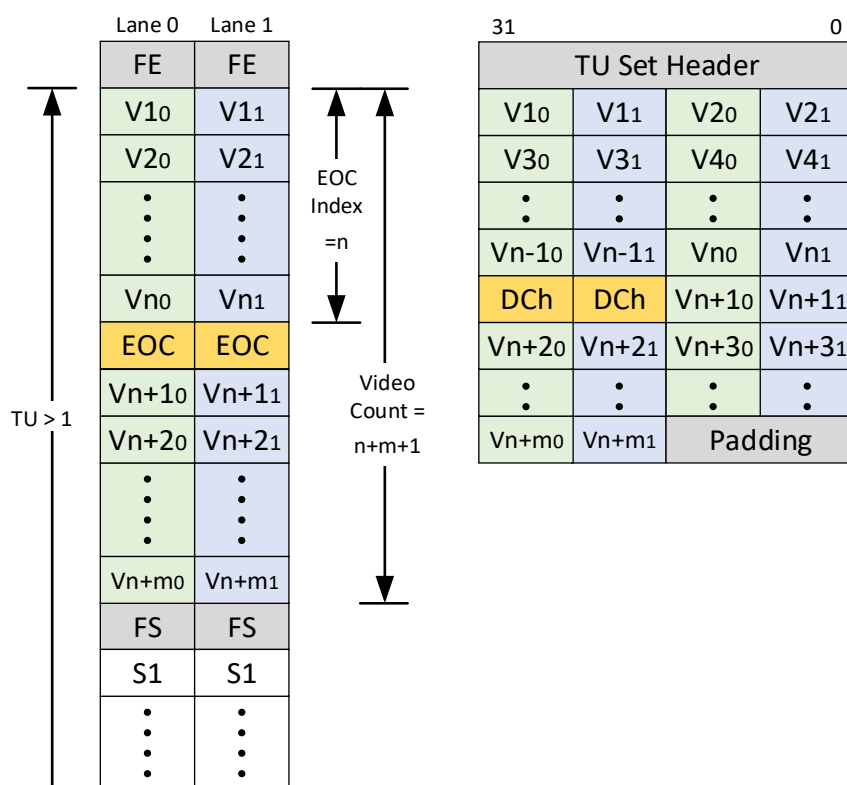
Figure 10-26. TU Set Packing for a 2-Lane Main-Link

Figure 10-27. TU Set Packing for a 1-Lane Main-Link

When EOC control link symbols are present in a TU, a DP IN Adapter shall pack the EOC symbols using the same scheme as for active pixel symbols. The EOC symbols shall be packed in their 8-bit value representation (DCh). Figure 10-28 shows an example of EOC symbol packing for a 2-lane Main-Link with n active video symbols before the EOC symbol and m active video symbols after it. The Video Count value of n+m+1 in this example is padded with 2 bytes to make the TU Set 32-bit aligned.

Figure 10-28. EOC Symbol Packing Example

During Panel Replay operation, a DPTX replaces BE with K28.7, to signify that the current video line is a dummy pixel line. In a dummy pixel line, all pixel data symbols are dummy data symbols, while the TU structure and timing remains the same as an active pixel line. When a DP IN Adapter supports Panel Replay Tunneling Optimization and it receives K28.7, it shall pack all the TUs within the dummy pixel line into TU Sets according to the same rules that are defined for a normal TU (i.e. a TU with an active pixel line) with the following exceptions:

- The TU Type shall be set to 01b
- The dummy data symbols shall not be packed into the TU Set.

Note: The dummy data symbols are still counted, and their count is reflected in the Video Count field within the TU Header.

- If EOC is present, its 8-bit representation (DCh), shall not be sent.

A DP OUT Adapter shall generate a BE control symbol before the first TU of an active or dummy pixel line, for both TU Type values 00b and 01b.

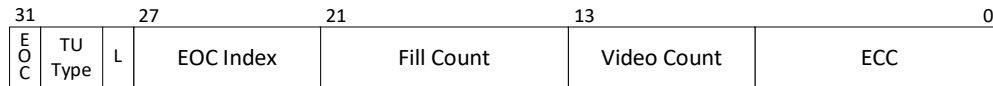
Each TU Set shall be prepended with a TU Set Header. Figure 10-29 shows the two formats for a TU Set Header.

Figure 10-29. TU Set Header Format

A – No EOC (Default)



B – EOC



The header in Figure 10-29(A) shall be used for a TU Set that contains a TU with no EOC Symbol. The header in Figure 10-29(B) shall be used for a TU Set that contains a TU with an EOC symbol. The fields forming the TU Set Header shall be as defined below:

- **ECC [7:0]:** Error correction field that is calculated over bits [31:8] of the TU Set Header. See Section 5.1.2.3 for calculation.
- **Video Count [13:8]:**
 - When TU Type = 00b (active pixel line), if the TU Set does not contain an EOC symbol, this field shall contain the number of active video symbols per lane. If the TU Set contains an EOC symbol, this field shall contain the number of active video symbols per lane plus 1. A value of zero represents 64. The total number of active video symbols in the TU Set is equal to (Video Count * Number of Lanes).

Note: The Video Count is set to 1h when a TU Set contains an EOC symbol and no active video symbols.

 - When TU Type = 01b (dummy pixel line), if the TU Set does not contain an EOC symbol, this field shall contain the number of dummy data symbols per lane. If the TU Set contains an EOC symbol, this field shall contain the number of dummy data symbols per lane plus 1. A value of zero represents 64.

Note: The Video Count is set to 1h when a TU Set contains an EOC symbol and no dummy data symbols.
- **(No EOC) Fill Count [27:14]:** This field shall have the value as defined in 10.5.1.5.
- **(EOC) Fill Count [21:14]:** This field shall have the value as defined in 10.5.1.5.
- **(EOC) EOC Index [27:22]:** This field shall contain the index of the EOC symbol inside the TU Set. Symbols within a TU Set are indexed starting with zero (for the first symbol) and ending with (Video Count – 1) for the last symbol.
- **L [Bit 28]:** Last TU Flag. This bit shall be set to 1b if the TU is the last TU Set of a line. Otherwise, this bit shall be set to 0b.
- **TU Type [30:29]:**
 - 00b – A TU Set that is part of an active pixel line.
 - 01b – A TU Set that is part of a dummy pixel line.
 - 10b-11b – Reserved.
- **EOC [Bit 31]:** This field shall be set to 1b if the TU Set contains an EOC symbol. Otherwise shall be set to 0b.

Note: DisplayPort Tunneling does not support the cases where hblank is bigger than 16370 cycles.

10.5.1.1.2 Packet Format

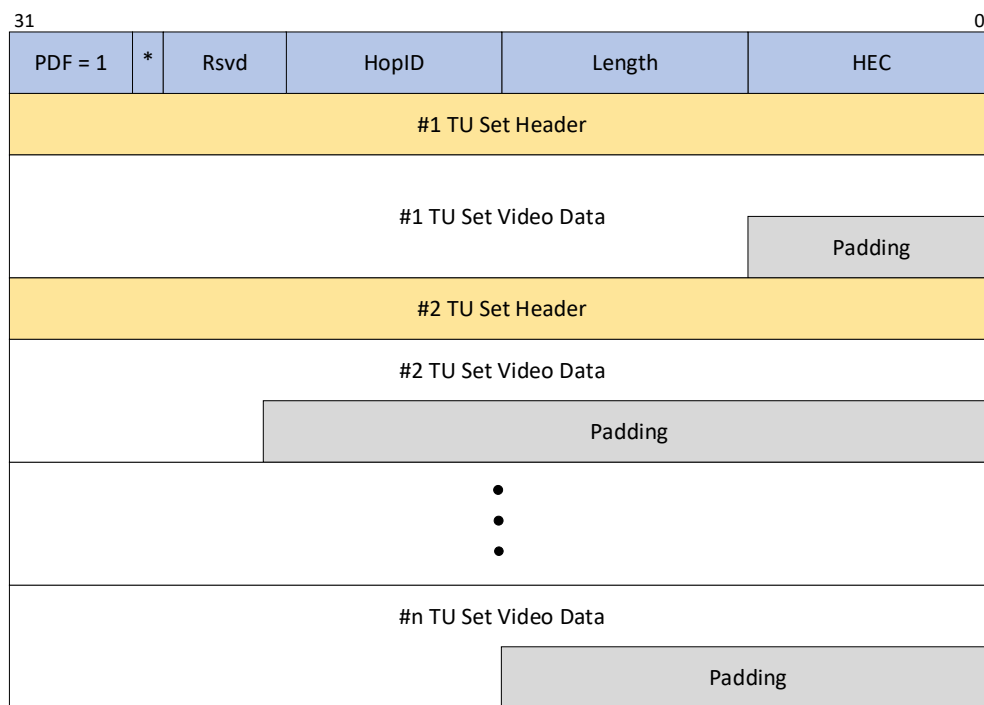
A Video Data Packet has the *PDF* field in the Tunneled Packet Header set to 1. A Video Data Packet shall have the format shown in Figure 10-30. As shown in Figure 10-30, the first 4 bytes of the Video Data Packet payload contain the first TU Set Header, followed by the video data payload of the first TU set. Additional TU Sets are appended to the payload of the Video Data Packet. It is recommended that a Video Data Packet include as many TU Sets as possible in order to reduce overhead on the USB4 Fabric.

All TU Set Headers within the Video Data Packet payload shall be aligned to 32-bits by adding padding bytes at the end of the TU set payload if necessary. The padding bytes may contain any value, however it is recommended that zero padding be used.

A DP IN Adapter shall follow the rules below when constructing a Video Data Packet:

- A Video Data Packet shall contain at least 1 TU Set and no more than 16 TU Sets. If a TU cannot fit within a single Video Data Packet, it shall be split into two TU sets.
- When a TU is split into two TU Sets, the remainder of the active pixel symbols shall be sent in the first TU Set in the next Video Data Packet. The *Fill Count* field in the TU Set Header of the second Video Data Packet for a TU that is split into multiple Video Data Packets shall be set to 0.
- The length of all TU Set Padding is included when calculating the *Length* field in the Tunneled Packet Header.

Figure 10-30. Video Data Packet Format



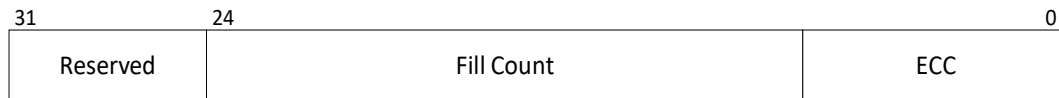
* SupplD

10.5.1.2 Main Stream Attribute Packet

The Main Stream Attribute Packet has the *PDF* field in the Tunneled Packet Header set to 3. The Main Stream Attribute Packet is used by a DP IN Adapter to transmit the display mode attributes once per frame during the vertical blanking period. It is identified by the presence of two Secondary Start (SS) control symbols on each lane of the Main-Link.

A Main Stream Attribute Packet shall consist of an MSA Header followed by packet payload. The packet payload shall contain the encoding of the 36-byte attribute information following the <SS, SS> control symbol pair. The MSA Header format is shown in Figure 10-31.

Figure 10-31. MSA Header Format



The fields forming an MSA Header shall be as defined below:

- **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the MSA Header. See Section 5.1.2.3 for calculation.
- **Fill Count [24:8]**: This field shall contain the fill count as defined in Section 10.5.1.5.
- **Reserved [31:25]**: Reserved.

Figure 10-32. MSA Packet Format

4 Lanes – DP Main Link					2 Lanes – DP Main Link						
31				0	31				0		
PDF = 3	*	Rsvd	HopID	Length = 28h	HEC	PDF = 3	*	Rsvd	HopID	Length = 28h	HEC
MSA Header					MSA Header						
Mvid 23:16		Mvid 23:16		Mvid 23:16	Mvid 23:16	Mvid 23:16		Mvid 23:16		Mvid 15:8	Mvid 15:8
Mvid 15:8		Mvid 15:8		Mvid 15:8	Mvid 15:8	Mvid 7:0		Mvid 7:0		Htotal 15:8	Hstart 15:8
Mvid 7:0		Mvid 7:0		Mvid 7:0	Mvid 7:0	Htotal 7:0		Hstart 7:0		Vtotal 15:8	Vstart 15:8
Htotal 15:8		Hstart 15:8		Hwidth 15:8	Nvid 23:16	Vtotal 7:0		Vstart 7:0		HSP, HSW 14:8	VSP, VSW 14:8
Htotal 7:0		Hstart 7:0		Hwidth 7:0	Nvid 15:8	HSW 7:0		VSW 7:0		Mvid 23:16	Mvid 23:16
Vtotal 15:8		Vstart 15:8		Vheight 15:8	Nvid 7:0	Mvid 15:8		Mvid 15:8		Mvid 7:0	Mvid 7:0
Vtotal 7:0		Vstart 7:0		Vheight 7:0	MISC0 7:0	Hwidth 15:8		Nvid 23:16		Hwidth 7:0	Nvid 15:8
HSP, HSW 14:8		VSP, VSW 14:8		0	MISC1 7:0	Vheight 15:8		Nvid 7:0		Vheight 7:0	MISC0 7:0
HSW 7:0		VSW 7:0		0	0	0		MISC1 7:0		0	0

1 Lane – DP Main Link					
31				0	
PDF = 3	*	Rsvd	HopID	Length = 28h	HEC
MSA Header					
Mvid 23:16		Mvid 15:8		Mvid 7:0	Htotal 15:8
Htotal 7:0		Vtotal 15:8		Vtotal 7:0	HSP, HSW 14:8
HSW 7:0		Mvid 23:16		Mvid 15:8	Mvid 7:0
Hstart 15:8		Hstart 7:0		Vstart 15:8	Vstart 7:0
VSP, VSW 14:8		VSW 7:0		Mvid 23:16	Mvid 15:8
Mvid 7:0		Hwidth 15:8		Hwidth 7:0	Vheight 15:8
Vheight 7:0		0		0	Mvid 23:16
Mvid 15:8		Mvid 7:0		Nvid 23:16	Nvid 15:8
Nvid 7:0		MISC0 7:0		MISC1 7:0	0

* SupplID

* SupplID

Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following:

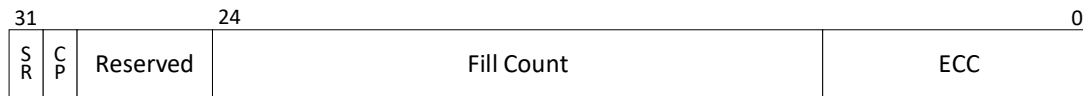
- Verify the *ECC* field in the MSA Header. If an uncorrectable error has occurred, the Main Stream Attribute Packet shall be dropped and ignored.
- Send Fill Count number of Stuffing Symbols on all lanes of the DP Main-Link according to Section 10.5.1.5.
- Send the control symbol pair <SS, SS> on all lanes of the DP Main-Link.
- Send the stream attribute information contained in the first 36 bytes of the payload of the Main Stream Attribute Packet by steering bytes from the payload onto the lanes of the DP Main-Link in a round robin fashion starting with lane 0.
- Send the control symbol <SE> on all lanes of the DP Main-Link.

10.5.1.3 Blank Start Packet

The Blank Start Packet has the *PDF* field in the Tunneled Packet Header set to 2. It used by a DP IN Adapter to indicate the beginning of a horizontal or vertical blanking period, reset scrambler and transfer control information at the beginning of a blanking period. A Blank Start Packet

shall consist of a Blank Start Header followed by packet payload. The packet payload shall contain the encoding of all 4 sets of <VB-ID, Mvid 7:0, Maud 7:0>. The Blank Start Header format is shown in Figure 10-33.

Figure 10-33. Blank Start Header Format



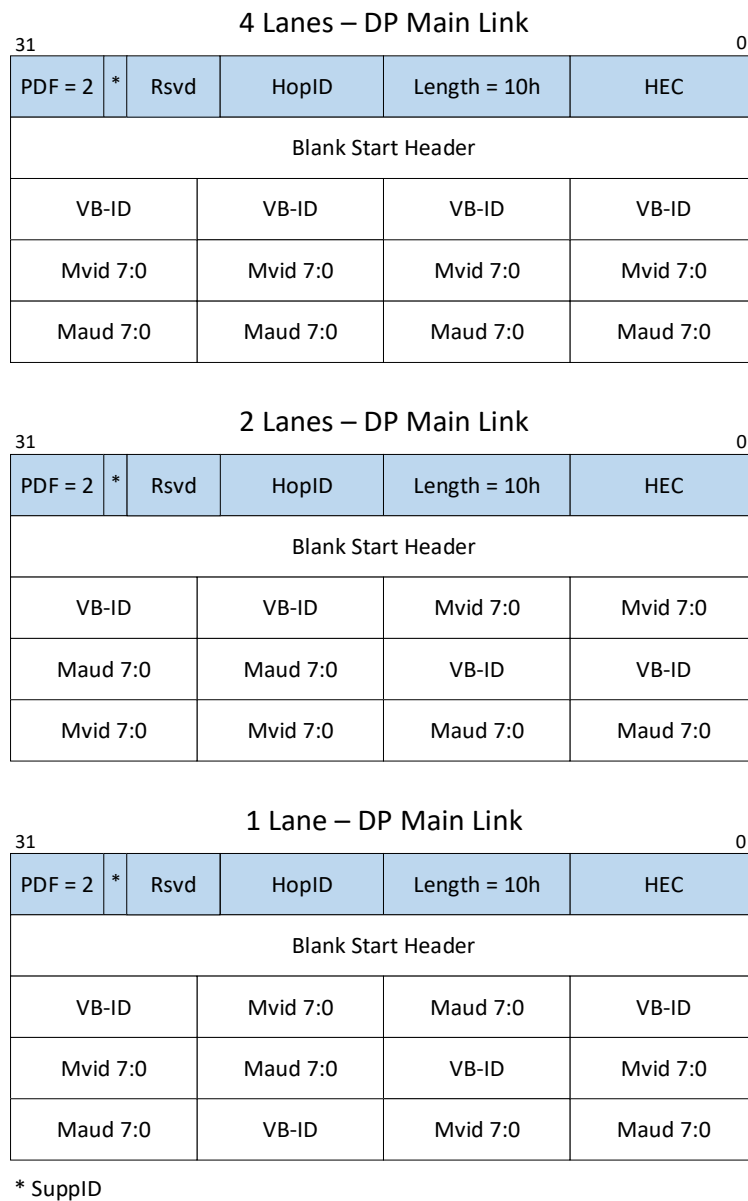
The fields forming the Blank Start Header shall be as defined below:

- **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the Blank Start Header. See Section 5.1.2.3 for calculation.
- **Fill Count [24:8]**: This field shall have the value as defined in Section 10.5.1.5.
- **Reserved [29:25]**: Reserved.
- **CP [30]**: Content Protection Flag shall be set to 1b if Blank Start DP Control Link Symbols sequence were <BS,CP,CP,BS> or <SR,CP,CP,SR>.
- **SR [31]**: Scrambler Reset Flag shall be set to 1b if Blank Start DP Control Link Symbols sequence were <SR,BF,BF,SR> or <SR,CP,CP,SR>.

Figure 10-34 shows the 12-byte encoding for the three different lane configurations. The packet payload is created by interleaving the control information carried on the lanes of the DP Main-Link one symbol at a time starting with lane 0 of the DP Main-Link.

Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations:

1. Verify the *ECC* field at the Blank Start Header. If an uncorrectable error has occurred, the Blank Start Packet shall be dropped.
2. Generate Stuffing Symbols on each lane of the DP Main-Link according to the *Fill Count* field in the Blank Start Header and Section 10.5.1.5.
3. Generate control symbols on each lane of the DP Main-Link marking the start of the blanking period based on the *SR Flag* and *CP Flag* as shown in Table 10-15.
4. Steer the three double-words of Blank Start Packet payload starting with the first double-word onto the Main-Link by interleaving a byte at a time onto the lanes of the DP Main-Link starting with lane 0.

Figure 10-34. Blank Start Packet Format**Table 10-15. Blank Start Control Link Symbols Mapping**

SR	CP	Blank Start Control Link Symbols Sequence
0	0	<BS, BF, BF, BS>
0	1	<BS, CP, CP, BS>
1	0	<SR, BF, BF, SR>
1	1	<SR, CP, CP, SR>

10.5.1.4 Secondary Data Packet

The DisplayPort Secondary-Data Packet (SDP) is used to carry secondary data embedded within the DisplayPort stream during the horizontal or vertical blanking period. The start of an SDP is identified by the presence of a single SS control symbol on each lane of the DP-Main Link. The end of an SDP is identified by the presence of a single SE control symbol.

10.5.1.4.1 Secondary Transfer Unit

A DP IN Adapter shall pack secondary data into one or more Secondary TUs. The method for splitting secondary data into Multiple TUs is described in Section 10.5.1.4.3. A Secondary TU is created by selecting a symbol from each lane of the DP Main-Link in a cyclic way, starting with lane 0. The packing of secondary data into a Secondary TU for a 4-Lane, 2-Lane and 1-Lane configuration are done the same as for TU Set shown in Figure 10-25, Figure 10-26, and Figure 10-27 respectively. Each Secondary TU shall be prepended with a Secondary TU Header. Figure 10-35 shows the format for a Secondary TU Header. The fields forming the Secondary TU Header shall be as defined below:

- **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the Secondary TU Header. See Section 5.1.2.3 for calculation.
- **Secondary Count [13:8]**: This field shall contain the number of secondary data symbols per lane. A value of zero represent 64 if ND bit equals 0. The total number of secondary data symbols in the Secondary TU is equal to (Secondary Count * Number of Lanes).
- **Fill Count [27:14]**: This field shall have the value as defined in Section 10.5.1.5. When both the *NSS* and *NSE* fields are 0b, the *Fill Count* field is extended by one bit and is constructed as {EFC, Fill Count} where EFC is the most significant bit.
- **L [Bit 28]**: Last TU Flag. This flag shall be set to 1b if the Secondary TU is either the last TU before a split or the TU represents the Secondary End Symbol. Otherwise it shall be set to 0b. See Section 10.5.1.4.4 for details.
- **NSE [Bit 29]**: No Secondary End. This bit shall be set to 1b if Last TU Flag is set to 1b and a Secondary End Control symbol is not present at the DP Main-Link. Otherwise it shall be set to 0b.
- **NSS [Bit 30]**: No Secondary Start. This bit shall be set to 1b if this is the first Secondary TU after a non-Secondary Tunneled Packet and a Secondary Start Control symbol is not present at the DP Main-Link. Otherwise it shall be set to 0b. See Section 10.5.1.4.3 for details.
- **EFC/ND [31]**: Extended Fill Count/No Data. This bit shall be set to 1b if the Secondary TU does not have any Secondary data.
 - **EFC**: When both the *NSS* and *NSE* fields are 0b, this bit is used as an extension to the *Fill Count* field.
 - **ND**: When either the *NSS* or *NSE* fields are 1b, this bit is used to indicate whether the Secondary TU has any Secondary data. This bit shall be set to 1b if the Secondary TU does not contain Secondary data. If the Secondary TU contains Secondary data, this bit shall be set to 0b.

Figure 10-35. Secondary TU Header Format

A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases:

- A single Secondary Start Control symbol <SS> is present on the DP Main-Link.
- The previous Secondary TU has reached the maximum capacity and the secondary data continues.
- The secondary data is split (as defined by the DisplayPort Specification) by a non-Secondary Data Packet and this packet has now ended.

A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases:

- Secondary End Control symbol <SE> is present on the DP Main-Link.
- Maximum capacity is reached:
 - For 1-Lane and 2-Lanes links: maximum capacity is reached when the *Secondary Count* field is 64.
 - For 4-Lane links: maximum capacity is reached when the *Secondary Count* field is 62.
- Secondary data stream was split by MSA, BS or Active video as defined in the DisplayPort Specification.

Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU:

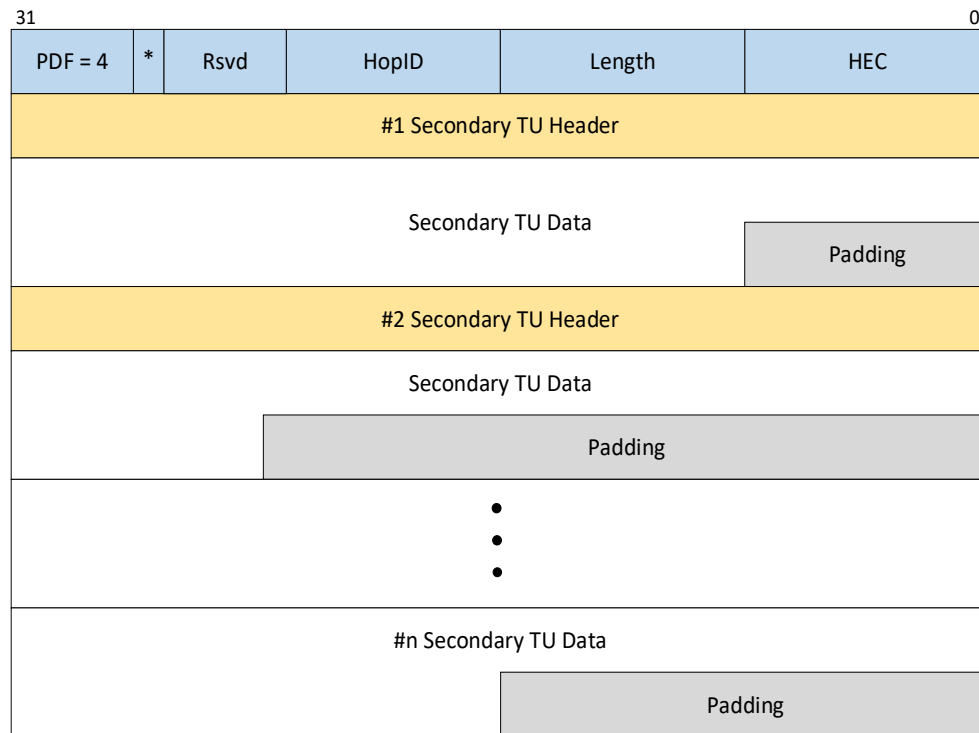
1. Verify the *ECC* field in the Secondary TU Header. If an uncorrectable error has occurred, the whole Secondary TU and the subsequent TUs within that packet shall be dropped and ignored.
2. Send Fill Count number of Stuffing Symbols on all lanes of the DP Main-Link according to Section 10.5.1.5.
3. If this Secondary TU is the first Secondary TU to follow a non-Secondary Data Packet and the *NSS* bit is not set in the Secondary TU Header, send the control symbol <SS> on all lanes of the DP Main-Link.
4. Send the secondary data contained in the Secondary TU.
 - a. The number of cycles of data shall be as according to the *Secondary Count* field in the Secondary TU Header.
 - b. The secondary data shall be sent on the DP Main-Link by steering bytes from the payload onto the lanes in a round robin fashion starting with lane 0.
5. If the *L Flag* is set and the *NSE* bit is not set in the Secondary TU Header, send the control symbol <SE> on all lanes of the DP Main-Link.

Note: DisplayPort Tunneling does not support the case where an SS symbol of an SDP Split is preceded by more than 15860 cycles of dummy symbols.

10.5.1.4.2 Packet Format

A Tunneled Secondary Data Packet has the *PDF* field in the Tunneled Packet Header set to 4. A Tunneled Secondary Data Packet shall have the format shown in Figure 10-36. As shown in Figure 10-36, the first 4 bytes of the Tunneled Secondary Data Packet payload contain the first Secondary TU Header, followed by the first Secondary TU payload. Additional Secondary TUs can only be added to the payload of the Tunneled Secondary Data Packet if the whole Secondary TU fits in the payload. A Tunneled Secondary Data Packet shall not include Secondary TUs from more than one DisplayPort SDP. It is recommended that a Tunneled Secondary Data Packet include as many Secondary TUs as possible in order to reduce overhead on the USB4 Fabric.

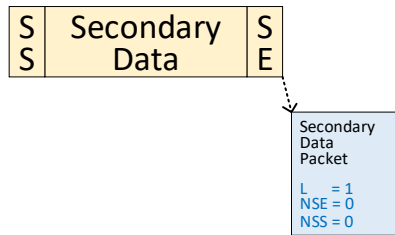
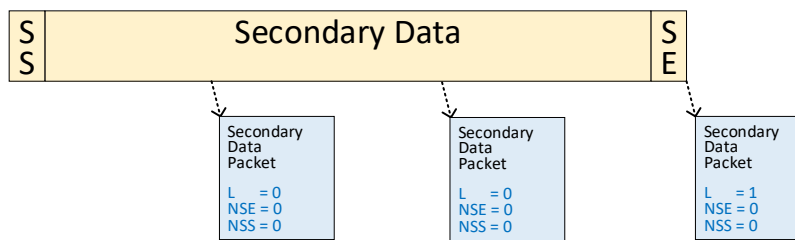
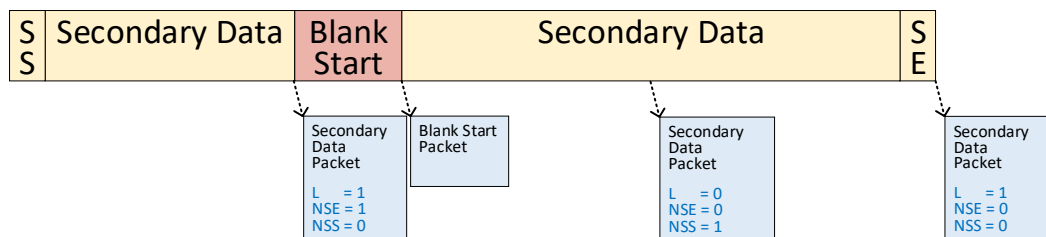
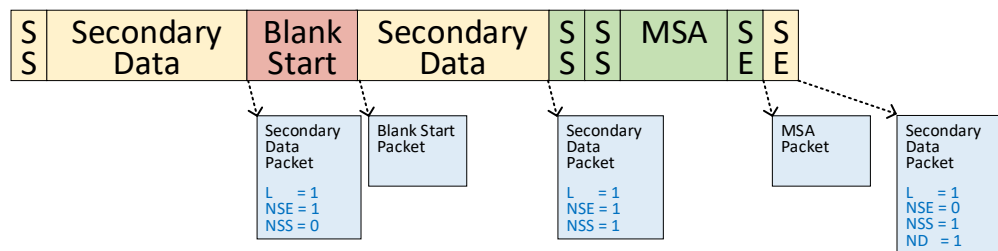
All Secondary TU Headers within the Tunneled Secondary Data Packet payload shall be aligned to 32-bits by adding Secondary TU Padding bytes at the end of the Secondary TU payload if necessary. Secondary TU Padding bytes values are don't care. The length of all Secondary TU Padding is included when calculating the *Length* field in the Tunneled Packet Header.

Figure 10-36. Tunneled Secondary Data Path Format

* SupplD

10.5.1.4.3 Secondary Data to Secondary TU Mapping Examples

Secondary data may be packed into several Secondary TUs depending on the secondary data length, the DP Main-Link lane count, and whether the secondary data is split by a non-Secondary Data Packet. Figure 10-37 shows several examples of packing the secondary data into Secondary TUs and the corresponding control bits in the Secondary TU Header.

Figure 10-37. Secondary Data to Secondary TUs Examples**A. Secondary Data to Single Secondary TU****B. Secondary Data to three Secondary TUs due to Max Capacity reach****C. Secondary Data to three Secondary TUs due to single Split and Max Capacity reach****D. Secondary Data to three Secondary TUs due to two Splits****10.5.1.5 Fill Count**

Every Tunneled Packet or TU that carries data from the SST Main-Link Path, contains a *Fill Count* field. The *Fill Count* field represents the number of DP link clock cycles between two adjacent packets over the DisplayPort Main-Link. The *Fill Count* field is an unsigned integer. Setting all bits to 1 in the *Fill Count* field is a special marking for the minimal value of -1.

Note: The term “previous packet” within this section refers to the previous packet or the previous TU within the same Tunneled Packet.

DP IN Adapter shall calculate the *Fill Count* field according to the following formula:

$$\text{Fill Count field} = \text{Act_Fill_Count} + \text{DP_K_Prev_Pkt} - \text{Prev_Factor}$$

where:

- Act_Fill_Count is the count of DP Link clock cycles between the previous packet and the current packet. The following cycles shall be counted as the Act_Fill_Count:
 - Stuffing Symbols.
 - BE – Blanking End.
 - FS – Filling Start.
 - FE – Filling End.
- DP_K_Prev_Pkt is the number of DP Link clock cycles which carried DP Control Link Symbols in the previous packet. DP Control Link Symbols which are counted in the Act_Fill_Count are not to be counted for this attribute.
 - EOC Control Link Symbol is treated as data, and not counted for the DP_K_Prev_Pkt attribute.
- Prev_Factor is an adjustment factor which is based on the previous packet type and sub type as appear in Table 10-16.

Table 10-16. Fill Count Prev_Factor

Previous Packet	Prev_Factor
Main Stream	3
Blank Start	1
Video TU	0
Secondary(NSS = 0 ; NSE = 0 ; L = 0)	0
Secondary(NSS = 0 ; NSE = 0 ; L = 1)	2
Secondary(NSS = 0 ; NSE = 1 ; L = 0)	NA
Secondary(NSS = 0 ; NSE = 1 ; L = 1)	1
Secondary(NSS = 1 ; NSE = 0 ; L = 0)	-1
Secondary(NSS = 1 ; NSE = 0 ; L = 1)	1
Secondary(NSS = 1 ; NSE = 1 ; L = 0)	NA
Secondary(NSS = 1 ; NSE = 1 ; L = 1)	0

A DP OUT Adapter shall use the following formula to calculate the actual number of Stuffing Symbols to be driven over the DP link:

$$\text{Act_Fill_Count} = \text{Fill Count field} + \text{Prev_Factor} - \text{DP_K_Prev_Pkt}$$

Figure 10-38 and Figure 10-39 show examples of *Fill Count* field calculations.

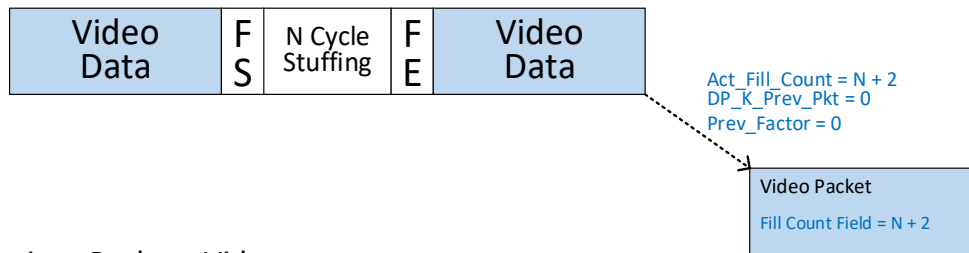
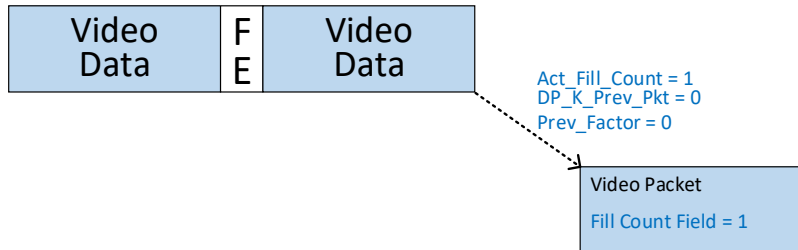
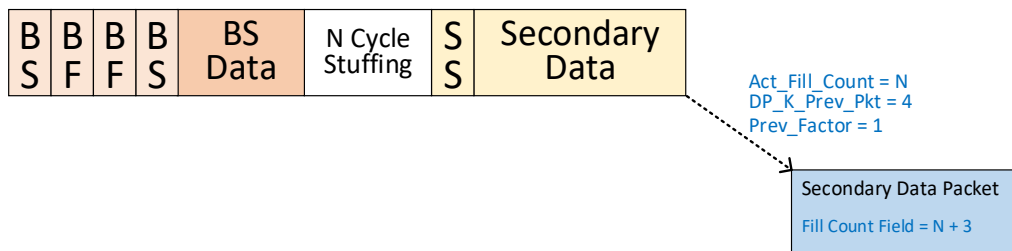
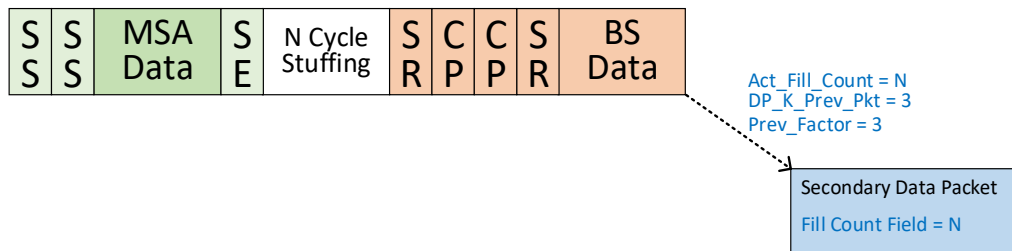
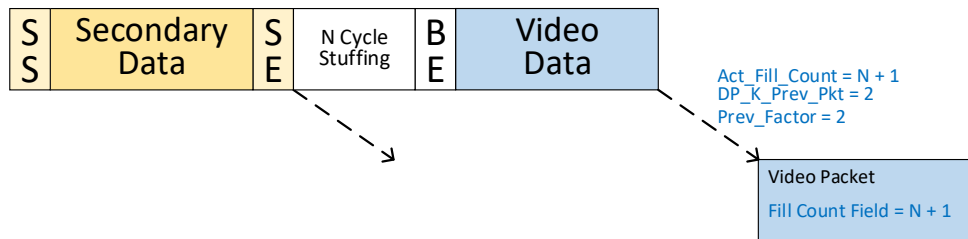
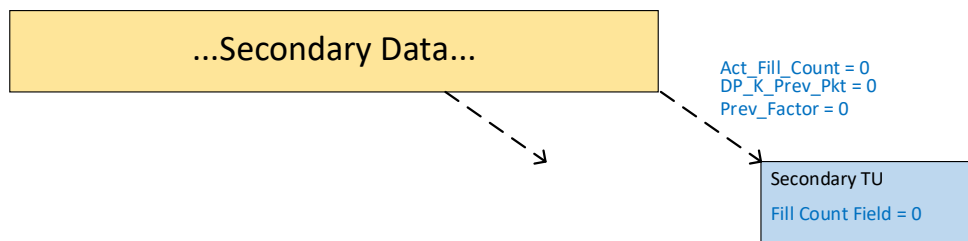
Figure 10-38. Non-Secondary Data Packet Fill Count Examples**A. Previous Packet - Video****B. Previous Packet - Video****D. Previous Packet – Blank Start****E. Previous Packet - MSA**

Figure 10-39. Secondary Data Packet Fill Count Examples

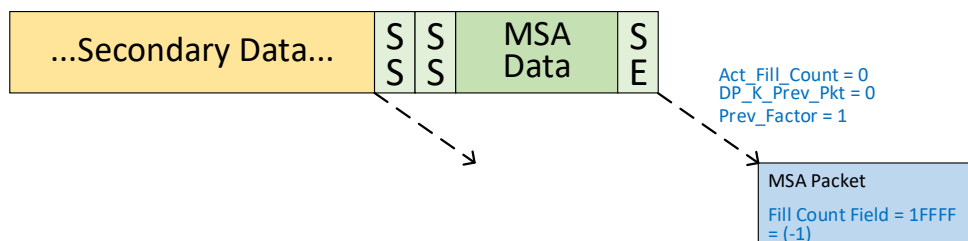
A. Secondary TU: L = 1 ; NSE = 0 ; NSS = 0



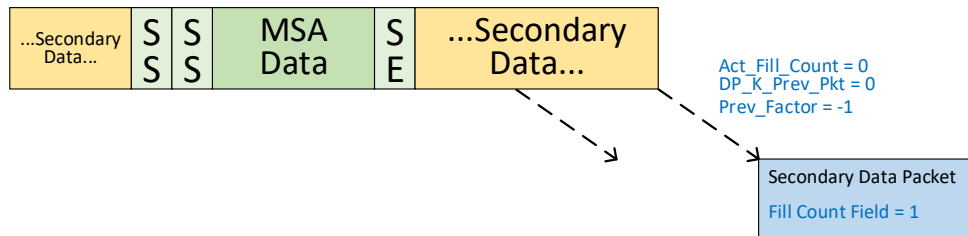
B. Secondary TU: L = 0 ; NSE = 0 ; NSS = 0



C. Secondary TU: L = 1 ; NSE = 1 ; NSS = 0



D. Secondary TU: L = 0 ; NSE = 0 ; NSS = 1



A DP IN Adapter may put any value in the *Fill Count* field in the first Tunneled Packet sent on the Main-Link Path after link training and after waking from an ALPM low power state. A DP OUT Adapter shall ignore the *Fill Count* field in the first Tunneled Packet sent on the Main-Link Path after DP link training and after waking from an ALPM low power state.

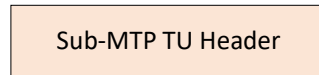
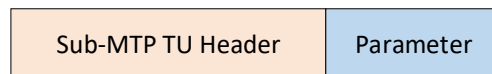
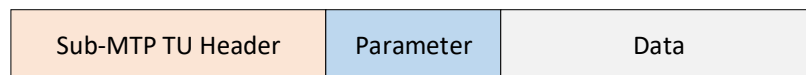
10.5.2 8b/10b MST Tunneling

The MST Link is built out of continually transported Multi Stream Transport Packets (MTP). An MTP is 64 link symbol cycles (i.e. 64 time slots) long. An MTP starts with an MTP Header in the first time slot (i.e. Time Slot 0).

MTPs are broken up into Sub-MTP Transfers Units before being encapsulated in Tunneled Packets. A DP IN Adapter converts each MTP into one or more Sub-MTP TU. A DP OUT Adapter recreates MTPs out of the Sub-MTP TUs.

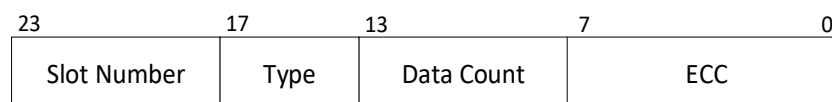
10.5.2.1 Sub-MTP TU

A Sub-MTP TU holds part of an MTP. A Sub-MTP TU consists of a header and optionally Parameter and/or Data bytes. Figure 10-40 shows the possible Sub-MTP TU structures.

Figure 10-40. Sub-MTP TU Structures**A. Header Only****B. Header and Parameter****C. Header and Data****D. Header, Parameter and Data**

A Sub-MTP TU Header shall have the format shown in Figure 10-41. The fields forming the Sub-MTP TU Header shall be as defined below:

- **ECC [7:0]**: Error correction field that is calculated over bits [23:8] of the Sub-MTP TU Header. See Section 5.1.2.3 for calculation.
- **Data Count[13:8]**: This field shall contain the number of Data Symbols per lane. The total number of Data Symbols in the Sub-MTP TU is equal to (*Data Count* * Number of Lanes).
- **Type[17:14]**: This field shall contain the Type encoding of the Sub-MTP TU. The Type encodings are defined in Table 10-17 for slot zero and in Table 10-18 for non-zero slots.
- **Slot Number[23:18]**: This field shall contain the first slot number in the MTP which this Sub-MTP TU Header is describing.

Figure 10-41. Sub-MTP TU Header Format**Table 10-17. Slot Zero Sub-MTP TU Header Types**

Header Name	Type Encoding [17:14]	Data Count	Valid for # Lanes in DP-Main Link
MTPH	0	0-63	1, 2, 4
SR MTPH	1	0-63	1, 2, 4

Header Name	Type Encoding [17:14]	Data Count	Valid for # Lanes in DP-Main Link
1 Data MTPH	3	0-63	1, 2, 4
2 Data MTPH	4	0-63	2
4 Data MTPH	5	0-63	4
1 K-Symbol MTPH	8	0-63	1, 2, 4
2 K-Symbol MTPH	9	0-63	2
4 K-Symbol MTPH	11	0-63	4
Corrupt	12	0	1, 2, 4

Table 10-18. Non-Slot Zero Sub-MTP TU Header Types

Header Name	Type Encoding [17:14]	Data Count	Valid for # Lanes in DP-Main Link
Data	0	1-63	1, 2, 4
Shifting SR	1	0-63	1, 2, 4
BS	2	0-63	1, 2, 4
BE	3	0-63	1, 2, 4
SS	4	0-63	1, 2, 4
SE	5	0-63	1, 2, 4
SF	6	0	1, 2, 4
VCPF	7	0	1, 2, 4
1 K-Symbol	8	0-63	1
2 K-Symbol	9	0-63	1, 2
3 K-Symbol	10	0-63	1
4 K-Symbol	11	0-63	1, 2, 4
Corrupt	12	0	1, 2, 4
AVF (Active Video Filling)	14	0	1, 2, 4
EOC	13	0-63	1, 2, 4
Unallocated	15	0	1, 2, 4

A DP IN Adapter that receives an MST stream shall perform the DisplayPort PHY layer and De-scrambler functions defined in the DisplayPort Specification.

Upon reception of the first SR after link training completion, a DP IN Adapter shall:

- Track the total number of allocated MST slots by snooping any DPCD AUX transactions that configure the VC Payload ID Table.
- Start mapping MTP from the DP Main-Link into Sub-MTP TUs.

Mapping an MTP to Sub-MTP TUs consists of determining the appropriate header, then appending any Parameter and/or Data bytes. For slot zero, Table 10-19 describes when each Sub-MTP TU Header type is used and what Parameter bytes (if any) are included. For non-zero slots, Table 10-20 describes when each Sub-MTP TU Header type is used and what Parameter bytes (if any) are included.

Table 10-19. Slot Zero Sub-MTP TU Packet Rules

Header Name	Parameter Bytes	Parameter Contents	Conditions When Used
MTPH	0	N/A	Data Symbol equal 00h is present on all active lanes.
SR MTPH	0	N/A	SR Control symbol is present on all active lanes.
1 Data MTPH	1	Byte 0 = Dx	The same Data Symbol (Dx) which is not equal to 00h, is present on all active lanes.
2 Data MTPH	2	Byte 0 = Dx0 Byte 1 = Dx1	Two different Data Symbols, Dx0 and Dx1 are present on lanes 0 and 1 respectively.
4 Data MTPH	4	Byte 0 = Dx0 Byte 1 = Dx1 Byte 2 = Dx2 Byte 3 = Dx3	One or more Data Symbols are not the same across all 4 lanes (Dx0, Dx1, Dx2, Dx3 are present on lanes 0, 1, 2 and 3 respectively).
1 K-Symbol MTPH	1	lower nibble = x upper nibble = 0h	The same K-Symbol Index (Cx) is present on all active lanes.
2 K-Symbol MTPH	1	lower nibble = x0 upper nibble = x1	Two different K-Symbols Indexes, Cx0 and Cx1 are present on lanes 0 and 1 respectively.
4 K-Symbol MTPH	2	Byte 0: lower nibble = x0 upper nibble = x1 Byte 1: lower nibble = x2 upper nibble = x3	One or more K-Symbol Indexes are not the same across all 4 lanes (Cx0, Cx1, Cx2 and Cx3 are present on lanes 0, 1, 2 and 3 respectively).
Corrupt	0	N/A	Either Data and K-Symbols are present for the same slot, or an error indication from the DP PHY Layer is present that cannot be resolved using majority voting as defined in the DisplayPort Specification.

Table 10-20. Non-Zero Slot Sub-MTP TU Packet Rules

Header Name	Parameter Bytes	Parameter Contents	Conditions When Used
Data	0	N/A	The slot is allocated and has Data Symbols on all active lanes.
Shifting SR	0	N/A	An SR Control symbol is present on all active lanes for the 4th time as described in Section 10.5.2.2.2.
BS	0	N/A	The BS Control Link Symbol Sequence C0-C0-C0-C0 is present in full.
BE	0	N/A	The BE Control Link Symbol Sequence C1-C1-C1-C1 is present in full.
SS	0	N/A	The SS Control Link Symbol Sequence C3-C3-C3-C3 is present in full.
SE	0	N/A	The SE Control Link Symbol Sequence C6-C6-C6-C6 is present in full.
SF	0	N/A	The SF Control Link Symbol Sequence C4-C4-C4-C4 is present in full and the last Sub-MTP TU Header sent was a VCPF or an AVF.
VCPF	0	N/A	The VCPF Control Link Symbol Sequence C0-C1-C2-C3 is present in full.

Header Name	Parameter Bytes	Parameter Contents	Conditions When Used
AVF	0	N/A	The DP IN Adapter supports Panel Replay Optimization and the Active Video Fill Control Link Symbol Sequence, C7-C7-C7-C7, is present in full.
1 K-Symbol	1	lower nibble = x upper nibble = 0h	A K-Symbol Index (Cx) is followed by either a non-K-Symbol ¹ or slot zero.
2 K-Symbol	1	lower nibble = x0 upper nibble = x1	Two K-Symbols Indexes (Cx0 and Cx1) are followed by either a non K-Symbol ¹ or slot zero.
3 K-Symbol	2	Byte 0: lower nibble = x0 upper nibble = x1 Byte 1: lower nibble = x2 upper nibble = 0h	Three K-Symbols Indexes (Cx0, Cx1 and Cx2) are followed by either a non-K-Symbol ¹ or slot zero.
4 K-Symbol	2	Byte 0: lower nibble = x0 upper nibble = x1 Byte 1: lower nibble = x2 upper nibble = x3	Four K-Symbol Indexes (Cx0, Cx1, Cx2 and Cx3) are present that do not match Types 2 to 7, Type 13, or Type 14 when Panel Replay Optimization is enabled.
Corrupt	0	N/A	Either Data and K-Symbols are present for the same slot or an error indication from the DP PHY Layer is present and cannot be resolved using majority voting as defined in the DisplayPort Specification.
EOC	0	N/A	The EOC Control Link Symbol Sequence (C2-C2-C2) is present in full.
Unallocated	0	N/A	Slot is the first Unallocated slot for this MTP.
Notes:			
1. An unallocated slot is considered a “non-K-Symbol”.			

When a Parameter includes a Data byte, the DP IN Adapter shall append the de-scrambled Data byte as the Parameter. For a K-Symbol, the nibble describing the index is equal to the de-scrambled Index in case of C0-C7 Symbols and equal to 8 in case of an SR, as described in Table 10-21.

Table 10-21. K-Code Index Nibble in Parameter Byte

Symbol	Index Nibble
C0	0
C1	1
C2	2
C3	3
C4	4
C5	5
C6	6
C7	7

A DP IN Adapter shall pack the Data bytes by selecting a byte from each Lane of the Main-Link in a cyclic way, starting with lane 0. The packing of Data bytes into a Sub-MTP TU for a 4-Lane, 2-

Lane and 1-Lane configuration are shown in Figure 10-42, Figure 10-43, and Figure 10-44 respectively. The figures use an MTP with 1 cycle of blank end followed by n slots of video data followed by unallocated slots to demonstrate packing.

A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU:

- A Sub-MTP TU is byte-aligned.
- The total length of a Sub-MTP TU (Header + Parameter Bytes + Data Bytes) does not exceed 252 Bytes.
- Slot 0 always starts a new Sub-MTP TU.
- A Sub-MTP TU includes data from one MTP only.
- A DP IN Adapter shall map an MTP into the minimum possible number of Sub-MTP TU
- A Sub-MTP TU shall be split into 2 Sub-MTP TUs if it does not fit into an MTP packet according to Section 10.5.2.3.
- Data from the same time slot is packed into a single Sub-MTP TU.

Figure 10-42. Sub-MTP TU 4-Lane Mapping

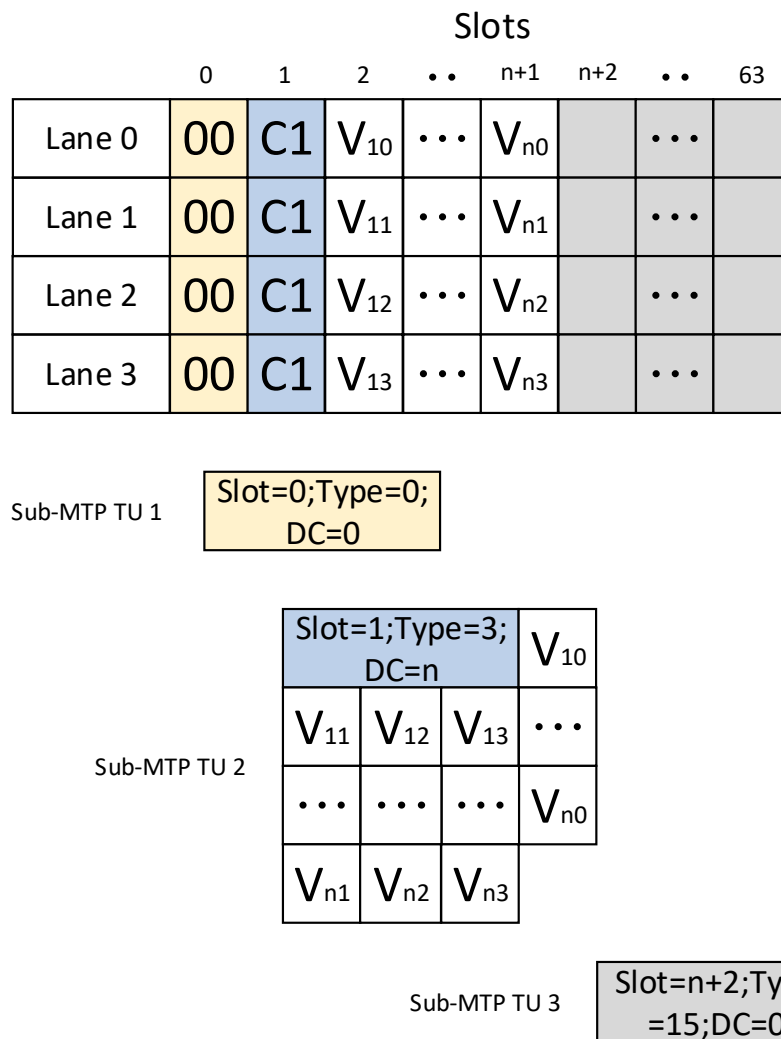


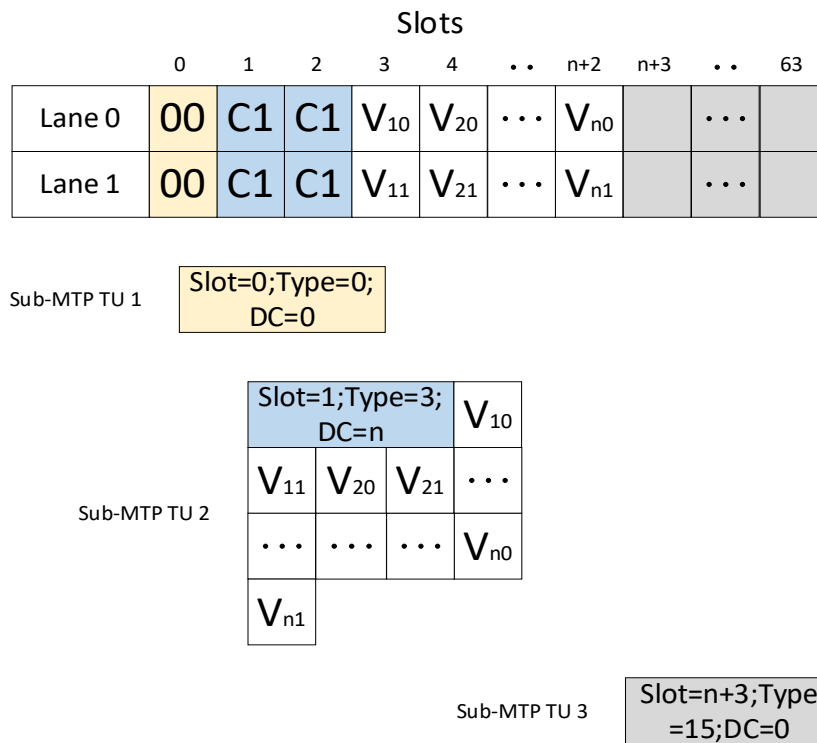
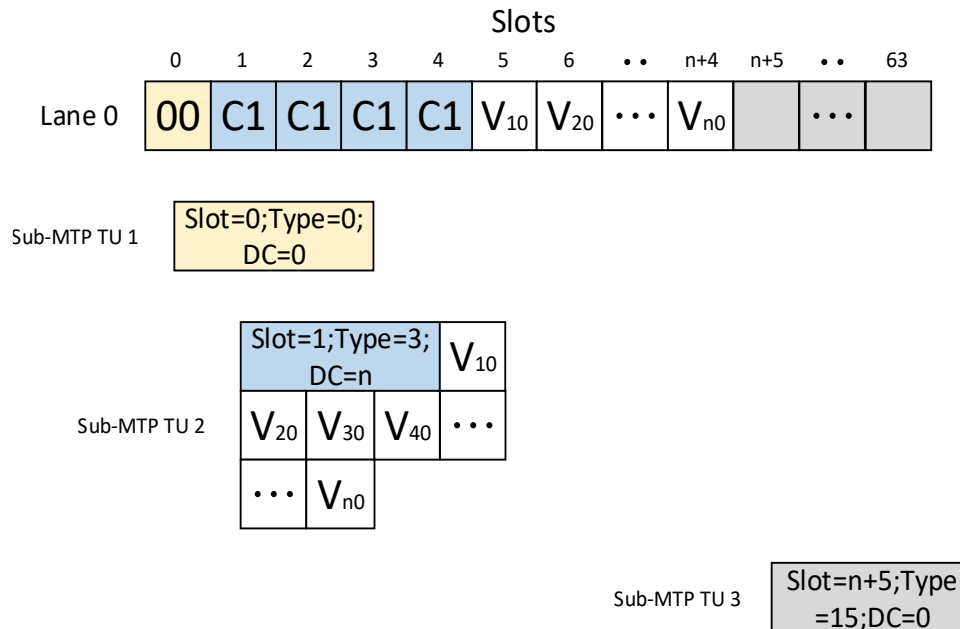
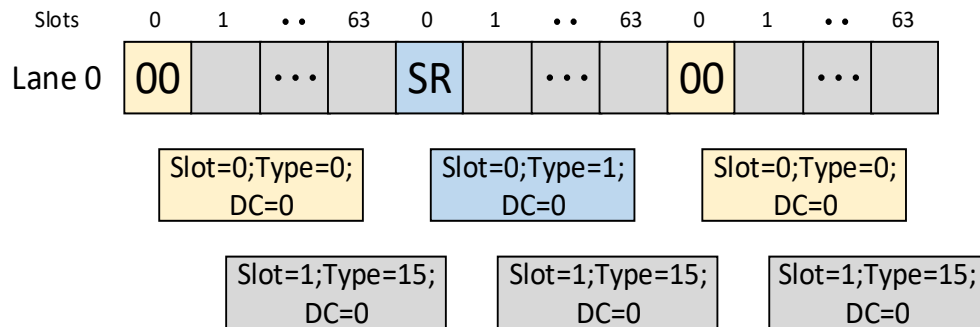
Figure 10-43. Sub-MTP TU 2-Lane Mapping**Figure 10-44. Sub-MTP TU 1-Lane Mapping****10.5.2.2 MTP to Sub-MTP TU Examples****10.5.2.2.1 No Allocation**

Figure 10-45 shows the 1-lane case where an MTP that has no allocated slots is mapped into two Sub-MTP TUs for both default MTPH and SR MTPH.

Figure 10-45. Unallocated Sequence, 1-Lane**10.5.2.2.2 Shifting SR**

The MST Link Timing Robustness section in the DisplayPort Specification requires that a DP IN Adapter ignore the appearance of SR at an unexpected time slot. Upon detecting a sequence of four consecutive SR with 2^{16} time-slot intervals, a DP IN Adapter shall switch to the new SR location. The first three SR that are not at Slot Zero's original location shall be mapped to a non-zero Slot Type 8 (1 K-Symbol), for the case of 1-lane, carrying Parameter byte = 8 (as defined in Table 10-20). The fourth SR shall be mapped to a non-zero Slot Type 1 (Shifting SR) forcing the next slot to be slot number 1. Figure 10-46 shows a 3rd and 4th SR in a 1-lane case of unallocated slots. For the case of 2-Lane DP links, the first three SR shall be mapped to Type 9 (2 K-Symbols). For the case of and 4-Lane DP links, the first three SR shall be mapped to Type 11 (4 K-Symbols).

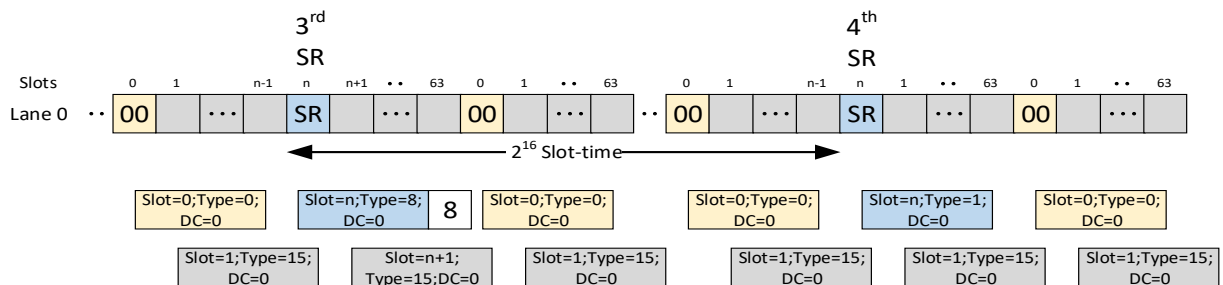
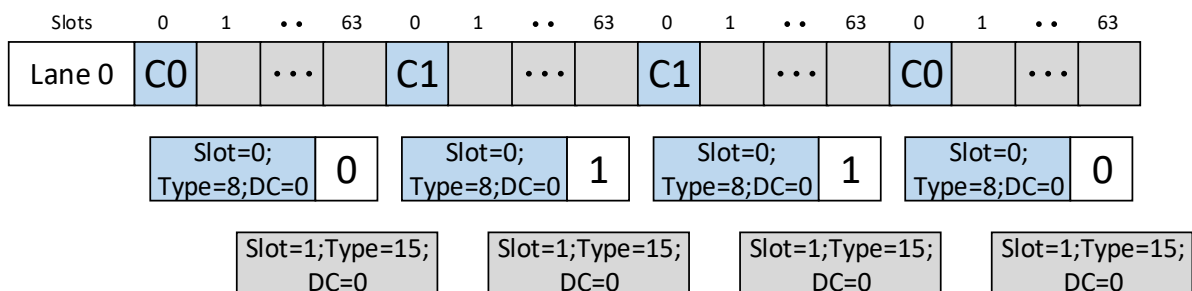
Figure 10-46. Shifting SR, 1-Lane**10.5.2.2.3 ACT**

Figure 10-47 shows the ACT sequence for a 1-lane case, where originally none of the slots are allocated.

Figure 10-47. ACT Sequence, 1-Lane

10.5.2.2.4 SF, AVF, and VCPF

A DP IN Adapter shall not map an SF sequence into a Sub-MTP TU unless the SF sequence comes immediately after a VCPF or an AVF sequence. Figure 10-48(A) shows the case where an SF sequence is present after Data Symbols, which results in no SF Sub-MTP TU. Figure 10-48(B) shows the case where a VCPF sequence is present after Data Symbols, which results in a one-time VCPF Sub-MTP TU. Figure 10-48(C) shows the case where a VCPF sequence is followed by SF sequence, which results a one-time VCPF Sub-MTP TU followed by one-time SF Sub-MTP TU. Figure 10-48(D) shows the case where an AVF sequence is present after Data Symbols, which results in a one-time AVF Sub-MTP TU.

Figure 10-48. SF, AVF and VCPF Sequences in 4-Lanes**A. SF only results No SF Sub-MTP TU**

Slots	0	1	2	3	..	n	n+1	..	63
Lane 0	00	V ₁₀	V ₂₀	C4	...	C4		...	
Lane 1	00	V ₁₁	V ₂₁	C4	...	C4		...	
Lane 2	00	V ₁₂	V ₂₂	C4	...	C4		...	
Lane 3	00	V ₁₃	V ₂₃	C4	...	C4		...	

Slot=0;Type=0; DC=2	V ₁₀			
V ₁₁	V ₁₂	V ₁₃	V ₂₀	
V ₂₁	V ₂₂	V ₂₃		

Slot=n+1; Type=15;DC=0				
---------------------------	--	--	--	--

B. VCPF only results VCPF Sub-MTP TU

Slots	0	1	2	3	..	n	n+1	..	63
Lane 0	00	V ₁₀	V ₂₀	C0	...	C0		...	
Lane 1	00	V ₁₁	V ₂₁	C1	...	C1		...	
Lane 2	00	V ₁₂	V ₂₂	C2	...	C2		...	
Lane 3	00	V ₁₃	V ₂₃	C3	...	C3		...	

Slot=0;Type=0; DC=2	V ₁₀			
V ₁₁	V ₁₂	V ₁₃	V ₂₀	
V ₂₁	V ₂₂	V ₂₃		

Slot=3;Type=7; DC=0				
------------------------	--	--	--	--

Slot=n+1; Type=15;DC=0				
---------------------------	--	--	--	--

C. VCPF followed by SF – VCPF and SF Sub-MTP TUs

Slots	0	1	2	3	..	m	m+1	..	n	n+1	..	63
Lane 0	00	V ₁₀	V ₂₀	C0	...	C0	C4	...	C4		...	
Lane 1	00	V ₁₁	V ₂₁	C1	...	C1	C4	...	C4		...	
Lane 2	00	V ₁₂	V ₂₂	C2	...	C2	C4	...	C4		...	
Lane 3	00	V ₁₃	V ₂₃	C3	...	C3	C4	...	C4		...	

Slot=0;Type=0; DC=2	V ₁₀			
V ₁₁	V ₁₂	V ₁₃	V ₂₀	
V ₂₁	V ₂₂	V ₂₃		

Slot=3;Type=7; DC=0				
------------------------	--	--	--	--

Slot=m+1; Type=6;DC=0				
--------------------------	--	--	--	--

Slot=n+1; Type=15;DC=0				
---------------------------	--	--	--	--

D. AVF only results AVF Sub-MTP TU

Slots	0	1	2	3	..	n	n+1	..	63
Lane 0	00	V ₁₀	V ₂₀	C7	...	C7		...	
Lane 1	00	V ₁₁	V ₂₁	C7	...	C7		...	
Lane 2	00	V ₁₂	V ₂₂	C7	...	C7		...	
Lane 3	00	V ₁₃	V ₂₃	C7	...	C7		...	

Slot=0;Type=0; DC=2	V ₁₀			
V ₁₁	V ₁₂	V ₁₃	V ₂₀	
V ₂₁	V ₂₂	V ₂₃		

Slot=3;Type=14; DC=0				
-------------------------	--	--	--	--

Slot=n+1; Type=15;DC=0				
---------------------------	--	--	--	--

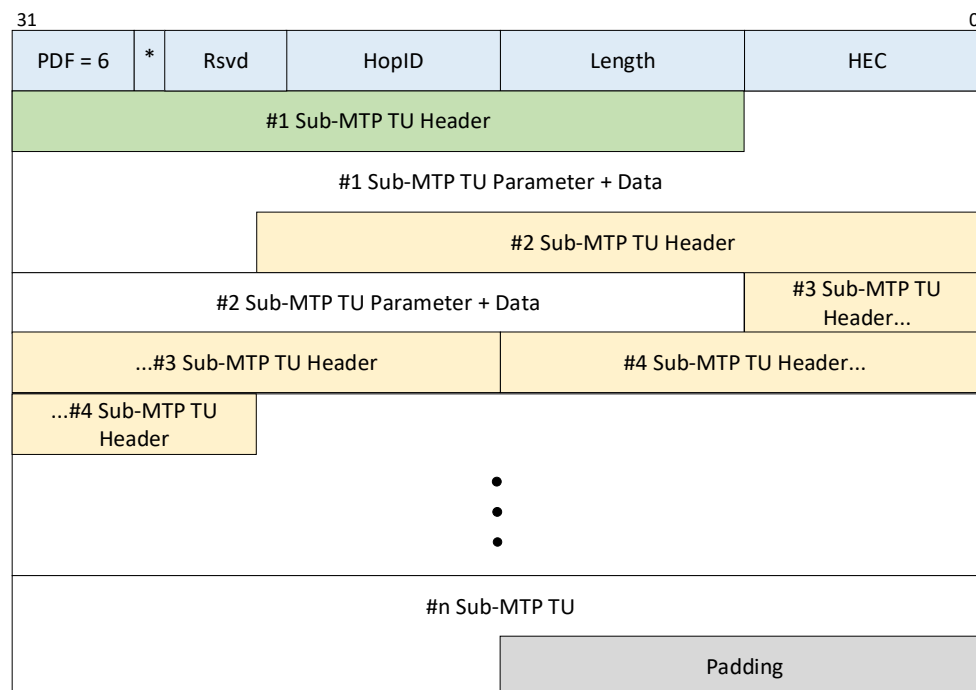
10.5.2.3 MST Packet Format

A DP IN Adapter uses an MST Packet to transport one or more Sub-MTP TUs. An MST Packet has the *PDF* field in the Tunneled Packet Header set to 6. An MST Packet shall have the format shown in Figure 10-49.

A DP IN Adapter shall follow the rules below when constructing an MST Packet:

- The first 3 bytes of the MST Packet payload contains the first Sub-MTP TU Header.
- When concatenating two Sub-MTP TUs, the first TU is not be padded.
- The number of consecutive time slots (both allocated and unallocated) described by the Tunneled Packet shall not exceed 1088 time slots. (1088 time slots is the equivalent of full 17 MTPs).
- The *Length* field in the Tunneled Packet Header does not include padding bytes.
- The Payload of the Tunneled Packet shall be between 230 and 252 Bytes (inclusive), unless the Payload contains the description of at least 960 time slots or it is the last MST Packet before entering ALPM.

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Figure 10-49. MST Packet Format

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10.5.2.4 MST Packets to DP MTP

A DP OUT Adapter receiving MST Packets from the USB4 Fabric recreates the DP MTP stream based on the Sub-MTP TUs included in the MST Packets and the slot number. A DP OUT Adapter is unaware of the number of allocated slots and each Sub-MTP TU parsing and handling is independent of the previous one. A DP OUT Adapter shall analyze each Sub-MTP TU Header and recreate the MTP K-Code and data bytes according to Table 10-17 (for slot zero) or Table 10-18 (for non-zero slots). If a DP OUT Adapter supports Panel Replay optimization, then the following exceptions apply when recreating the MTP K-Code and data bytes according to the incoming Sub-MTP TUs:

- If the Sub-MTP TU Header is AVF, a DP OUT Adapter shall insert dummy pixel data.
- If the Sub-MTP TU Header is either 1 K-Symbol, 2 K-Symbol, 3 K-Symbol or 4 K-Symbol, then for every K-Symbol index that equals 7, a DP OUT Adapter shall insert dummy pixel data.

If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below:

- If the last Sub-MTP TU Header was VCPF, insert VCPF.
- If the last Sub-MTP TU Header was AVF, insert dummy pixel data.
- If the last Sub-MTP TU Header was Unallocated, insert unallocated (data bytes equal zero).
- For all other cases, insert SF.

After creating the MTPs, the DP OUT Adapter shall follow all the PHY Layer functions required by the DisplayPort Specification.

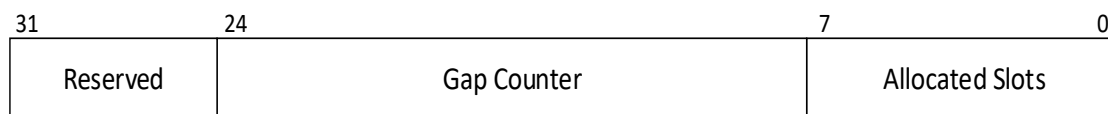
10.5.3 128b/132b Tunneling

A DP IN Adapter maps the DisplayPort 128b/132b Link Layer symbols into Tunneled Packets. A DP OUT Adapter reconstructs the DisplayPort 128b/132b Link Layer symbols from the Tunneled Packets it receives.

10.5.3.1 128b/132b LLCP Encapsulation

Upon reception of Link Layer Control Packet (LLCP) over the DisplayPort Main-Link, a DP IN Adapter shall send a 128b/132b LLCP Packet. A 128b/132b LLCP Packet has the *PDF* field in the Tunneled Packet Header set to 8h. A 128b/132b LLCP Packet shall consist of a 128b/132b LLCP Header followed by six DWs that contain the three LLCP Data Link Symbols that were received over the DisplayPort Main-Link. The 128b/132b LLCP Header format is shown in Figure 10-50. The 128b/132b LLCP Packet format is shown in Figure 10-51.

Figure 10-50. 128b/132b LLCP Header Packet Format



The fields forming a 128b/132b LLCP Header shall be as defined below:

- **Allocated Slots [7:0]:** The number of allocated time slots within each MTP in the Link Layer Frame associated with the LLCP.
- **Gap Counter [24:8]:** This field shall contain the number of 128b/132b Link Symbol Clocks between the first LLCP_MARKER symbol of the current LLCP and the first LLCP_MARKER symbol of the previous LLCP. Nominal Gap Counter should be 65540 (64 time slots x 1024 MTPs + 4 Cycles of LLCP).
 - The Gap Counter of the first LLCP Packet sent after link training shall be set to 0h.
 - The Gap Counter of the first LLCP Packet sent after an ALPM wake sequence shall be set to 0h.
 - The Gap Counter shall be set to 0x1FFFF if the count is greater than 0x1FFFF.

Note: Place Holder symbols are not counted by the Gap Counter.

- **Reserved [31:25]:** Reserved.

Figure 10-51. 128b/132b LLCP Packet Format

	31							0				
	PDF = 8		*	Rsvd		HopID		Length = 1Ch		HEC		
128b/132b LLCP Header	Reserved			Gap Counter					Allocated Slots			
Data Link Symbol 0	ECF[15:0]						Reserved			LL EI	H E I	A C T
Data Link Symbol 1	ECF[47:16]											
Data Link Symbol 2 – Lane 0	LVP – Lane 0						ECF[63:48]					
Data Link Symbol 2 – Lane 1	LVP – Lane 1						ECF[63:48]					
Data Link Symbol 2 – Lane 2	LVP – Lane 2						ECF[63:48]					
Data Link Symbol 2 – Lane 3	LVP – Lane 3						ECF[63:48]					

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The *ACT*, *HEI*, *LLEI*, and *ECF* fields are received four times per LLCP Packet, once per DisplayPort Link Layer lane. A DP IN Adapter may choose to encapsulate the value of a field from any of the DisplayPort Link Layer lanes, since the values for each of the above fields is identical on all of the four lanes. A DP IN Adapter shall map the *LVP* field received on the DisplayPort Link Layer lane *X* to the *LVP – Lane X* field, since the *LVP* field may be different for each DisplayPort Link Layer lane.

10.5.3.2 Time Slot Allocation

A DP IN Adapter tracks the total number of allocated time slots by snooping any DPCD AUX transactions that configure the VC Payload ID Table. The DP IN Adapter communicates the total number of allocated time slots to the DP OUT Adapter through the *Allocated Slots* field in the 128b/132b LLCP Packet.

Upon reception of an LLCP Packet with the *ACT* bit set to 1b over the DisplayPort Main-Link, a DP IN Adapter shall update the *Allocated Slots* field in the 128b/132b LLCP Header according to the snooped AUX transactions. If the *ACT* bit is set to 0b, a DP IN Adapter shall set the *Allocated Slots* field to the same value it sent in the previous LLCP Packet. If an LLCP Packet is the first received LLCP Packet and the *ACT* bit is set to 0b, a DP IN Adapter shall set the *Allocated Slots* field to 0h.

As defined in Section 10.5.3.3, upon reception of an LLCP Packet with the *Link Layer End Indicator (LLEI)* bit set to 1b over the DisplayPort Main-Link, a DP IN Adapter encapsulates the received MTPs as if the allocated time slots are set to 0. Upon reception of an LLCP Packet with the *Link Layer End Indicator* bit set to 0b over the DisplayPort Main-Link, a DP IN Adapter encapsulates the received MTPs according to the *Allocated Slots* field. A DP IN Adapter does not change the *Allocated Slots* field in the 128b/132b LLCP Header as a result of receiving an LLCP Packet with the *Link Layer End Indicator* bit set to 1b.

Upon reception of an LLCP Tunneled Packet with the *Link Layer End Indicator* bit set to 1b, a DP OUT Adapter reconstructs the MTPs over the DisplayPort Link as if the *Allocated Slots* field in the 128b/132b LLCP Header is set to 0h. Upon reception of an LLCP Tunneled Packet with the *Link Layer End Indicator* bit set to 0b, a DP OUT Adapter reconstruct the MTPs according to the *Allocated Slots* field in the 128b/132b LLCP Header.

10.5.3.3 128b/132b MTP Encapsulation

A DP IN Adapter maps the 128b/132b Link Layer MTPs based on the number of allocated time slots and on the received Control and Data Symbols:

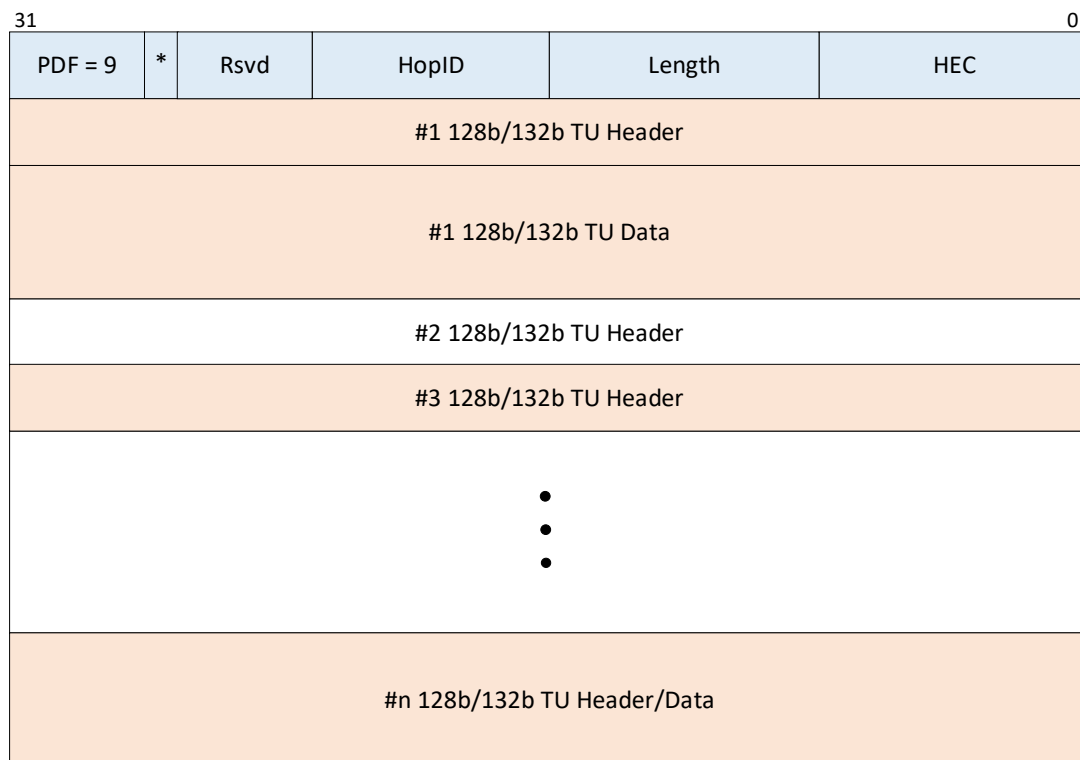
- When the number of allocated time slots is not zero and the last received *Link Layer End Indicator* bit was set to 0b:
 - A DP IN Adapter maps the 128b/132b Link Layer MTPs into two types of Tunneled Packets:
 - 128b/132b Control and Data Packet – Consists of Data Symbols and Control symbols. See Section 10.5.3.3.1.
 - 128b/132b Data Packet – Consists of Data Symbols only. See Section 10.5.3.3.2.
 - A DP IN Adapter shall pack the Data and Control symbols into a Tunneled Packet in the same order as received over the 128b/132b DisplayPort Link.
 - A DP IN Adapter shall pack the Data Link Symbols into a Tunneled Packet by selecting a Data Link Symbol from each Lane of the DP Main-Link in a cyclic way, starting with Lane 0.
- When the number of allocated time slots is zero or the last received *Link Layer End Indicator* bit was set to 1b, a DP IN Adapter shall not send 128b/132b Data Packet and 128b/132b Control and Data Packet.

10.5.3.3.1 128b/132b Control and Data Packet

A DP IN Adapter uses a 128b/132b Control and Data Packet to transport one or more 128b/132b Transfer Units (TU). A 128b/132b Control and Data Packet has the *PDF* field in the Tunneled Packet Header set to 9h. A 128b/132b Control and Data Packet shall have the format shown in Figure 10-52.

A DP IN Adapter shall follow the rules below when constructing an 128b/132b Control and Data Packet:

- The Tunneled Packet shall include at least one 128b/132b Control TU.
- The first doubleword in the payload contains a 128b/132b TU Header.
- The Tunneled Packet shall not include two consecutive Control TUs with the same *Control Type* field.
- The Tunneled Packet shall not include two consecutive Data TUs.
- The number of consecutive time slots (both allocated and unallocated) described by the Tunneled Packet shall not exceed 128 time slots. If the data of a time slot is split between two Tunneled Packets, the time slot is counted by each of the Tunneled Packets.
- A DP IN Adapter shall concatenate 128b/132b TUs into a single Tunneled Packet until one of the following conditions are true, resulting sending the Tunneled Packet:
 - The Tunneled Packet payload size is either 248 or 252 bytes.
 - Terminating the packet at 248 bytes is allowed only if the next payload to pack is a 128b/132b Data TU Header.
 - The maximum number (128) of allowed time slots described by the Tunneled Packet is reached.
 - An LLCP was received.

Figure 10-52. 128b/132b Control and Data Packet Format

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10.5.3.3.1.1 128b/132b Transfer Unit

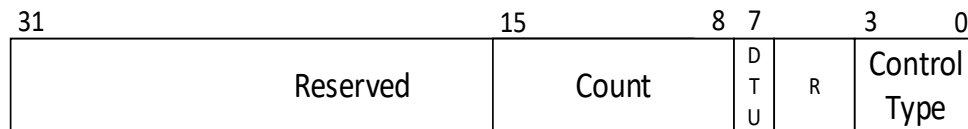
A 128b/132b Transfer Unit (TU) holds part of an MTP or MTPs. A 128b/132b TU consists of a header and optionally Data DWs. There are two types of 128b/132b TUs:

- **128b/132b Control TU** – Consists of a 128b/132b TU Header without any Data DWs. A single Control Symbol or a series of the same Control Symbol, whether they are consecutive or separated by unallocated time slots, are mapped into a 128b/132b Control TU.
- **128b/132b Data TU** – Consists of a 128b/132b TU Header and at least one Data DW. Data Symbols are mapped into a 128b/132b TU with both, header and Data DWs.

A 128b/132b TU Header shall have the format shown in Figure 10-53. The fields forming the 128b/132b TU Header shall be as defined below:

- **Control Type [3:0]:** For a Control TU, this field shall contain the value that represents the Control Link Symbol (as defined in Table 10-22). For a Data TU this field shall be set to 0.
- **Reserved [6:4]:** Reserved.
- **Data TU [7]:** This bit identifies the 128b/132b TU type:
 - 0b – Indicates a 128b/132b Control TU.
 - 1b – Indicates a 128b/132b Data TU.

- **Count [15:8]:** For a 128b/132b Data TU, this field shall contain the number of Data DWs following the 128b/132b TU Header. For a 128b/132b Control TU, this field shall contain the number of allocated time slots carrying the same Control symbol. This field shall have a value greater than zero.
- **Reserved [31:16]:** Reserved.

Figure 10-53. 128b/132b TU Header Format**Table 10-22. 128b/132b Control TU Types**

Control Link Symbol	Value
BS	02h
EOC	03h
SE	05h
SS	06h
SF	07h
BE	08h
VCPF	09h
(AVF) Active Video Fill	0Bh

A DP IN Adapter shall follow the rules below when constructing a 128b/132b TU:

- A 128b/132b TU shall be doubleword-aligned.
- The total length of a 128b/132b TU shall not exceed 252 Bytes.
- A 128b/132b TU may include data from up to 128 consecutive time slots.
- A 128b/132b TU shall not include data from more than 128 consecutive time slots.

10.5.3.3.2 128b/132b Data Packet

A DP IN Adapter uses a 128b/132b Data Packet to transport Data Symbols. A 128b/132b Data Packet has the *PDF* field in the Tunneled Packet Header set to Ah. A 128b/132b Data Packet shall have the format shown in Figure 10-54.

- A DP IN Adapter shall pack Data Symbols into a single Packet until one of the below conditions are true, resulting sending the Tunneled Packet:
 - The Tunneled Packet payload size is either 248 or 252 bytes.
 - Terminating the packet at 248 bytes is allowed only if the next payload to pack is a 128b/132b Control TU.
 - The maximum number of time slots (both allocated and unallocated) described by the Tunneled Packet reached the maximum allowed (128 time slots). If the data of a time slot is split between two Tunneled Packets, the time slot is counted by each of the Tunneled Packets.
 - An LLCP was received.

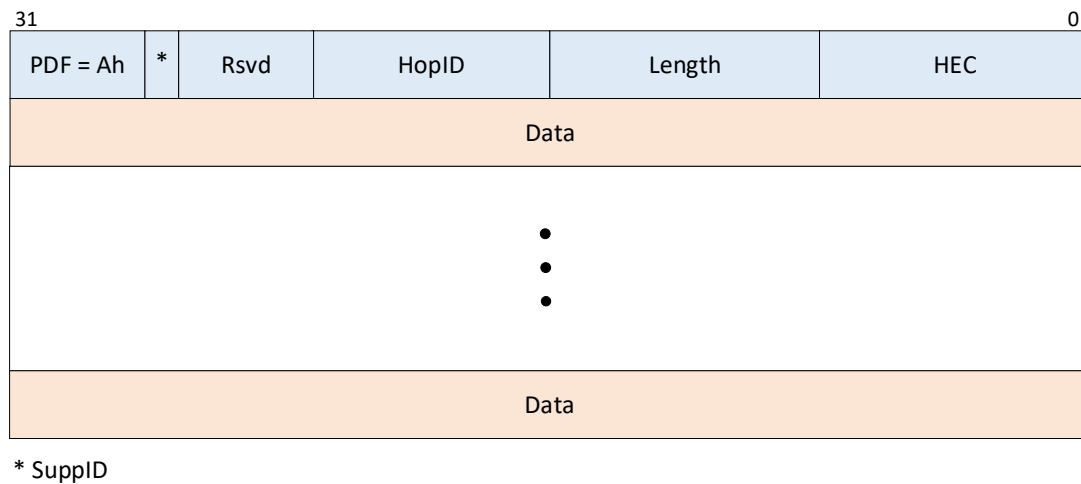
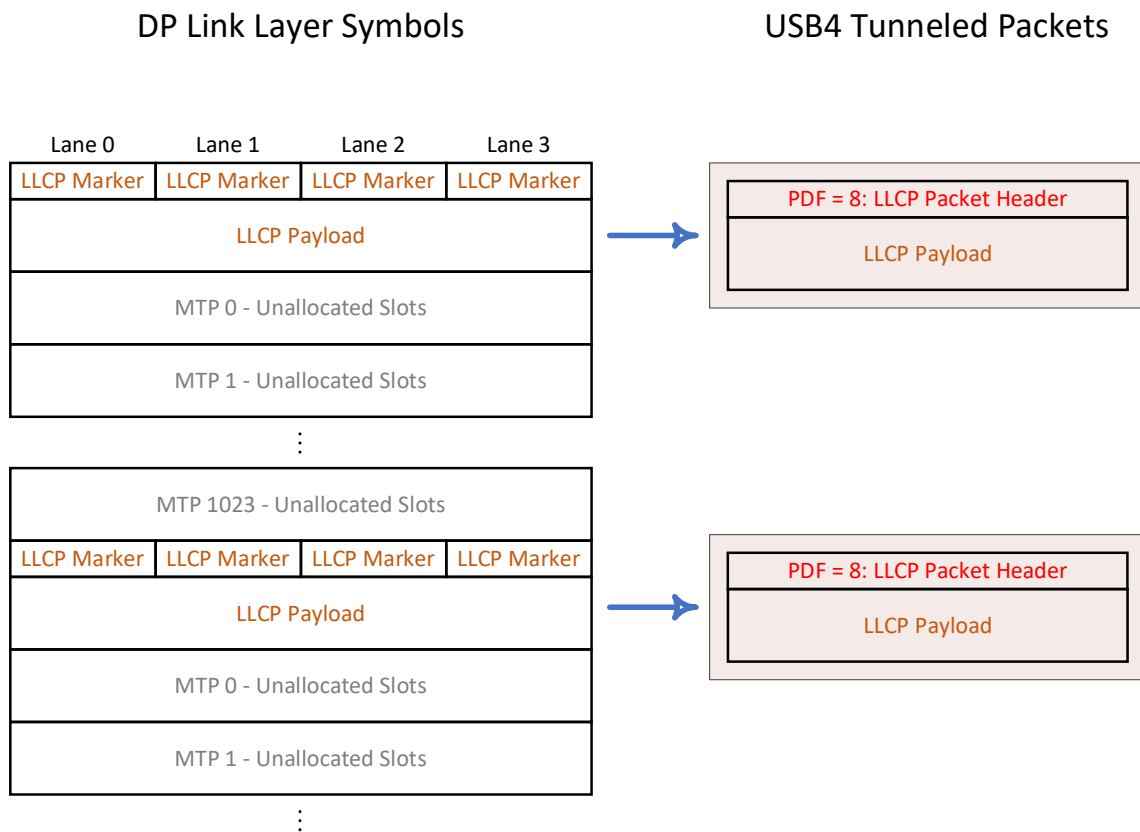
Figure 10-54. 128b/132b Data Packet Format**10.5.3.4 128b/132b Encapsulation Examples****10.5.3.4.1 No Time Slots are Allocated**

Figure 10-55 illustrates the case where no time slots are allocated. In this case only 128b/132b LLCP Packets are sent.

Figure 10-55 No Time Slots are Allocated

10.5.3.4.2 MSA Packet Encapsulation

Figure 10-56 illustrates an encapsulation of an MSA Packet into 128b/132b Data and Control Packet. Note it is an example, and the encapsulation of the entire MSA Packet may split across multiple USB4 Tunneled Packets.

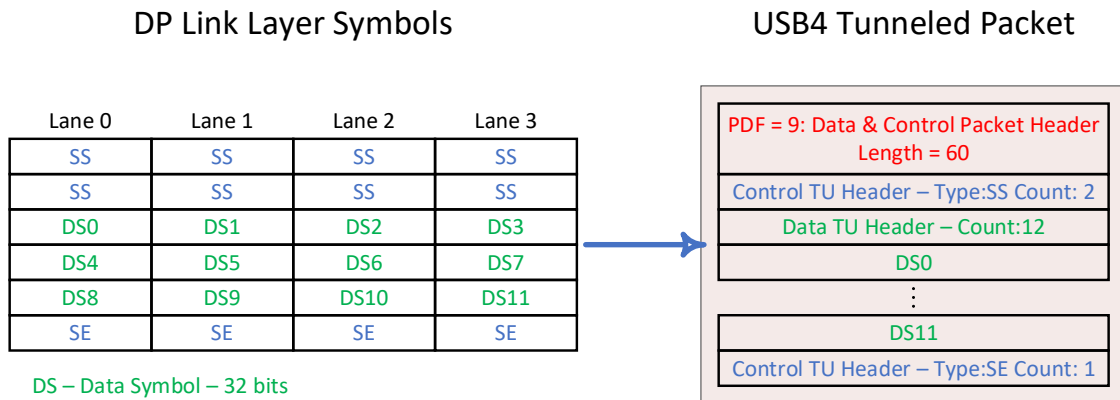
Figure 10-56 128b/132b MSA Packet Encapsulation**10.5.3.4.3 128b/132b Data Only, 128 Time Slots**

Figure 10-57 illustrates an encapsulation of a DP Link with four allocated time slots. The DP symbols contain only Data Symbols, which is encapsulated into 128b/132b Data Packet. The 128b/132b Data Packet is sent due to 128 time slots limit reach.

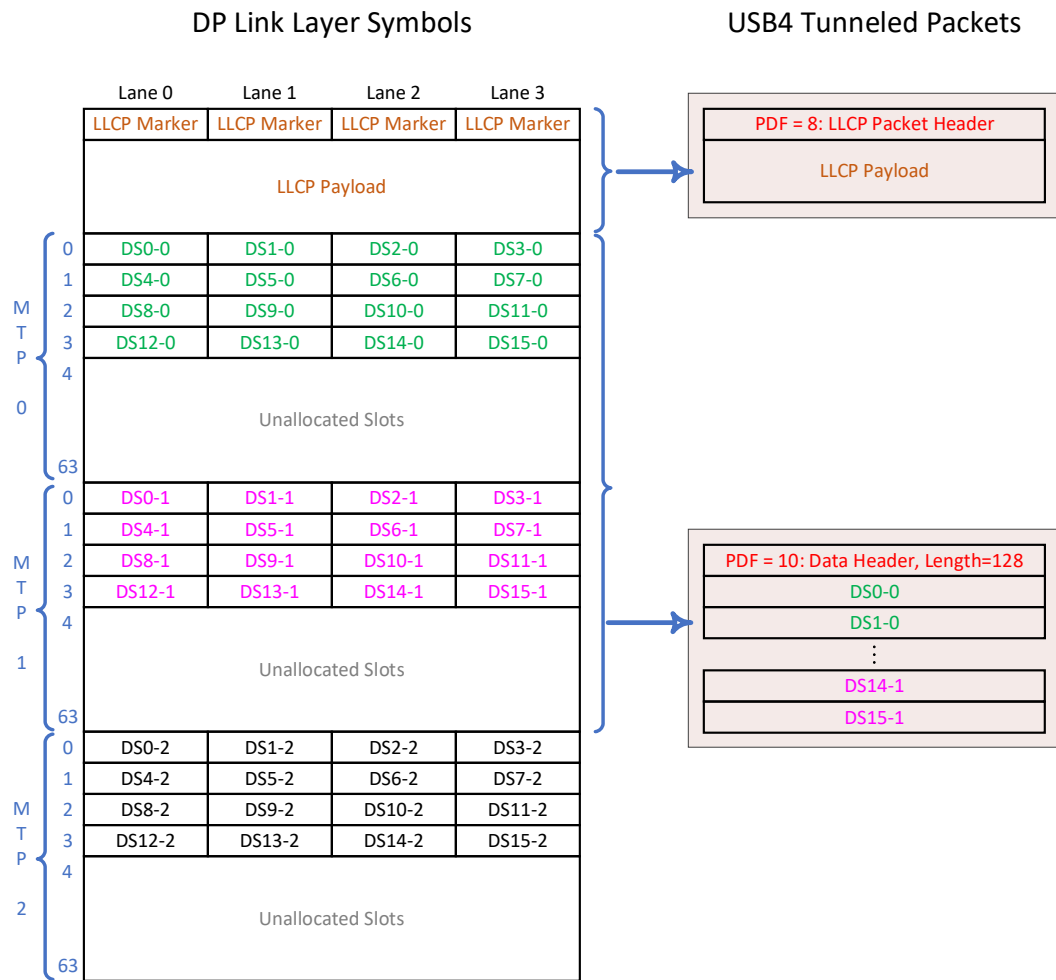
Figure 10-57 128b/132b Data Only, 128 Time Slots**10.5.3.4.4 128b/132b Data Only, 252 Bytes**

Figure 10-58 illustrates an encapsulation of a DP Link with ten allocated time slots. The DP symbols contain only Data Symbols, which is encapsulated into 128b/132b Data Packets. The 128b/132b Data Packets are sent due to 252 bytes payload limit reach.

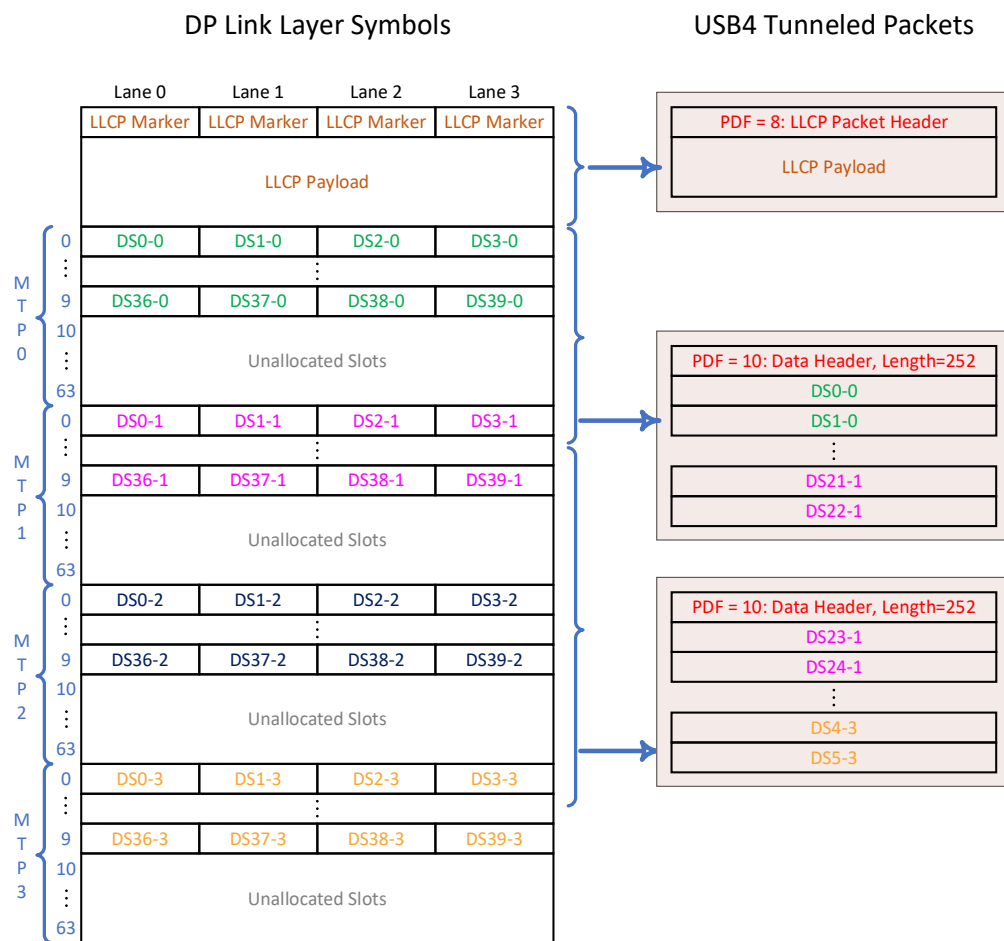
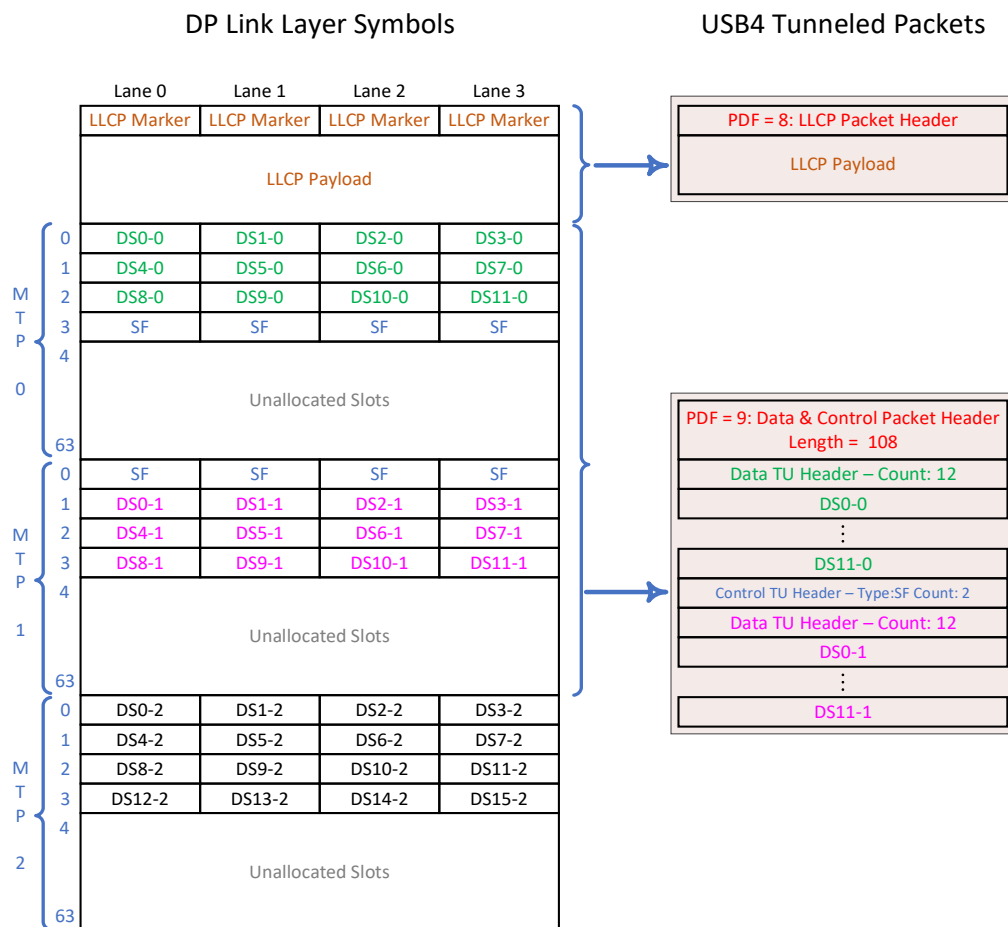
Figure 10-58 128b/132b Data Only, 252 Bytes**10.5.3.4.5 128b/132b Data and Control, 128 Time Slots**

Figure 10-59 illustrates an encapsulation of a DP Link with four allocated time slots. The DP symbols contain Data and Control Symbols, which is encapsulated into 128b/132b Data & Control Packet. The 128b/132b Data & Control Packet is sent due to 128 time slots limit reach.

Figure 10-59 128b/132b Data and Control, 128 time slots

10.5.4 FEC Functionality

10.5.4.1 8b/10b FEC

This section describes the methods by which a DP Adapter, operating with a 8b/10b DP Link, supports FEC functionality while ensuring that all Main-Link Symbols, Data and Control, generated by the DP OUT Adapter are identical to the Main-Link Symbols received by the DP IN Adapter over the DP Link.

10.5.4.1.1 SR Count

A DP Adapter shall implement the SR Count counter, which counts the number of cycles that have elapsed since the last SR. A DP IN Adapter uses this counter to measure and report to the DP OUT Adapter, the number of cycles from the last SR it received to the first cycle of the FEC_DECODE_EN or FEC_DECODE_DIS sequences. A DP OUT Adapter uses this counter to count the number of cycles which elapsed since the last SR it transmitted in order to recreate the FEC_DECODE_EN or FEC_DECODE_DIS sequences at the same cycle, and after the same SR, as the DP IN Adapter has received.

A DP IN Adapter shall initiate the SR Count at the first cycle after receiving an SR. A DP OUT Adapter shall initiate the SR Count at the first cycle after transmitting an SR. For SST, the count starts after receiving or transmitting all four Enhanced Framing Mode Symbols. SR Count counts any link clock cycle, including cycles which carry FEC-related symbols.

10.5.4.1.2 DP IN Adapter Requirements

A DP IN Adapter shall:

- Implement FEC Decoding as defined in the DisplayPort Specification.
- Construct an FEC_DECODE Packet as defined in Section 10.5.4.1.4 upon FEC_DECODE_EN or FEC_DECODE_DIS sequence detection.
- The Adapter Layer shall prioritize the FEC_DECODE Packet over all other Main-Link Path packets when pass it to the Transport Layer. If the Adapter Layer is constructing a Main-Link Path Packet when the FEC_DECODE_EN or FEC_DECODE_DIS sequence is received over the DP Main-Link, the Adapter Layer may first finish constructing the Main-Link Path Packet and pass it to the Transport Layer before passing the FEC_DECODE Packet.

A DP IN Adapter shall not:

- Tunnel any FEC-related symbols including FEC_PARITY_MARKER, FEC_DECODE & FEC_PARITY_PH.
- Count the Link cycles of FEC Symbols for fill count purposes.

10.5.4.1.3 DP OUT Adapter Requirements

A DP OUT Adapter shall:

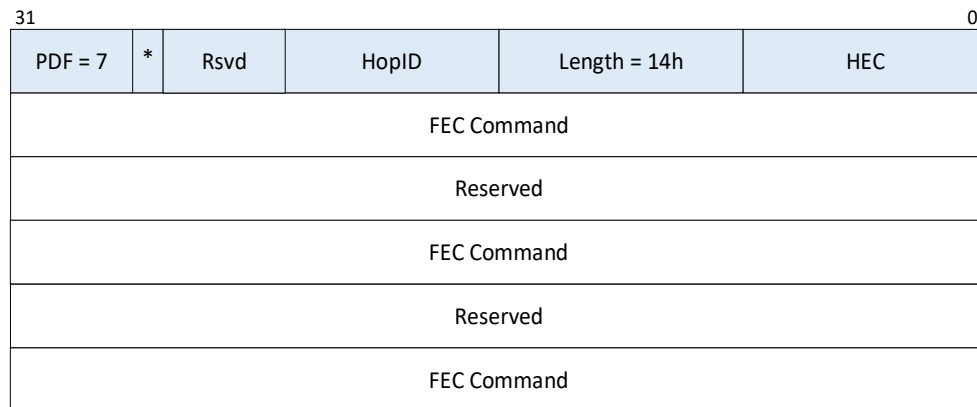
- Implement FEC Encoding as defined in the DisplayPort Specification.
- Apply majority voting for the repeated fields with in the FEC_DECODE Packet.
 - SR Count.
 - FEN.
 - FDS.
- Generate FEC_DECODE_EN and FEC_DECODE_DIS upon reception of a FEC_DECODE Packet.
 - FEC_DECODE_EN sequence shall be generated if *FEN* field in the FEC_DECODE Packet is 1b.
 - FEC_DECODE_DIS sequence shall be generated if *FDS* fields in the FEC_DECODE Packet is 1b.
 - The first symbol of the FEC_DECODE_EN and FEC_DECODE_DIS sequences shall be transmitted according to the *SR Count* field of the FEC_DECODE Packet, i.e. the FEC_DECODE_EN and FEC_DECODE_DIS sequence shall be transmitted *SR Count* link clock cycles after the most recently transmitted SR.
 - When a FEC_DECODE Packet is received, a DP OUT Adapter compares the Packet SR Count and the Counter SR Count as follows:
 - If Packet SR Count > Counter SR Count the DP OUT Adapter waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.
 - Else, a DP OUT Adapter waits for next SR to be transmitted, then waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.

A DP OUT Adapter shall not:

- Count the Link cycles of FEC Symbols for fill count purposes.

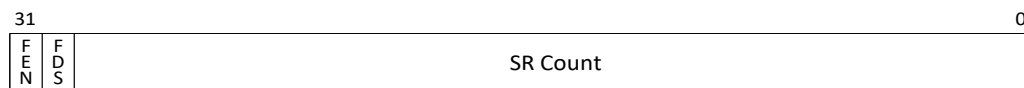
10.5.4.1.4 FEC_DECODE Packet

A FEC_DECODE Packet is sent over the Main-Link Path from DP IN Adapter to DP OUT Adapter. A FEC_DECODE Packet shall have the format shown in Figure 10-60.

Figure 10-60. FEC_DECODE Packet Format

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The *PDF* field in the header shall be set to 7 and the *Length* field shall be 14h. An FEC Command shall have the format defined in Figure 10-61. The three FEC Commands in an FEC_DECODE Packet shall be identical to each other.

Figure 10-61. FEC Command Format

The fields in an FEC Command shall contain the following:

- **SR Count [29:0]:** This field contains the number of DP Link clock cycles between the last received SR and the first FEC_DECODE_EN or FEC_DECODE_DIS sequences. The minimum value for this field is 1h (occurs when SR is immediately followed by FEC_DECODE sequence).
- **FEC DISABLE (FDS) [30]:** This field shall be set to 1b if a FEC_DECODE_DIS sequence was detected. In all other cases it shall be set to 0b.
- **FEC ENABLE (FEN) [31]:** This field shall be set to 1b if a FEC_DECODE_EN sequence was detected. In all other cases it shall be set to 0b.

10.5.4.2 128b/132b FEC

A DP IN Adapter shall implement FEC Decoding as defined in the DisplayPort Specification.

A DP IN Adapter shall not tunnel any FEC-related symbols including RS Parity symbols and the associated padding bits.

A DP OUT Adapter shall implement FEC Encoding as defined in the DisplayPort Specification

10.5.5 DP OUT Adapter Buffer

In order to reconstruct DP Main-Link traffic without any interruptions, a DP OUT Adapter shall implement a buffer that can be used to compensate for the jitter in the latency of the received Tunneled Packets.

After the DP link is successfully trained, a DP OUT Adapter may start generating idle pattern as described in the DisplayPort Specification or keep transmitting the same TPS it is currently transmitting. The DP OUT Adapter transitions from sending self-generated idle pattern or TPS to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps:

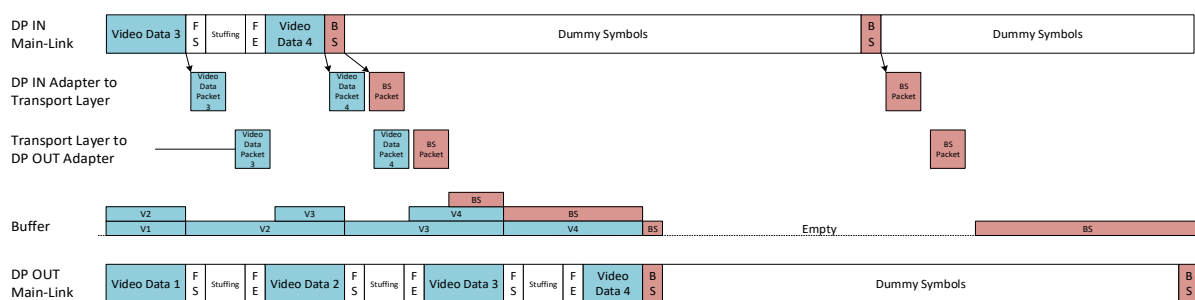
1. The DP OUT Adapter shall adjust the PLL frequency at least once as a result of an Adjust PLL event as described in Section 10.6.
2. The DP OUT Adapter ensures, in an implementation specific manner, that within eight PLL frequency adjustments the link symbol clock frequency difference between its own and the DPTX is such that buffer overflow and buffer underrun is avoided.
3. The DP OUT Adapter shall wait to receive an SR (for 8b/10b DP Link) or an LLCP (for 128b/132b DP Link) from the DP IN Adapter.
 - All Main-Link Path Tunneled Packets, besides DP Clock Sync Packets, are dropped by the DP OUT Adapter until reception of the SR (for 8b/10b DP Link) or an LLCP (for 128b/132b DP Link).
 - After the next step is completed, the received SR (for 8b/10b DP Link) or an LLCP (for 128b/132b DP Link), shall be the first symbol driven by the DP OUT Adapter as the reconstructed Main-link.
4. The DP OUT Adapter delays sending the SR (for 8b/10b DP Link) or an LLCP (for 128b/132b DP Link) in Step 3 for a number of Accumulation Cycles (see Section 10.5.5.2).
 - During the delay, the DP OUT Adapter shall accumulate the DP Main-Link traffic from the DP IN Adapter.

10.5.5.1 Buffer Operation

During Active Video periods, the buffer is filled to some extent due to the Accumulation Cycles that the DP OUT Adapter waits when switching from self-generated idle pattern or TPS to reconstruction of DP Main-Link.

During Blanking periods and idle pattern, where the maximal distance between two BS could be 8K cycles, the buffer might become empty. If the buffer becomes empty, a DP OUT Adapter shall continue to drive Dummy Symbols on the DP Main Link, assuming that the next Main-Link Path Tunneled Packet holds a Fill Count value larger than the driven Dummy Cycles. Figure 10-62 shows the process of switching from Active Video to Blanking for 8b/10b DP SST link.

Figure 10-62. Active Video to Blanking for 8b/10b DP SST Link



10.5.5.2 Accumulation Cycles

Accumulation Cycles are counted in Link Symbol clock cycles, where one Accumulation Cycle equals one Link Symbol clock cycle. The number of Accumulation Cycles that a DP OUT Adapter waits is a function of the following:

- DP IN Jitter – the Jitter between Tunneled Packets from the DP IN Adapter.
 - The delay from when a DP construct is received over the DP Main-Link until a DP IN Adapter generates the Main-Link Tunnel Packet can vary where:

- Minimal delay is for LLCP, MSA and BS.
- Maximal delay is:
 - 8b/10b MST: 17 MTPs + Max 8b/10b FEC Cycles¹ = 1088 + 37 = 1125 LS Cycles.
 - 8b/10b SST: 16 Video TUs + Max 8b/10b FEC Cycles = 1024 + 37 = 1061 LS Cycles.
 - 128b/132b: 2 MTPs (1 Lane) + 2 PHY SYNC + Max 128b/132b FEC Cycles² = (4 x 2 x 64) + 2 + 18 = 532 LS Cycles
- USB4 Delay Jitter – the Jitter cause by delays over the USB4 Fabric.
 - The following can create delays at the Egress Adapter for each Hop:
 - Time Sync Packets.
 - Credit Grant Packets.
 - Control Packets.
 - Other Tunneled Packets (on both same priority and lower priority Paths).
 - Packet forwarding jitter within a Router.
 - The delay depends on the number Credit Grant Records, the number of additional DP Paths, the USB4 Link speed, and the assumptions regarding how many delay factors on average affect each Hop.

A DP OUT Adapter shall report the Maximum Accumulation Cycles it performs. The maximum is needed when operating at the maximum DisplayPort Link Rate.

The following is an example of a DP OUT Adapter that supports the maximum DP Link Rate of HBR3, supports MST, and assumes that a DP Tunneled Packet is delayed at every Hop by two full size Packets:

- Worst case Accumulating Cycles = (DP IN Jitter) + (USB4 Delay Jitter)

$$= (17\text{MTPs} + \text{Max FEC Cycles}) + (((5\text{ Hops} \times 2 \times 260\text{ Bytes} \times 8) \times \text{USB4 UI}) / (10 \times \text{HBR3 UI}) + (6\text{ Hops} \times \text{tTunneledPacketJitter} / (10 \times \text{HBR3 UI})))$$

$$= (1088+37) + ((20800\text{ Bits} \times 0.1\text{ ns} / 1.23\text{ ns}) + (6 \times 100\text{ ns} / 1.23\text{ ns})) = 3305\text{ Link Symbol Cycles}$$

10.5.6 HDCP

High-bandwidth Digital Content Protection (HDCP) is performed in the DisplayPort Link Layer. A DisplayPort tunnel is transparent to HDCP. A DP Adapter is not aware of whether or not HDCP is used and does not participate in the HDCP process.

A DP IN Adapter shall not perform HDCP decryption. It shall not drop or modify an AUX Request or AUX Response associated with HDCP functionality.

A DP OUT Adapter shall not perform HDCP encryption.

Note: When HDCP is active, the Stuffing Symbols generated by a DP OUT Adapter do not have the same values as generated by the DPTX.

¹ Max 8b/10b FEC Cycles = 3 x FEC_PARITY_PH + 1 x FEC_PM = 3 x 12 + 1 x 1 = 37 Cycles.

² Max 128b/132b FEC Cycles = 6 x (FEC_PARITY + FEC Padding bits + CDI) = 6 x (64 + 8 + 24) / 32 = 18 Cycles.

10.5.7 AUX-less Advanced Link Power Management (ALPM)

The AUX-less Advanced Link Power Management (ALPM) feature is defined by DisplayPort Specification. ALPM allows the DisplayPort Main-Link to enter a Low Power state during a vertical blanking period, and exit before a new frame is transmitted. The DPTX signals the entrance to the Low Power state (sleep sequence) and exit from the Low Power state (wake sequence) over the Main-Link.

Support for ALPM is optional for DP Adapters. A DP Adapter that supports ALPM shall set the DP_LOCAL_CAP.ALPM *Support* bit to 1b. A DP Adapter that does not supports ALPM shall set the DP_LOCAL_CAP.ALPM *Support* bit to 0b.

The ALPM feature is supported over a DP Tunnel if the DP_COMMON_CAP.ALPM *Support* bit is 1b. If ALPM is supported over a DP Tunnel, the DP Adapters shall support the sleep sequence defined in Section 10.5.7.2 and the wake sequence defined in Section 10.5.7.3.

10.5.7.1 ALPM DP Link Control Packet

The ALPM DP Link Control Packet is sent over the Main-Link Path from DP IN Adapter to DP OUT Adapter as part of the sleep and wake sequences defined in Section 10.5.7.2 and Section 10.5.7.3 respectively. An ALPM DP Link Control Packet shall have the format shown in Figure 10-63.

Figure 10-63: ALPM DP Link Control Packet Format

31		28		26		23		22		16		15		8		7		0	
PDF=11		*		Reserved		HopID				Length = 4				HEC					
Type = 01h				SR Count														S / W	

The *PDF* field in the header shall be set to 11 and the *Length* field shall be 04h.

The fields forming the ALPM DP Link Control Packet payload shall be as defined below:

- **S/W [0]:** This bit indicates if this is a sleep or a wake packet. In a sleep sequence, this bit shall be set to 1b. In a wake sequence, it shall be set to 0b.
- **SR Count [23:1]:** When operating with a 8b/10b DP Link and the *S/W* bit is set to 1b, this field contains the number of DP Link clock cycles between the last received SR and the first ML_PHY_SLEEP sequence. The minimum value for this field is 1h (occurs when SR is immediately followed by ML_PHY_SLEEP sequence). When operating with a 128b/132b DP Link or the *S/W* bit is set to 0, this field shall be set to 0h.
- **Type [31:24]:** This field shall be set to 01h, indicating that the packet is a DP Link Control Packet of type ALPM.

10.5.7.2 Sleep Sequence

Upon reception of an ML_PHY_SLEEP sequence, as defined in the DisplayPort Specification, a DP IN Adapter shall perform the following sleep sequence:

1. Stop sending DP Clock Sync Packets.
2. Send as Tunneled Packets, all the DP Main-Link constructs that were received prior to the ML_PHY_SLEEP.
3. Send a DP Link Control Packet of type ALPM with the following fields:
 - a. *S/W* – Set to 1b.
 - b. *SR Count* – If the DP Link is 8b/10b then set to the number of cycles as described in Section 10.5.7.1. If the DP Link is 128b/132b then set to 0h.

Note: For an 8b/10b DP Link, the DP Link Control Packet of Type ALPM may be sent by the DP IN Adapter prior to sending all the Tunneled Packets mentioned in Step 2.

If *USB4 CL1 Granted through ALPM* bit in the DPCD Tunnel POWER MANAGEMENT CONFIGURATION (address E0032h bit 0) is set to 1b, the DP IN Adapter shall send a PM Packet with the *CLx State* field set to 01b over the Main-Link Path. If *USB4 CL1 Granted through ALPM* bit is set to 0b, the DP IN Adapter shall not send a PM Packet with the *CLx State* field set to 01b over the Main-Link Path.

Note: A DP IN Adapter follows the sleep sequence above after receiving the first ML_PHY_SLEEP, regardless of its position in the LTTPR count.

Upon reception of an ALPM DP Link Control Packet with the *S/W* bit set to 1b, a DP OUT Adapter shall perform the following sleep sequence:

1. Store the current transmitter frequency.
2. For a 128b/132b DP Link:
 - a. Reconstruct the Tunneled Packets that were received prior to the ALPM DP Link Control Packet into DP native packets and transmit them over the DP Main Link.
 - b. Insert scrambled zeros to complete the FEC frame that includes the DP native packets from Step 2.
3. For an 8b/10b DP Link, compare the Packet SR Count and the Counter SR Count as follows:
 - If Packet SR Count > Counter SR Count, the DP OUT Adapter waits for the Counter SR Count to be equal to Packet SR Count.
 - Else, a DP OUT Adapter waits for the next SR to be transmitted, then waits for the Counter SR Count to be equal to Packet SR Count.

While performing this step, reconstruct the Tunneled Packets into DP native packets and transmit them over the DP Main Link.

4. Generate ML_PHY_SLEEP pattern as DPTX generates it, according to the DisplayPort Specification. A DP OUT Adapter generates the ML_PHY_SLEEP pattern according to the number of LTTPRs reported in the *Downstream_LTTPRs* field in the SET_LTTPR_MODE SET_CONFIG Packet it received from the DP IN Adapter.

10.5.7.3 Wake Sequence

Upon detecting an LFPS, which is qualified as a wake signal according to the DisplayPort Specification, a DP IN Adapter shall send a DP Link Control Packet of type ALPM with the *S/W* bit set to 0b and the *SR Count* field set to 0h. The DP IN Adapter shall send the DP Link Control Packet within tDPALPMWake after detecting the LFPS.

When a DP IN Adapter ends its PHY establishment and detects an ML_PHY_LOCK, as defined by DisplayPort Specification, it shall start converting DisplayPort Main-Link Symbols into Tunneled Packets after receiving an SR (for a 8b/10b DP Link) or an LLC (for a 128b/132b DP Link).

After a DP IN Adapter sends the DP Link Control Packet of type ALPM with the *S/W* bit set to 0b, it shall:

1. Before advancing to Step 2, ensure it has ended its PHY establishment and detected an ML_PHY_LOCK.
2. Enable its Clock Synchronization – Start advancing the Lifetime Counter and send DP Clock Sync Packets as defined in Section 10.6.

2-a. The first Clock Sync packet shall be sent within 4.3ms from the DP Link Control Packet of type ALPM with the S/W bit set to 0b.

Note: Clock Synchronization is restarted from the initial state after ALPM Wake. Therefore, the first Measure Window Event will not produce a DP Clock Sync packet as it might not be accurate, from 2nd Measure Window Event and on DP Clock Sync packet shall be produce-d as defined in Section 10.6.2.1.

Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 0b, a DP OUT Adapter shall perform the following wake sequence:

1. If the DP OUT Adapter is in the process of a Sleep sequence, it shall:
 - a. Complete the Sleep sequence as defined in Section 10.5.7.2
 - b. Park its transmitters in electrical idle for at least tEnterLFPS (2us), as defined in the DisplayPort spec
2. Start generating the LFPS followed by ML_PHY_LOCK_LTTPr pattern as the LTTPr that is adjacent to the DPTX generates it, according to DisplayPort Specification. The DP OUT Adapter shall start generating LFPS within tDPALPMWake after receiving the ALPM DP Link Control Packet and the DP Link is in electrical idle.
 - DP OUT Adapter shall generate the ML_PHY_LOCK_LTTPr pattern for tDCS, as defined in the DisplayPort Spec. The tDCS is calculated according to the number of LTTPrs reported in the *Downstream_LTTPrs* field in the SET_LTTPr_MODE SET_CONFIG Packet it received from the DP IN Adapter.
 - DP OUT Adapter shall activate its transmitters at the nominal frequency.
3. Complete the following within tACDS (tACDS is defined in DisplayPort specification):
 - a. Transition the transmitters frequency from the nominal frequency to the same frequency it saved during the previous sleep sequence
 - b. Switch the transmitted pattern from ML_PHY_LOCK_LTTPr to ML_PHY_LOCK
4. For a 128b/132b DP Link, send 7 x (Downstream_LTTPrs + 1) ML_PHY_LOCK and then transition to 1-Bit CDI operation at the next PHY Sync symbol.
5. For a 8b/10b DP Link, continue transmitting ML_PHY_LOCK.
6. Start accumulating DP Main Link traffic coming from the DP IN Adapter after receiving an SR (for 8b/10b DP Link) or an LLCP (for 128b/132b DP Link). After accumulating for a number of Accumulation Cycles, A DP OUT Adapter shall start reconstructing the DP Main-Link from the Tunneled Packets.
7. After waiting for tCLxConvergeTime from the reception the ALPM DP Link Control Packet with the S/W bit set to 0b, enable its Clock Synchronization – Start advancing the Lifetime Counter

Upon reception of a DP Clock Sync Packet, a DP OUT Adapter resumes adjusting the DP OUT PLL as defined in Section 10.6.2.2.

Note: A DP OUT Adapter starts accumulating the DP Main Link traffic regardless of whether or not the DP OUT Adapter PLL frequency was adjusted by a DP Clock Sync Packet.

Note: The relationships between the Lifetime Counters in the DP IN and DP OUT Adapters are not maintained when entering and exiting ALPM sleep.

10.6 DP Link Clock Sync

A DisplayPort Sink device recovers the link symbol clock from the Main-Link and uses the M and N values (for 8b/10b DP Link) or VFREQ (for 128b/132b DP Link) embedded within the video stream to derive the stream clock (pixel clock) from the recovered link symbol clock. When a DisplayPort link is tunneled across a USB4 Fabric, the DP IN and DP OUT Adapters are in different clock domains, Link Symbol clock synchronization is needed so that:

- The DisplayPort Sink is able to recreate the pixel clock.
- Symbols received by a DP IN Adapter are identical to the symbols sent by the DP OUT Adapter.

This section describes the method by which the DP OUT Adapter generates the DP-Main Link Symbol clock at the same frequency as the DP IN Adapter recovers it.

10.6.1 Synchronization Method

Clock Synchronization starts as soon as the Link Symbol clock is stable. It is achieved by periodically following the steps below:

1. Both the DP IN Adapter and DP OUT Adapter measure the number of link symbol clocks within a synchronized measurement window.
2. The DP IN Adapter sends its measurement to the DP OUT Adapter.
3. The DP OUT Adapter computes the difference between the frequencies and adjusts its Link symbol clock frequency.

10.6.1.1 Events

10.6.1.1.1 Measuring Events

The measuring events at a DP Adapter are derived from the Host Router Time, which guarantees high accuracy, synchronized events. The two measuring events used for the DP Main-Link Symbol Clock Synchronization scheme are:

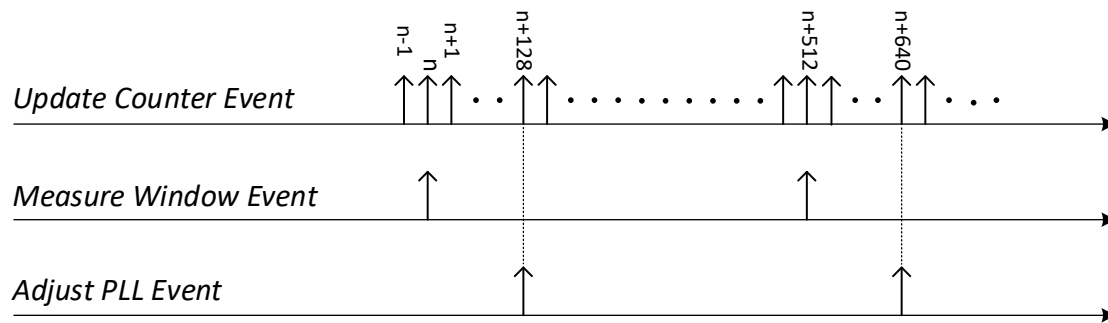
- Measure Window Event – occurs every 2^{21} ns (i.e. when bit 21 of the *Nanosecond* field of the Host Router Time changes polarity).
- Update Counter Event – occurs every 2^{12} ns (i.e. when bit 12 of the *Nanosecond* field of the Host Router Time changes polarity).

Note: If the Domain operates in Inter-Domain mode and it is a follower, then the Host Router Time refers to the Inter-Domain Host Router Time defined in Section 7.4.2. Otherwise, it refers to Host Router Time defined in Section 7.4.1.

10.6.1.1.2 Adjust PLL Event

An Adjust PLL event is used by a DP OUT Adapter to initiate the PLL frequency adjustment. An Adjust PLL Event occurs when there have been 128 Update Counter Events since the last Measure Window Event.

Figure 10-64 illustrates when Adjust PLL Events occur.

Figure 10-64: Adjust PLL Event Occurrence**10.6.1.2 Lifetime Counter**

The Lifetime Counter (LC) is a free running 64-bit counter that advances in proportion to the DP Main-Link Symbol clock. It increases by 1 for each Symbol clock (10 UI) when the DP Main-Link operates in RBR or HBR. It increases by 1 for every 2 Symbol clocks (20 UI) when the DP Main-Link operates in HBR2 or HBR3. It increases by 1 for every 32 UI when the DP Main-Link operates in UHBR10, UHBR13.5, or UHBR20. The LC is reset when DP Main-Link is down and starts counting when DP Main-Link Symbol clock is stable.

A DP OUT Adapter shall start counting as soon as Link Symbol clock is stable for starting link training with DPRX.

A DP IN Adapter shall start counting as soon as it completed its equalization process.

In order to filter out the variation introduced by spread-spectrum modulation, the LC shall be filtered using a first order IIR filter. Therefore, the value of the LC is sampled upon an Update Counter Event, converted to fractional representation, and then used for calculating the Filtered Lifetime Counter (FLC), according to formula:

$$LC_Frac[n] = \{LC[n], 00000000b\}$$

$$FLC[n] = LC_Frac[n] \gg 5 + FLC[n-1] - FLC[n-1] \gg 5 ; n > 0$$

$$FLC[n] = LC_Frac[n] \gg 5 ; n = 0$$

where:

LC[n] – is the current sample of LC.

LC_Frac[n] – is the current sample of LC represented in fractional format.

FLC[n-1] – is the previous output of the filter.

FLC[n] – is the new output of the filter.

The filtering operation shall be done with 8-bit truncation at the fraction part to assure reproducible result. All operands of IIR filter shall have the same format of 64 bits of integer followed by 8 bits of fraction.

The *Window Count* field, LC Counter, LC_Frac operand, and FLC Counter structures are shown in Figure 10-65. An illustration of the computation logic is shown in Figure 10-66.

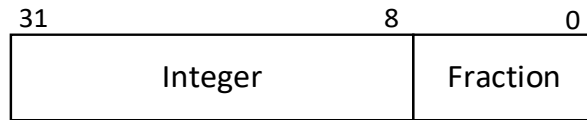
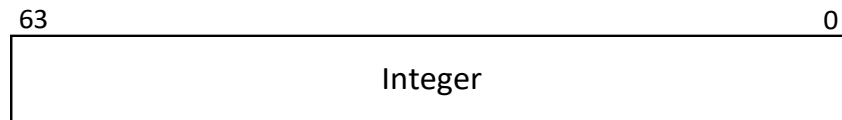
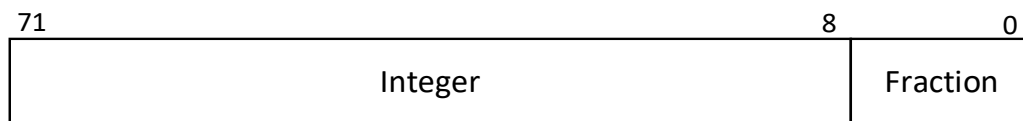
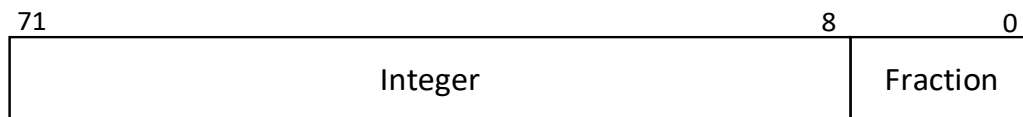
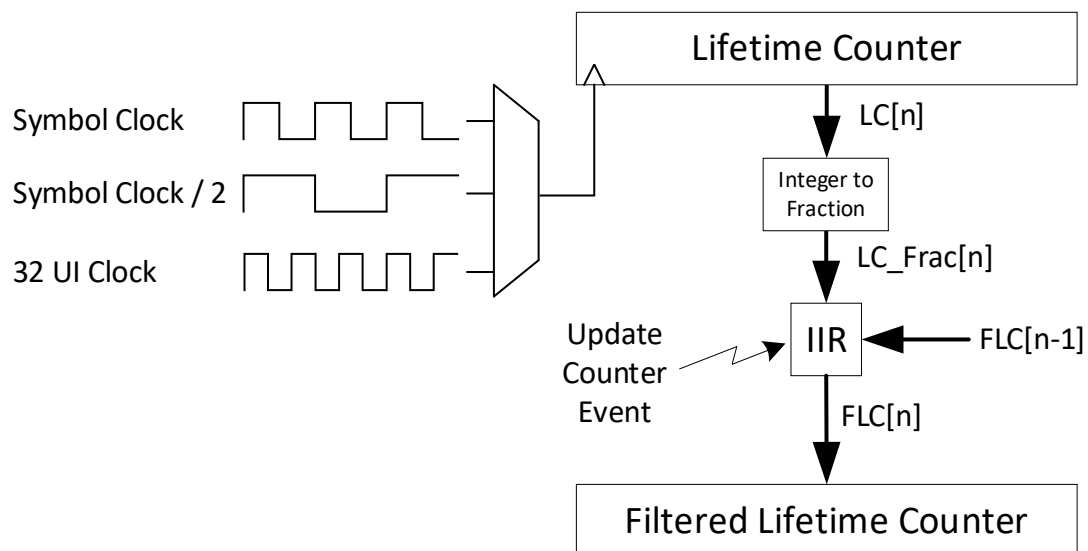
Figure 10-65. Lifetime Counter Format**A. Window Count****B. Lifetime Counter (LC)****C. Lifetime Counter – Fraction representation (LC_Frac)****D. Filtered Lifetime Counter (FLC)****Figure 10-66. Filtered Lifetime Counter Logic Concept**

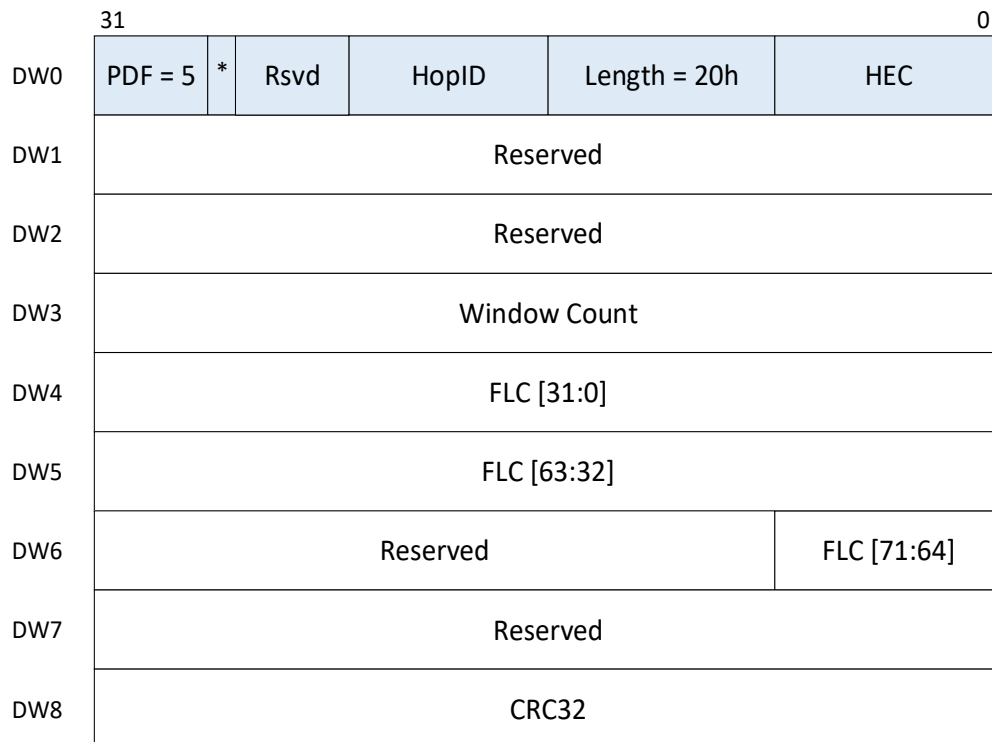
Table 10-23 shows an example of five FLC calculations, starting from $n=0$.

Table 10-23. FLC Calculation Examples

n	LC	FLC
0	0xBC	0x5E0
1	0x50E	0x2E21
2	0x95F	0x77A8
3	0xDB1	0xE173
4	0x1203	0x16A80

10.6.1.3 DP Clock Sync Packet

A DP Clock Sync Packet has the *PDF* field in the Tunneled Packet Header set to 5. It is sent over the Main-Link Path from a DP IN Adapter to a DP OUT Adapter. A DP Clock Sync Packet shall have the format shown in Figure 10-67.

Figure 10-67. DP Clock Sync Packet Format

* SupplD

The fields forming a DP Clock Sync Packet shall be as defined below:

- **Reserved:** This field is reserved and shall be set to 0.
- **Window Count:** This field is defined in Section 10.6.2.1. The *Window Count* field structure is shown in Figure 10-65(A).
- **FLC:** This field contains the snapshot of the Filtered Lifetime Counter at the time the Window Measured Event occurred.
- **CRC32:** This field contains a CRC32 computed over the entire payload using the following DW order: DW1, DW3, DW2, DW7, DW6, DW5, DW4. The following CRC shall be used:

- Width: 32
- Poly: 1EDC 6F41h
- Init: FFFF FFFFh
- RefIn: True
- RefOut: True
- XorOut: FFFF FFFFh

Figure 10-68 shows an example of a DP Clock Sync Packet.

Figure 10-68. DP Clock Sync Packet Example

31						0
PDF = 5	*	Rsvd	HopID	Length = 20h	HEC	
00_00_00_00h						
00_00_00_00h						
09h		73h		2Fh		C6h
CAh		FDh		40h		02h
34h		56h		78h		9Ah
00_00_00h						12h
00_00_00_00h						
47h		64h		79h		0Ah

* SupplD

10.6.2 DP Adapter Requirements

10.6.2.1 DP IN Adapter Requirements

A DP IN Adapter shall:

- Implement a Lifetime Counter as described in Section 10.6.1.1.2.
- Implement the logic to perform the LC filtering.
- Update FLC upon an Update Counter Event.
- Upon the first Measure Window Event:
 - Capture the current FLC.
 - Store the current captured FLC to be used as previous captured FLC at the next Measure Window Event.
- Upon each subsequent Measure Window Event:
 - Capture the current FLC.

- Compute the Window Count by calculating the current captured FLC minus the FLC that was captured at the previous Measure Event.
- Construct a DP Clock Sync Packet and send it over the Main-Link Path within tDPClockSync after the Measure Window Event.
 - The maximum allowed deviation for the Window Count field is 10 ppm over a window of 100ms. The window terminates if the DisplayPort link goes to a low power state.
- Store the current captured FLC to be used as previous captured FLC at the next Measure Window Event.



IMPLEMENTATION NOTE

To meet the Window Count maximum deviation requirement from the first DP Clock Sync Packet, the DP IN Adapter needs to ensure that the Lifetime Counter filter is not in its initial transient phase.

Note: A DP IN Adapter may send a DP Clock Sync Packet before DP Link Training is completed.

10.6.2.2 DP OUT Adapter Requirements

A DP OUT Adapter shall:

- Implement a Lifetime Counter as described in Section 10.6.1.2.
- Implement the logic to perform the LC filtering.
- Update FLC upon an Update Counter Event.
- Upon a Measure Window Event:
 - Capture the current FLC.
 - Compute the Window Count as described in Section 10.6.2.1.
- Upon receiving a DP Clock Sync Packet after the Measure Window Event and before the PLL Adjust Event, compute the PLL frequency adjustment. The method for computing the PLL frequency adjustment is outside the scope of this specification.
- Upon an Adjust PLL Event, adjust the PLL frequency based on the computation performed at the Measure Window Event.

If a DP OUT Adapter receives a DP Clock Sync Packet after an Adjust PLL Event but before the next Measure Window Event, it shall not adjust the PLL and shall silently discard the packet.

If a DP OUT Adapter receives a DP Clock Sync Packet before it computed the first Window Count, it shall not adjust the PLL and shall silently discard the packet.

When a DP OUT Adapter changes the DisplayPort Main-Link transmitter frequency as a result of adjusting the PLL frequency, it shall adhere to the DisplayPort Specification. The PLL frequency adjustment shall be completed within tDPPLLAdjust after the Adjust PLL Event.



IMPLEMENTATION NOTE

A DP OUT Adapter needs to take measures to ensure that the number of Link Symbol clock cycles between it and the DP IN Adapter don't drift over time. This includes the following:

- *The Lifetime Counters in the DP IN Adapter and the DP OUT Adapter start counting at different points in time. This causes an initial offset between the FLC values in the DP IN and DP OUT Adapter, which a DP OUT Adapter can calculate at the first Measure Window Event where it has FLC values from the DP IN Adapter (as provided in a DP Clock Sync Packet). In subsequent PLL frequency adjustments, a DP OUT Adapter should maintain a distance equal to the initial offset when adjusting the PLL frequency.*

- A DP OUT Adapter uses two data points when computing the PLL frequency adjustment: Window Count, and FLC. Including the FLC as a data point, helps eliminate drift.

10.7 DP BW Allocation Mode

A DP IN Adapter shall support DP BW Allocation Mode as defined in this section.

When DP BW Allocation Mode is enabled (see Section 10.7.1), the DPTX and the Connection Manager communicate through the DP IN Adapter. The interaction between a DP IN Adapter and a DPTX is described in Section 10.7.2. The interaction between a DP IN Adapter and a Connection Manager is described in Section 10.7.3.

10.7.1 DP BW Allocation Mode Enablement

A DP IN Adapter shall:

- Update the AUX Response for DPCD DP TUNNELING SUPPORT. *DP_IN_BW_Allocation_Mode_Support* (E000Dh, bit 7) to 1b.
- Update the AUX Response for DPCD USB4_DRIVER_BW_CAPABILITY. *USB4_Driver_BW_Allocation_Mode_Support* (E0020h, bit 7) to have the same value as *ADP_DP_CS_2.CM BW_Allocation_Mode_Support*.

When a Connection Manager changes *ADP_DP_CS_2.CM BW_Allocation_Mode_Support* bit, a DP IN Adapter shall:

- Set the *BW_Allocation_Capability_Changed* field to 1b in DP_TUNNELING_STATUS DPCD register.
- Set *DP_TUNNELING_IRQ* bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
- If *Unmask_BW_Allocation_IRQ* is 1b, generate an IRQ_HPDP.

DP BW Allocation Mode enablement is initiated by the DPTX only if both, the DP IN Adapter and the Connection Manager, support the DP BW Allocation Mode.

When DPTX sets DPTX_BW_ALLOCATION_MODE_CONTROL. *DP_Display_Driver_BW_Allocation_Mode_Enable* (E0030h, bit 7) to 1b, a DP IN Adapter shall:

- Enable DP BW Allocation Mode.
- Send the Connection Manager a Notification Packet with Event Code = DP_BW as defined in Table 6-12.

10.7.2 Interaction with DPTX

Table 10-24 lists the fields in the DPCD registers that are used by DPTX to negotiate bandwidth allocation with a Connection Manager. Table 10-25 describes how a DP IN Adapter maps the DPCD fields to Adapter Configuration Space.

Table 10-24. DPCD Bandwidth Allocation Registers

DPCD Register	Register Address	Bits	DPCD Field Type	DPCD Field Name
DP_TUNNELING_CAPABILITIES	E000Dh	[7]	Read Only	DP_IN_BW_Allocation_Mode_Support

DPCD Register	Register Address	Bits	DPCD Field Type	DPCD Field Name
USB4_DRIVER_ID	E000Fh	[3:0]	Read Only	USB4_Driver_ID
USB4_DRIVER_BW_CAPABILITY	E0020h	[7]	Read Only	USB4_Driver_BW Allocation Mode Support
DP_IN_ADAPTER_TUNNEL_INFORMATION	E0021h	[2:0]	Read Only	Group_ID
DP_BW_GRANULARITY	E0022h	[1:0]	Read Only	Granularity
ESTIMATED_BW	E0023h	[7:0]	Read Only	Estimated BW
ALLOCATED_BW	E0024h	[7:0]	Read Only	Allocated BW
DP_TUNNELING_STATUS	E0025h	[0]	Clearable, Read Only (Bit is cleared when 1 is written by way of an AUX_CH write transaction)	BW Request Failed
		[1]		BW Request Succeeded
		[2]		Estimated BW Changed
		[3]		BW_Allocation_Capability_Changed
DP_TUNNELING_MAX_LINK_RATE	E0028h	[7:0]	Read Only	DP_Tunneling_Max_Link_Rate
DP_TUNNELING_MAX_LANE_COUNT	E0029h	[7:0]	Read Only	DP_Tunneling_Max_Lane_Count
DPTX_BW_ALLOCATION_MODE_CONTROL	E0030h	[6]	Read/Write	Unmask_BW_Allocation_IRQ
		[7]	Read/Write	DP_Display_Driver_BW_Allocation_Mode_Enable
REQUESTED_BW	E0031h	[7:0]	Read/Write	Requested BW

Table 10-25. DP IN Adapter Configuration Space Mapping

DPCD Field Name	DPCD Field Type	DP IN Adapter Register	DP IN Field
USB4_Driver_BW Allocation Mode Support	Read Only	ADP_DP_CS_2	<i>CM BW Allocation Mode Support</i>
USB4_Driver_ID	Read Only	ADP_DP_CS_2	<i>CM_ID</i>
Group_ID	Read Only	ADP_DP_CS_2	<i>Group_ID</i>
Granularity	Read Only	ADP_DP_CS_2	<i>Granularity</i>
Estimated BW	Read Only	ADP_DP_CS_2	<i>Estimated BW</i>
Allocated BW	Read Only	DP_STATUS	<i>Allocated BW</i>
DP_Display_Driver_BW_Allocation_Mode_Enable	Read/Write	ADP_DP_CS_8	<i>DPTX BW Allocation Mode Enable</i>
Requested BW	Read/Write	ADP_DP_CS_8	<i>Requested BW</i>

When a DP IN Adapter receives a DPCD AUX Write transaction that targets a DPCD register within Table 10-25, and the targeted DPCD field Type is Read/Write, it shall update the corresponding field in Adapter Configuration Space with the value of the write transaction.

When a DP IN Adapter receives a DPCD AUX Read transaction that targets a DPCD register within Table 10-25, and the targeted DPCD field Type is Read Only, it shall update the read transaction with the value in the corresponding field in Adapter Configuration Space.

When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall:

- Store the current *Allocated BW* in an internal variable.

- If the recovery timer is advancing, stop and reset it.
- Initiate a bandwidth request handshake with the Connection Manager as defined in Section 10.7.3.

When a Connection Manager writes a value to the *Allocated BW* field that is equal to or greater than the Requested BW, a DP IN Adapter shall:

- Set the *BW Request Succeeded* field to 1b in DP_TUNNELING_STATUS DPCD register.
- Set the *DP_TUNNELING_IRQ* bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
- If the *Unmask_BW_Allocation_IRQ* bit is 1b, generate an IRQ_HPDP.
- If the *ESTIMATED_BW* field was locked for updates due to bandwidth request failure, unlock it.

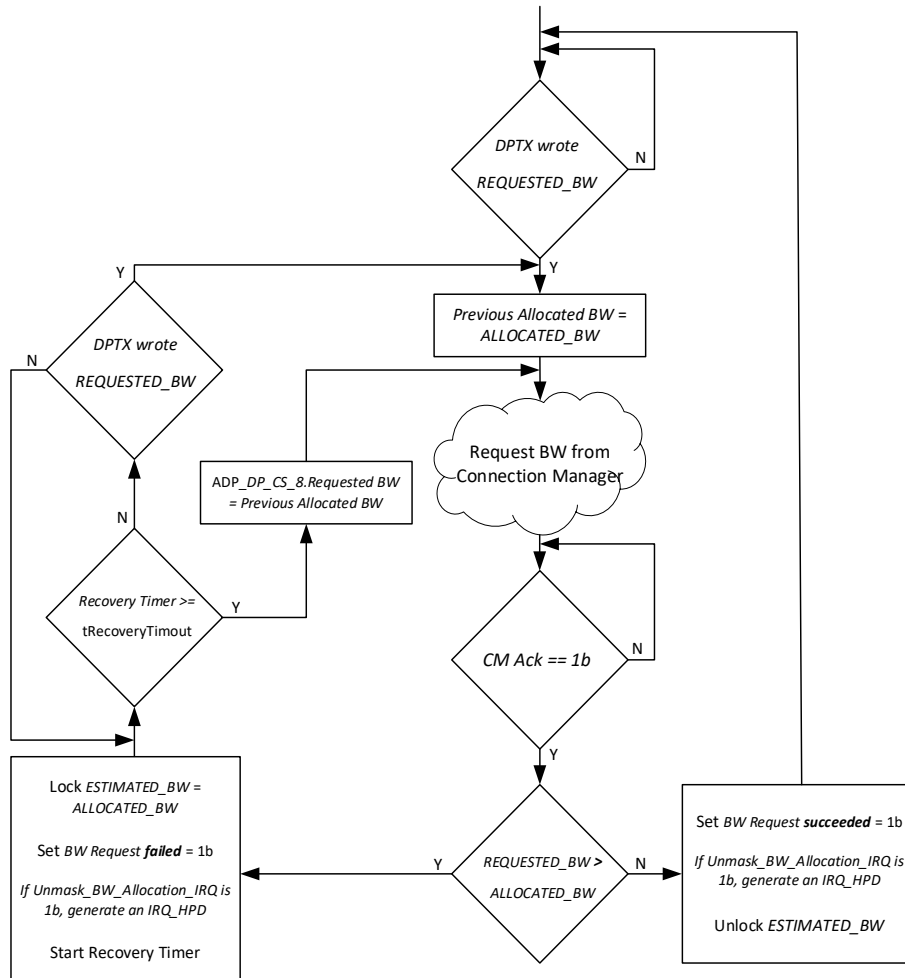
When a Connection Manager writes a value to the *Allocated BW* field that is smaller than the Requested BW, a DP IN Adapter shall:

- Set the *ESTIMATED_BW* field to the Allocated BW, and lock its value (i.e. ignore any changes in the *Estimated_BW* field).
- Set the *BW Request Failed* bit to 1b in DP_TUNNELING_STATUS DPCD register.
- Set the *DP_TUNNELING_IRQ* bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
- If the *Unmask_BW_Allocation_IRQ* bit is 1b, generate an IRQ_HPDP.
- Start the recovery timer.
- If the recovery timer has reached *tDPBWRecoveryTimeout*, the DP IN Adapter initiates a bandwidth allocation request. The DP BW that a DP IN Adapter requests shall be the same bandwidth as before the failed bandwidth allocation (i.e. the same value as in the *Allocated BW* field before the DPTX last updated the DPCD Requested BW register).

Note: When a DPTX writes to the REQUESTED_BW DPCD register, the DP IN Adapter should store the current Allocated BW in an internal variable. Then, in case of a tDPBWRecoveryTimeout timeout, the DP IN Adapter knows what Requested BW value to request.

A DP IN Adapter interacts with DPTX according to Figure 10-69.

Figure 10-69: DP IN Adapter Interaction with DPTX During DP BW Allocation



10.7.2.1 Estimated Bandwidth

Whenever the bandwidth allocation changes, the Connection Manager updates the available bandwidth by writing to ADP_DP_CS_2.Estimated BW field. Note that the *Estimated BW* field includes the bandwidth that is already allocated to the DP IN Adapter.

Upon a change in the *Estimated BW* field, a DP IN Adapter shall:

- Set the *Estimated BW Changed* bit in the DPCD DP_TUNNELING_STATUS register to 1b.
- Set the *DP_TUNNELING_IRQ* bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
- If the *Unmask_BW_Allocation_IRQ* bit is 1b, generate an IRQ_HPDP.

**CONNECTION MANAGER NOTE**

When there is a change in bandwidth across its Domain, the Connection Manager recalculates the estimated bandwidth for each DP IN Adapter in the Domain. The estimated bandwidth for a DP IN Adapter includes:

- *The bandwidth that has already been allocated to the DP IN Adapter.*
- *The available BW along the Path.*
- *Bandwidth that is allocated to the internal Host Controller, but not consumed*

After the estimated bandwidth is recalculated, a Connection Manager updates the ADP_DP_CS_2.Estimated BW field.

10.7.3 Interaction with the Connection Manager

When DPTX sends a DPCD AUX write transaction that targets the *REQUESTED_BW* field, a DP IN Adapter shall:

1. Set the ADP_DP_CS_8.DPTX Req field to 1b.
2. Send the Connection Manager a Notification Packet with Event Code = DP_BW as defined in Table 6-12.
3. Wait for the Connection Manager to set the ADP_DP_CS_2.CM Ack bit to 1b.
4. Set the ADP_DP_CS_8.DPTX Req field to 0b.
5. Wait for the Connection Manager to set the ADP_DP_CS_2.CM Ack bit to 0b.

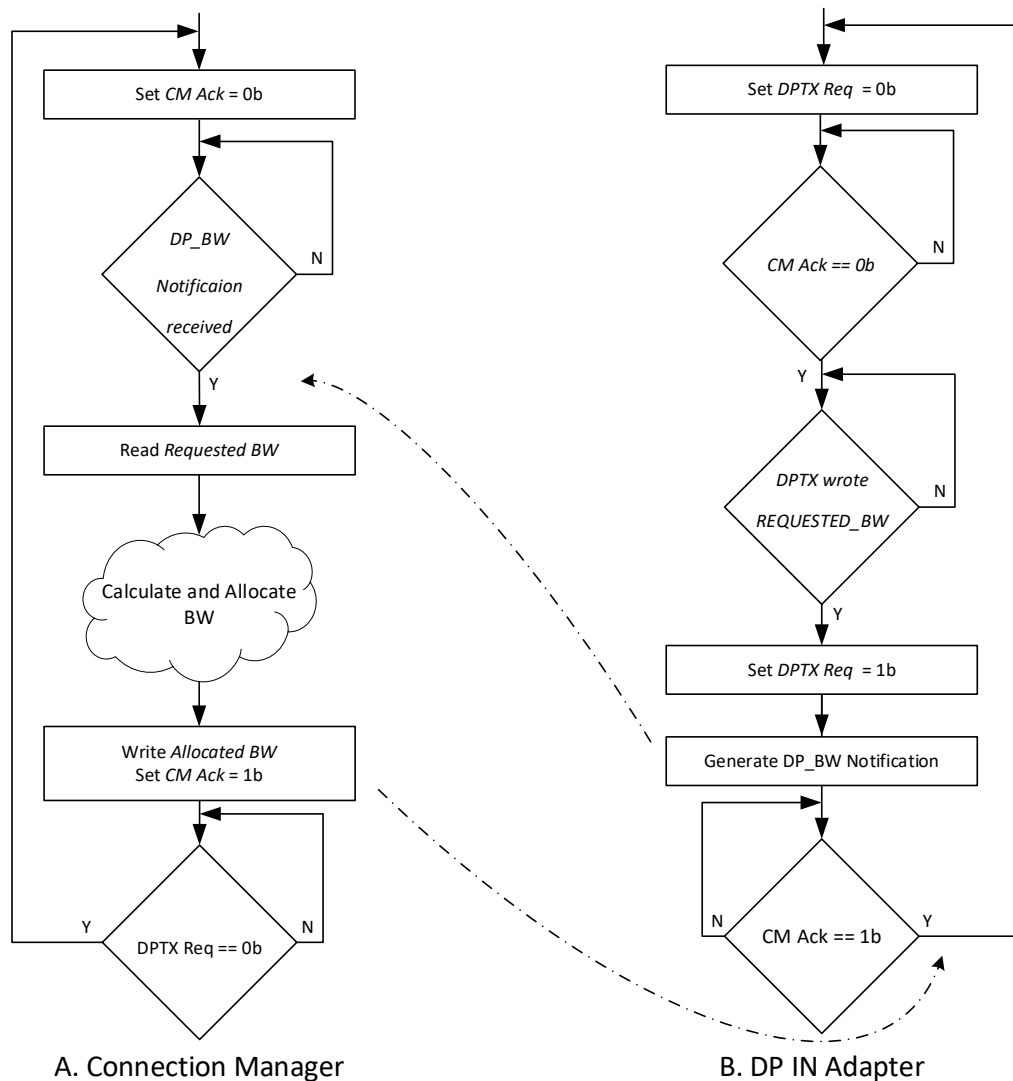
**CONNECTION MANAGER NOTE**

When a Connection Manager receives a DP_BW Notification Packet, it completes the following steps:

1. *Reads ADP_DP_CS_8.Requested BW.*
2. *Allocates bandwidth:*
 - a. *If the Request bandwidth is less than or equal to the currently allocated bandwidth, then the new allocation will be equal to the new requested bandwidth.*
 - *If the DP IN Adapter has a Group_ID different than zero, then for the following 10 seconds, the Connection Manager will reserve the released bandwidth to be allocated to DP IN Adapters with the same Group_ID.*
 - b. *Else, the Connection Manager tries to allocate bandwidth from the available bandwidth and by freeing bandwidth from other clients.*
3. *Writes the new allocated bandwidth to the DP_STATUS.Allocated BW field.*
4. *Sets the ADP_DP_CS_2.CM Ack bit to 1b.*
5. *Waits for the DP IN Adapter to set the ADP_DP_CS_8.DPTX Req bit to 0b.*
6. *Sets the ADP_DP_CS_2.CM Ack bit to 0b.*

A DP IN Adapter interacts with a Connection Manager according to Figure 10-70.

Figure 10-70: DP BW Allocation Interaction with Connection Manager



10.8 DP Discovery

Note: The term “Connector” in this section refers collectively to a Downstream facing USB Type-C port and/or a native DP connector. The native DP connector can be physical (e.g. an external DP port) or virtual (e.g. an internal DP connection).

10.8.1 DPRX Discovery

The DPRX Discovery feature enables system software to discover all the monitors that are connected to the topology. System software discovers the capability of a monitor by first setting a Virtual AUX Tunnel between a Host Interface Descriptor Ring and a DP OUT Adapter, then issuing AUX Requests and receiving AUX Responses over the Virtual AUX Tunnel. The Virtual AUX Tunnel is defined in Section 10.8.1.1.

A Device Router shall support DPRX Discovery through one of two options:

- **Full Implementation** – The Device Router implements a dedicated DP OUT Adapter for each Connector it supports. See Section 10.8.1.2.
- **Partial Implementation** – The Device Router implements less DP OUT Adapters than the number of Connectors that it supports. See Section 10.8.1.3.

10.8.1.1 Virtual AUX Tunnel

A Connection Manager builds the Virtual AUX Tunnel by setting two AUX Tunneled Paths:

1. An AUX outbound Path from a Host Interface Transmit Ring to either a DP OUT Adapter or a DP OUT AUX Adapter.
2. An AUX inbound Path from either the DP OUT Adapter or DP OUT AUX Adapter to a Host Interface Receive Ring.

Note: The system software that drives and consumes the Tunneled Packets to and from the Virtual AUX Tunnel acts as a DP IN Adapter. The Tunneled Packets over the Virtual AUX Tunnel are identical to the Tunneled Packets defined in Section 10.3.4.2.

10.8.1.2 Full Implementation

This section defines the requirements for a Device Router that supports DPRX Discovery through the Full Implementation option.

A Device Router that supports DPRX Discovery through the Full Implementation option shall set the *Partial DP Connectivity Implementation* bit to 0b.

The Device Router sends notifications for monitor plug and unplug events as defined in Section 10.3.3.1. The Device Router shall contain a DP OUT Adapter for each Downstream facing USB Type-C port on the Device Router and shall contain a DP OUT Adapter for each native DP connector it supports (i.e. the total number of DP OUT Adapters shall be equal to the number of Connectors supported).

10.8.1.3 Partial Implementation

This section defines the requirements for a Device Router that supports DPRX Discovery through the Partial Implementation option.

The Device Router shall set the *Partial DP Connectivity Implementation* bit to 1b.

The Device Router shall implement a DP OUT AUX Adapter, as defined in Section 10.8.1.3.1.

The Device Router shall support the following Router Operations:

- Get Connectors Information.
- Connect DP OUT Adapter.

The Device Router shall support the following modes, which depend on the value of the *SW Mapping* bit:

- HW Mapping Mode (*SW Mapping* = 0b; Default) – The Device Router autonomously controls the mapping of monitors to DP OUT Adapters. See Section 10.8.1.3.2.
- SW Mapping Mode (*SW Mapping* = 1b) – The Device Router maps monitors and DP OUT Adapters according to Connection Manager commands. See Section 10.8.1.3.3.

**CONNECTION MANAGER NOTE**

A Connection Manager shall not set the SW Mapping bit to 1b if the Partial DP Connectivity Implementation bit is set to 0b.

10.8.1.3.1 DP OUT AUX Adapter

A DP OUT AUX Adapter is used for discovering monitor capabilities through AUX Transactions.

A Device Router shall implement full connectivity between the DP OUT AUX Adapter and all Downstream facing USB Type-C connectors and between the DP OUT AUX Adapter and all native DP Connectors. The DP OUT AUX Adapter shall adhere to all the DP OUT Adapter requirements except the following:

- It shall not implement the Main-Link Path and the Main-Link DP Physical Layer. It therefore does not reconstruct Main-Link data and does not perform Link Training.
- It shall not implement the *Video Enable* bit. Therefore, Path Enable and Path Disable events are defined as when the *AUX Enable* bit is set to 1b and 0b, respectively.
- For AUX Transaction initiation, it shall operate in DPTX Only mode, as described in Section 10.3.1.

10.8.1.3.2 HW Mapping

When a Device Router operates in HW Mapping mode, it autonomously connects and disconnects monitors to and from the DP OUT Adapters. The Device Router sends notifications for monitor plug and unplug events as defined in Section 10.3.3.1.

10.8.1.3.3 SW Mapping

System software learns about the connectivity options between the DP OUT Adapters and the Connectors on a Device Router through the Get Connectors Information Router Operation. Through this operation it also learns the state of the current connectivity. See Section 8.3.1.3.6 for more information on the Get Connectors Information Router Operation.

When a Device Router is in SW Mapping mode, any change within the Device Router connectivity between a DP OUT Adapter and a Connector shall be done using a Connect DP OUT Adapter Router Operation. See Section 8.3.1.1.4 for more information on the Connect DP OUT Adapter Router Operation.

When a Device Router detects a Plug Event, an Unplug Event or an IRQ_HPD (as defined in the DisplayPort Specification) on a Connector number N, which is not connected to a DP OUT Adapter or a DP OUT AUX Adapter, it shall send the Connection Manager a Notification Packet with *Event Code* = DP_CON_CHANGE as defined in Table 6-12 with the following *Event Info*:

- *Connector Number* field equal to N.
- *IRQ_HPD* field set to 1b if IRQ_HPD was detected, otherwise set to 0b.
- *Plug/Unplug* field set to 1b if Plug was detected, otherwise set to 0b.

10.8.2 DPTX Discovery

The DPTX Discovery feature enables system software to discover the connectivity between a DPTX and a DP IN Adapter. System software can use this information to pair a specific DP IN Adapter with a DP OUT Adapter.

A Router may optionally support the DPTX Discovery feature. A Router that supports DPTX Discovery shall set the *DPTX Discovery Support* bit to 1b, otherwise it shall set this bit to 0b.

10.8.2.1 DP IN Adapter Requirements

A DP IN Adapter shall enter the DPTX Discovery state when the ADP_DP_CS_13.*DPTX Discovery Mode* bit is set to 1b.

Upon entering the DPTX Discovery state, a DP IN Adapter shall:

1. Set the DPCD DPTX_DISCOVERY_STATUS.*Discovery_Mode* bit (E002Dh, bit 0) to 1b.
2. Drive the HPD signal high.
3. Start the DPTX Discovery timer.

While in DPTX Discovery state:

- If a DP IN Adapter receives an AUX Request that is listed in Table 10-26, the DP IN Adapter shall reply with an AUX Response. The DP IN Adapter shall not forward the AUX Request to the DP Tunnel.
 - If the DPTX performs an AUX Write to a field listed in Table 10-27, the DP IN Adapter shall update the corresponding DP IN field as defined in Table 10-27.
 - If the DPTX sets DPCD DPTX_DISCOVERY_CONTROL.*Discovery_Done* bit (E00033h, bit 7) to 1b, the DP IN Adapter shall set the ADP_DP_CS_9.*Discovery Success* bit to 1b and shall send the Connection Manager a Notification Packet with Event Code = DPTX_DISCOVERY as defined in Table 6-12.
- If a DP IN Adapter receives an AUX Request that is not listed in Table 10-26 or the DPTX Discovery timer is equal or greater than tDPTXDiscoveryTimeout, a DP IN Adapter shall:
 1. Drop the AUX Request.
 2. Drive the HPD signal low.
 3. Set the ADP_DP_CS_9.*Discovery failure* bit to 1b.
 4. Send the Connection Manager a Notification Packet with Event Code = DPTX_DISCOVERY as defined in Table 6-12.
 5. Drop any incoming AUX Requests until it exits the DPTX Discovery state.

A DP IN Adapter shall exit the DPTX Discovery state when the ADP_DP_CS_13.*DPTX Discovery Mode* bit is set to 0b.

If the DP Paths are enabled when the *DPTX Discovery Mode* bit is set to 0b and the DPTX Discovery ended successfully, a DP IN Adapter shall keep the HPD signal high. Upon the first received HPD with the *P Flag* bit set to 1b, a DP IN Adapter shall:

1. Set DPCD DPTX_DISCOVERY_STATUS.*Discovery_Mode* bit (E002Dh, bit 0) to 0b.
2. Set DPCD DP_TUNNELING_STATUS.*Exit_Discovery_Mode* bit (E0025h, bit 4) to 1b.
3. Set DPCD LINK_SERVICE_IRQ_VECTOR_ESIO.*DP_TUNNELING_IRQ* bit (02005h, bit 5) to 1b.
4. Generate an IRQ_HP.

If the DP Paths are disabled when the *DPTX Discovery Mode* bit is set to 0b, a DP IN Adapter shall:

1. Set DPCD DPTX_DISCOVERY_STATUS.*Discovery_Mode* bit (E002Dh, bit 0) to 0b.
2. Drive the HPD signal low.

**CONNECTION MANAGER NOTE**

A Connection Manager which enables the DP Path while in DPTX Discovery Mode shall set the DPTX Discovery Mode bit to 0b after it enabled the Paths at the DP IN Adapter and before it enables the DP Paths at the DP OUT Adapter.

Table 10-26 lists the DPCD registers that the DPTX may use during the DPTX Discovery process. Table 10-27 describes how a DP IN Adapter maps the DPTX Discovery DPCD fields to Adapter Configuration Space.

Table 10-26. DPCD DPTX Discovery Registers

DPCD Register	Register Address	Bits	DPCD Field Type	DPCD Field Name
DPTX_DISCOVERY_STATUS	E002Dh	[0]	Read Only	Discovery_Mode
Router specific fields	E0000h–E000Bh	12x [7:0]	Read Only	IEEE_OUI, Device Identification String, Hardware Revision, Firmware/Software Major/Minor Revision
DP_TUNNELING_CAPABILITIES	E000Dh	[7:0]	Read Only	DP Tunneling Support, Panel Replay Tunneling Optimization Support, DP_IN_BW_Allocation_Mode_Support
DP_IN_ADAPTER_INFO	E000Eh	[5:0]	Read Only	DP_IN_Adapter_Number
USB4_DRIVER_ID	E000Fh	[3:0]	Read Only	USB4_Driver_ID
USB4_ROUTER_TOPOLOGY_ID	E001Bh–E001Fh	5x [7:0]	Read Only	Level 0/1/2/3/4 Lane Adapter Number
DP_TUNNELING_STATUS	E0025h	[4]	Write 1 to Clear/Read	Exit_Discovery_Mode
DPTX_DISCOVERY_CONTROL	E0033h	[7]	Read/Write	Discovery_Done
Source Device-specific field	00300h–0030Bh	12x [7:0]	Read/Write	IEEE_OUI, Device Identification String, Hardware Revision, Firmware/Software Major/Minor Revision
DPTX_DISCOVERY_CONTROL	E0033h	[3:0]	Read/Write	DPTX_Port_Number
DPTX_DISCOVERY_CONTROL	E0033h	[6:4]	Read/Write	DPTX_UNIQUE_ID

Table 10-27. DP IN Adapter Configuration Space Mapping for DPTX Discovery

DPCD Field Name	DPCD Field Type	DP IN Adapter Register	DP IN Field
DPTX_Port_Number	Read/Write	ADP_DP_CS_10	<i>DPTX_Port_Number</i>
DPTX_UNIQUE_ID	Read/Write	ADP_DP_CS_10	<i>DPTX_Unique_ID</i>
IEEE_OUI (Source Device-specific field)	Read/Write	ADP_DP_CS_10	<i>DPTX IEEE_OUI</i>
Device Identification String (Source Device-specific field)	Read/Write	ADP_DP_CS_11/ ADP_DP_CS_12	<i>DPTX Device Identification String</i>

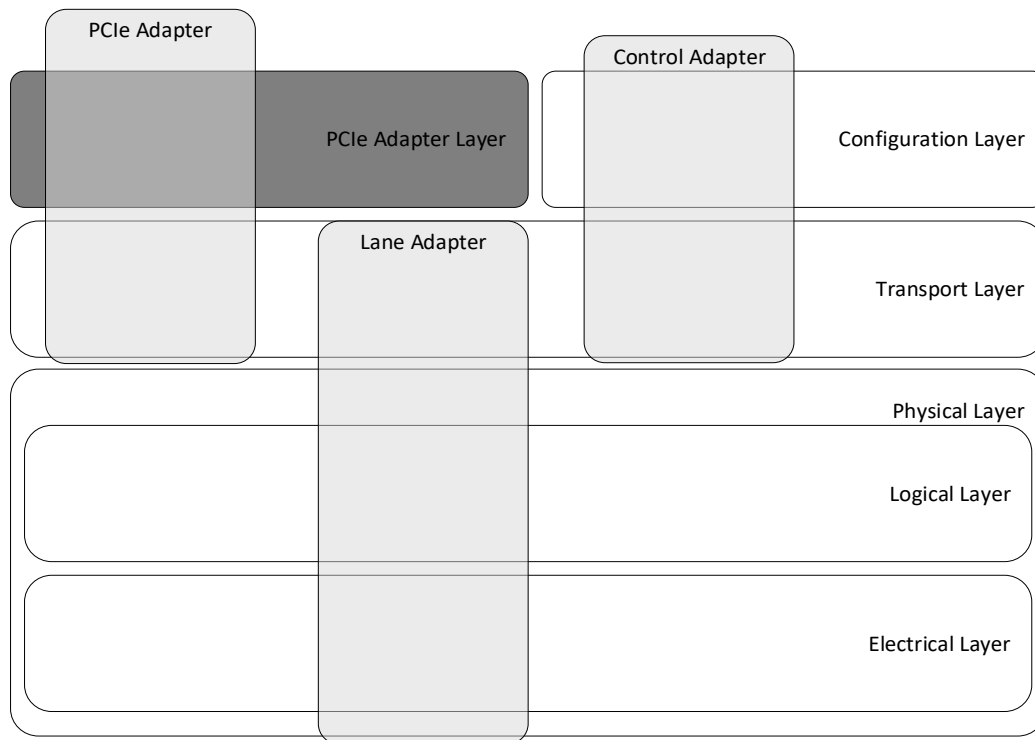
10.9 Timing Parameters

Table 10-28 lists the timing parameters for a DP Adapter.

Table 10-28. DP Adapter Timing Parameters

Parameter	Description	Min	Max	Units
tDPAckResponse	Maximum time between receiving a SET_CONFIG or HPD Packet and sending the corresponding ACK.	--	4	μs
tDPAckTimeout	Maximum time after sending a SET_CONFIG or HPD Packet that a DP Adapter waits for the corresponding ACK Packet.	--	400	μs
tDPSetConfigGap	Minimum time between receiving an ACK Packet and sending a SET_CONFIG Packet.	50 ¹	--	μs
tDPPlug	Maximum time a Router can wait after detection of a Source/Sink Connect/Disconnect before sending the corresponding Hot Plug/Hot Removal Event. Maximum time a DP OUT Adapter can wait after transitioning to the Paired state before sending an HPD Packet.	--	150	μs
tDPInit	Maximum time between receiving a SET_CONFIG Packet as part of DP Adapters Init Flow and responding with a SET_CONFIG Packet.	--	1	ms
tDPPLLAdjust	Maximum time between detecting an Adjust PLL Event and completing the PLL adjustment.	--	100	μs
tDPClockSync	Maximum time to send a DP Clock Sync Packet.	--	100	μs
tIRQDelay	The time a DP OUT Adapter waits after Link training is complete, before it sends SET_CONFIG IRQ.	200	300	μs
tDPBWRRecoveryTimeout	The time a DP IN Adapter waits for DPTX to request bandwidth in case of an allocation failure.	10	11	sec
tCMHSClear	Time between when the Connection Manager writes to the DP_STATUS_CTRL.CMHS and DP_STATUS_CTRL.UF fields and when the DP OUT Adapter sets the DP_STATUS_CTRL.CMHS bit to 0b.	--	5	ms
tDPTXDiscoveryTimeout	The time a DP IN Adapter waits for DPTX to complete the DPTX Discovery process.	10	11	sec
tDPALPMWake	For a DP IN Adapter, the maximum time between detecting LFPS and sending an ALPM DP Link Control Packet. For a DP OUT Adapter, the maximum time to start transmitting LFPS after receiving the ALPM DP Link Control Packet and the DP Link is in electrical idle.		3	μs
tDPAUXDelayIn	The maximum time between a DP IN Adapter receiving an AUX Request over the DP AUX and sending the AUX Request Tunneled Packet. The maximum time between a DP IN Adapter receiving an AUX Response Tunneled Packet and sending the AUX Response over the DP AUX.		45	μs
tDPAUXDelayOut	The maximum time between a DP OUT Adapter receiving an AUX Response over the DP AUX and sending the AUX Response Tunneled Packet. The maximum time between a DP OUT Adapter receiving an AUX Request Tunneled Packet and sending the AUX Request over the DP AUX.		10	μs
tDPAUXtoWAKE	The maximum time between a DP IN Adapter receiving the end of the AUX_SYNC pattern of an AUX Request over the DP AUX and sending the SET_CONFIG Packet of type AUX_PATH_CLX.		10	μs

Parameter	Description	Min	Max	Units
tDPAUXSleepHS	The maximum time between receiving the SET_CONFIG of type AUX_PATH_CLX with S/W set to 1b by a DP OUT Adapter until sending the PM Packet.		100	μs
<i>Notes:</i> 1. Unless specified otherwise, tDPSetConfigGap minimum value is 50 μs, for exception refer Section 10.4.15.1.2				

11 PCI Express Tunneling**USB4® Hosts:**

A USB4 Host may optionally support PCIe Tunneling. A USB4 Host that tunnels PCIe traffic does one of the following:

- Incorporate an internal PCIe Switch.
- Connect to a Root Complex via Root Ports.

The Host Router in a USB4 Host that supports PCIe Tunneling shall have one Downstream PCIe Adapter per Downstream Facing Port. Each Downstream PCIe Adapter shall interface to a downstream port of the internal PCIe Switch or Root Complex.

USB4 Hubs:

A USB4 Hub shall support PCIe Tunneling. A USB4 Hub shall contain an internal PCIe Switch.

The Device Router in a USB4 Hub shall have:

- An Upstream PCIe Adapter that interfaces to the internal PCIe Switch.
- For each Downstream Facing Port, a Downstream PCIe Adapter that interfaces to a downstream port of the internal PCIe Switch.

USB4 Devices:

A USB4 Device may optionally support PCIe Tunneling. A USB4 Device that tunnels PCIe traffic shall contain either an internal PCIe Switch or an internal PCIe Endpoint.

The Device Router in a USB4 Device that supports PCIe tunneling shall have an Upstream PCIe Adapter that interfaces to the internal PCIe Switch or Endpoint.

Note: In this Chapter, the term “Internal PCIe Port” refers to either an internal PCIe switch port, an internal PCIe endpoint upstream port, or a PCIe root complex downstream port.

Note: A reference to the PCIe Specification in this chapter refers to either Revision 4 or Revision 5.0 depending on the revision supported by the Internal PCIe Port.

A native PCIe device within a USB4 Hub or USB4 Device shall implement LTR.

11.1 PCIe Adapter Layer

11.1.1 Encapsulation

The PCIe Adapter Layer shall encapsulate the following PCIe constructs in Tunneled Packets:

- Transaction Layer Packets (TLP).
- Data Link Layer Packets (DLLP).
- Ordered Sets.
- Out-of-band events.

A PCIe Adapter Layer shall not encapsulate Idle Data Symbols into Tunneled Packets.

A PCIe Adapter Layer shall follow the rules below when encapsulating a PCIe construct into a Tunneled Packet:

- TLPs and DLLPs shall be encapsulated as defined in Section 11.1.1.1.3.
- Each Ordered Set shall be encapsulated into a separate Tunneled Packet.
- Each PCIe out-of-band event shall be encapsulated into a separate Tunneled Packet.
- The order of bytes and bits in the Tunneled Packet shall be identical to the original PCIe construct. The least-significant byte of the encapsulated construct is mapped to B0 in the Tunneled Packet Payload (see Figure 4-20). Bit 7 in each byte of the encapsulated construct is mapped to bit 7 in respective byte of the Tunneled Packet Payload.

The *PDF* field in a Tunneled Packet identifies the type of PCIe construct contained therein. Table 11-1 defines the PDF values that shall be used for each type of PCIe construct.

Table 11-1. PDF Values for PCIe Tunneled Packets

PDF	Type	Contents of Tunneled Packet
0h	Rsvd	Reserved.
1h	Ordered Set	One PCIe EIOS, TS1, or TS2 Ordered Set.
2h	Electrical Idle State	Indication of an Electrical Idle state on PCIe.
3h	TLP/DLLP	PCIe TLPs and/or DLLPs.
4h	TLP Next	TLP Payload that does not fit into a single Tunneled Packet.
5h	PERST Active	PCIe Reset (PERST) in active state.
6h	PERST Inactive	PCIe Reset (PERST) in inactive state.
7h	EDB	Indicates a nullified TLP.
8h – Fh	Rsvd	Reserved.

If a PCIe Adapter receives a Tunneled Packet with a Rsvd PDF value, it shall discard the Tunneled Packet and shall not send any Packets in response.

11.1.1.1 PCIe TLP and DLLP

When a PCIe Adapter Layer receives a Tunneled Packet with a pre-header that does not match any of the pre-headers defined in this section, it shall discard the packet and report the mismatch as a PCIe Receiver Error to the Internal PCIe Port.

11.1.1.1.1 Tunneled Packet Payload for TLP

This section defines the modifications in a PCIe TLP before it is encapsulated into a Tunneled Packet.

As shown in Figure 11-1, before encapsulation into a Tunneled Packet, a PCIe Adapter Layer shall:

1. Truncate a TLP by removing the STP Symbol, four leading Reserved bits, and the END or EDB Symbol.
2. Add the TLP Pre-Header defined in Table 11-2.

TLP bytes are mapped into the payload of a Tunneled Packet as shown in Figure 11-1. The TLP Pre-Header is mapped into byte B0 starting with the *Type* field. The truncated TLP immediately follows the TLP Pre-Header.

Figure 11-1. Tunneled PCIe TLP

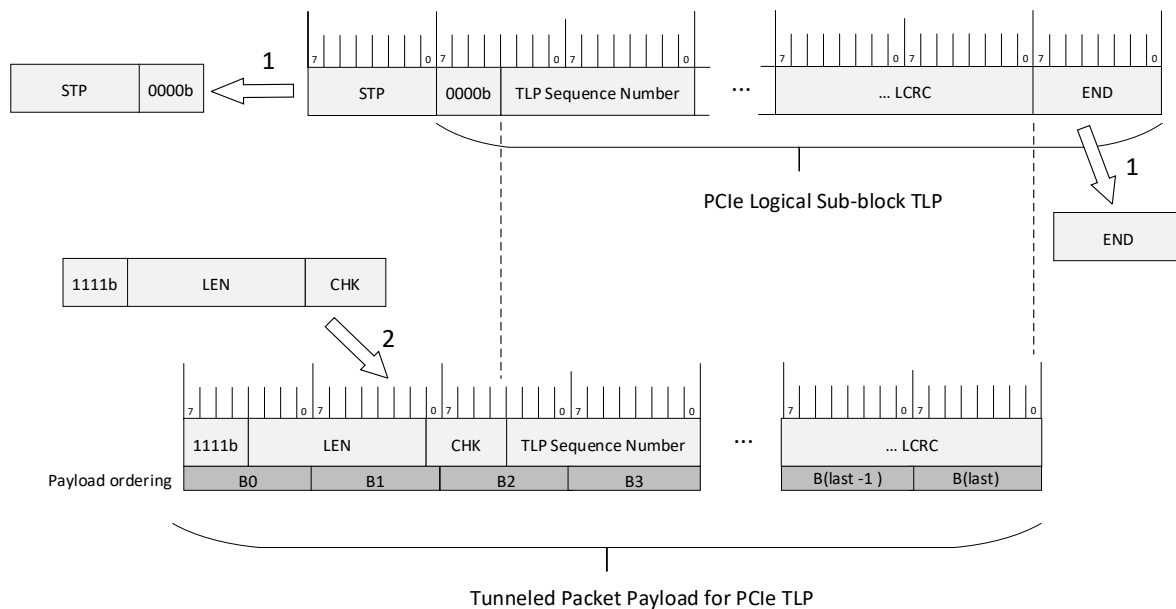


Table 11-2. TLP Pre-Header

Field	Size	Description
TYPE	4 bit	Identifies the PCIe construct. Set to 1111b for TLP.
LEN	11 bit	Length of TLP starting after the TLP <i>Sequence Number</i> field. Counted in DWs with a fix offset of 4. Value of 0 represents the minimum case of 4 DWs (TLP Header size of 3 DW plus 1 DW of LCRC). For example, with a Max Payload Size of 128 Bytes, a value of 38 represents the maximum case of 42 DWs (32 DW of TLP, plus 4 DW of maximal TLP Header, plus 1 DW of LCRC, plus 1 DW of TLP Digest, plus 4 DW of End-to-End TLP Prefix).

CHK	5 bit	<p>Error detection code on the vector, $V[14:0] = \{TYPE, LEN\}$. $CHK[3:0]$ are calculated as follows:</p> <ul style="list-style-type: none"> $CHK[0] = V[14] \wedge V[13] \wedge V[12] \wedge V[10] \wedge V[8] \wedge V[7] \wedge V[4] \wedge V[0]$ $CHK[1] = V[12] \wedge V[11] \wedge V[10] \wedge V[9] \wedge V[7] \wedge V[5] \wedge V[4] \wedge V[1]$ $CHK[2] = V[13] \wedge V[12] \wedge V[11] \wedge V[10] \wedge V[8] \wedge V[6] \wedge V[5] \wedge V[2]$ $CHK[3] = V[14] \wedge V[13] \wedge V[12] \wedge V[11] \wedge V[9] \wedge V[7] \wedge V[6] \wedge V[3]$ $CHK[4] = \text{XORing of } [14:0] \text{ bits.}$ <p>A PCIe Adapter Layer that receives a TLP Tunneled Packet with a mismatch in this field shall report the mismatch as a PCIe Receiver Error and the TLP shall be discarded.</p>
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11.1.1.1.2 Tunneled Packet Payload for DLLP

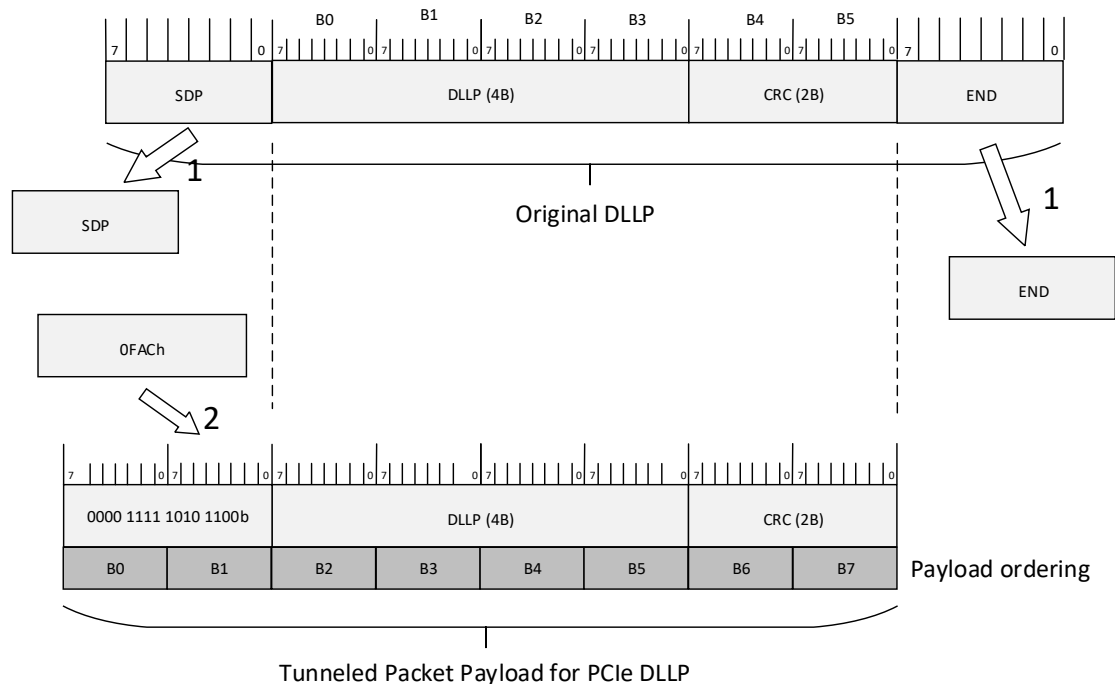
This section defines the modifications in a PCIe DLLP before it is encapsulated into a Tunneled Packet.

Before encapsulating a DLLP into a Tunneled Packet, a PCIe Adapter Layer shall:

1. Truncate a DLLP by removing the SDP Symbol and the END Symbol.
2. Add a DLLP Pre-Header of 0FACH to a DLLP as shown in Figure 11-2.

DLLP bytes are mapped into the payload of the Tunneled Packet as in Figure 11-2. The DLLP Pre-Header is mapped into bytes B0 and B1. The truncated DLLP immediately follows the DLLP Pre-Header.

Figure 11-2. Tunneled PCIe DLLP



11.1.1.1.3 DLLP and TLP Encapsulation

A PCIe Adapter Layer shall support all the following options for encapsulating DLLPs and TLPs into Tunneled Packets:

- Single TLP.
- 1 to N DLLPs:
 - When the *Extended Encapsulation* bit in the PCIe Adapter Configuration Capability is set to 0b, $N=2$.

- When the *Extended Encapsulation* bit in the PCIe Adapter Configuration Capability is set to 1b, N=3.
- 1 to M DLLPs followed by a single TLP:
 - When the *Extended Encapsulation* bit in the PCIe Adapter Configuration Capability is set to 0b, M=1.
 - When the *Extended Encapsulation* bit in the PCIe Adapter Configuration Capability is set to 1b, M=2.

Section 11.1.1.1.1 defines the structure of an encapsulated TLP. Section 11.1.1.1.2 defines the structure of an encapsulated DLLP.

If the total payload size of the encapsulated DLLPs and TLP is 252 bytes or less, the PCIe Adapter Layer shall encapsulate the DLLPs and/or TLP into a single Tunneled Packet with PDF = 3h.

- A nullified TLP shall be discarded and shall not be encapsulated.

If the total payload size of the encapsulated DLLPs and TLP exceeds 252 bytes, the PCIe Adapter Layer shall encapsulate the DLLPs and TLP into multiple Tunneled Packets according to the following rules:

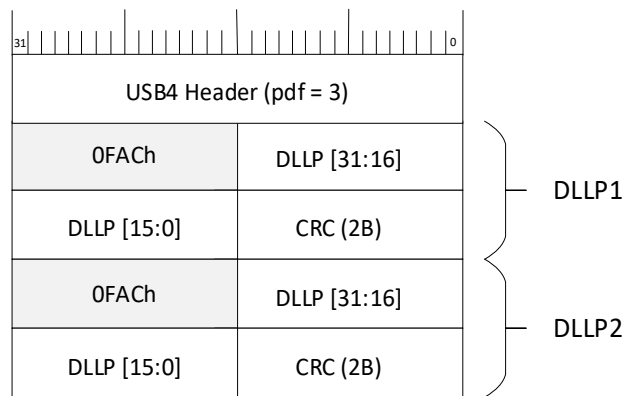
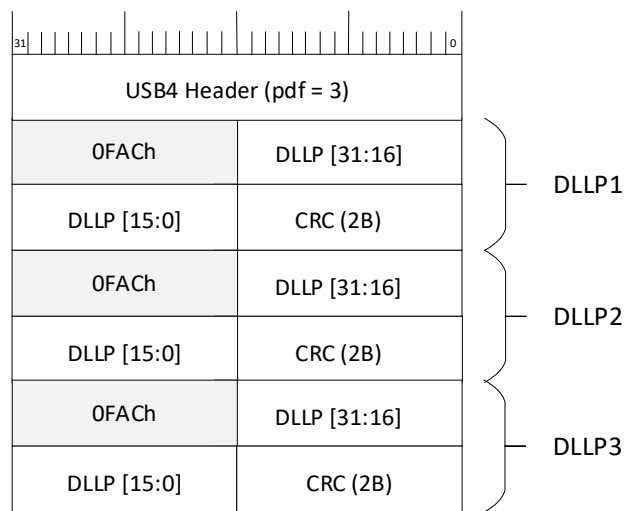
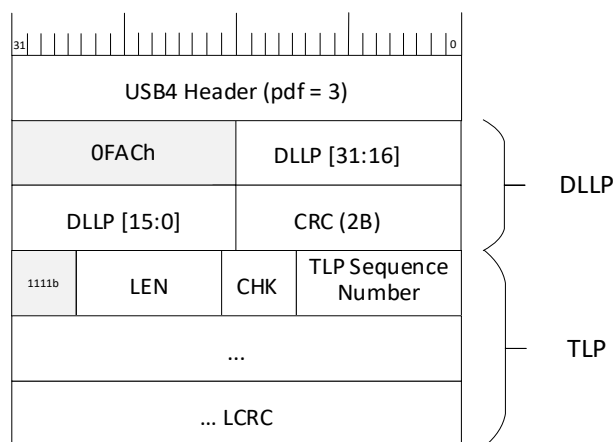
- All encapsulated DLLPs shall fit into the first Tunneled Packet.
- The encapsulated TLP shall be segmented into multiple Tunneled Packets.
 - All Tunneled Packets, with the possible exception of the last, shall contain 252B of payload.
 - The last Tunneled Packet shall contain up to 252B of payload.
- The first Tunneled Packet shall be assigned a PDF=3h.
- The following Tunneled Packets shall be assigned a PDF=4h.
- A nullified TLP may be discarded by the transmitting Router or may be transmitted over the tunnel. If the TLP is transmitted, the last Tunneled Packet for that TLP shall be assigned a PDF=7h as an EnD Bad (EDB) indication. Note that a nullified TLP may be truncated and have fewer DWs than specified by *Length* field in the PCIe Header.
- If a TLP is partially received over the USB4 Link (due to some USB4 Link error), the receiver may either drop the TLP or may deliver the partial TLP to the PCIe port with an EnD Bad (EDB) indication.

Note: When a Domain contains a USB4 Ver. 1 Router, the Ver. 1 Router supports PCIe Max Payload Size (MPS) of 128B only. That limits the whole PCIe sub-hierarchy to operate with MPS of 128B. Therefore, a Ver. 1 Router operating together with Ver. 2 Routers receives only PCIe TLPs that fit into a single USB4 Packet.



CONNECTION MANAGER NOTE

If the Routers on both ends of a USB4 Link support Version 2.0 of this specification, a Ver. 2 Connection Manager shall set the Extended Encapsulation bit to 1b. Otherwise, the Connection Manager shall set the Extended Encapsulation bit to 0b.

Figure 11-3. Encapsulation of Multiple DLLPs**Figure 11-4. Encapsulation of Multiple DLLPs (Extended Encapsulation is Enabled)****Figure 11-5. Encapsulation of 1 DLLP + 1 TLP into a Single Tunneled Packet**

- A PCIe Adapter Layer shall only transmit TS Ordered Sets that target Lane 0. TS Ordered Sets that target a non-zero Lane shall be discarded and shall not be send over the USB4 Fabric.
- A PCIe Adapter Layer shall modify a TS Ordered Set as defined in Table 11-3.

Table 11-3. TS Ordered Sets

PCIe Symbol Number	USB4 Byte Number	TS1 Contents	TS2 Contents
0	0	A PCIe Adapter Layer shall replace the COM Symbol with the value BCh.	Same as for TS1.
1	1	Link Number A PCIe Adapter Layer shall replace the PAD symbol with the value F7h. All other values are unchanged.	Same as for TS1.
2	2	Lane Number The PCIe Adapter Layer shall replace a PAD Symbol with the value F7h. Lane Number = 0 is unchanged.	Same as for TS1.
3	3	N_FTS The byte value is unchanged by the PCIe Adapter Layer.	Same as for TS1.
4	4	Data Rate Identifier The byte value is unchanged by the PCIe Adapter Layer.	Same as for TS1.
5	5	Training Control The byte value is unchanged by the PCIe Adapter Layer. Note that loopback request (Bit 2) is not supported.	Same as for TS1.
15:6	15:6	A PCIe Adapter Layer shall replace the D10.2 Symbol with the value 4Ah.	A PCIe Adapter Layer shall replace the D5.2 Symbol with the value 45h.

Receiver rules:

Upon receiving a TS Ordered Set from the Transport Layer, a PCIe Adapter Layer shall transfer the TS Ordered Set to the Internal PCIe Port.

**IMPLEMENTATION NOTE**

A PCIe Adapter Layer may send back-to-back identical copies of the TS Ordered Set to the PCIe Physical Layer Logical sub-block until either a different Transport Layer Packet is received or the LTSSM in the PCIe Physical Layer Logical sub-block enters a Configuration.Idle or Recovery.Idle state.

11.1.1.2.2 Electrical Idle Ordered Sets (EIOS)

When a PCIe Adapter Layer receives an Electrical Idle Ordered Set (EIOS) from the Internal PCIe Port, it shall send two consecutive EIOS Tunneled Packets over the USB4 Fabric. An EIOS shall be encapsulated in a Tunneled Packet with payload as defined in Table 11-4.

Table 11-4. Electrical Idle Ordered Sets

Symbol	Contents
0	COM Symbol with the value BCh.
1 – 3	IDL Symbol with the value 7Ch.

A PCIe Adapter Layer that receives an EIOS Tunneled Packet shall:

1. Transfer the EIOS to the Internal PCIe Port.
2. Indicate Rx Electrical Idle to the Internal PCIe Port.

11.1.1.3 Electrical Idle State

Upon detecting that a PCIe Physical Layer Logical sub-block is in Electrical Idle state, a PCIe Adapter Layer shall send at least 3 Electrical Idle State Tunneled Packets. The payload for an Electrical Idle State Tunneled Packet shall consist of one DW that contains a value of 0000 0000h.

A PCIe Adapter Layer that receives an Electrical Idle State Tunneled Packet shall indicate Rx Electrical Idle to the Internal PCIe Port.

When a PCIe Adapter Layer receives a Tunneled Packet that is not an Electrical Idle State Tunneled Packet or an EIOS Tunneled Packet, it shall stop indicating Rx Electrical Idle to the Internal PCIe Port.

11.1.1.4 PERST

11.1.1.4.1 PERST Tunneled Packets

PERST Active and PERST Inactive Tunneled Packets are used to propagate PCIe PERST# assertion and de-assertion. A Router shall send PERST Active and PERST Inactive packets only from a Downstream PCIe Adapter. The payload for a PERST Active Tunneled Packet and a PERST Inactive Tunneled Packet shall consist of one DW that contains a value of 0000 0000h.

11.1.1.4.2 PERST Activation in a Host Router

Upon detecting an assertion of PERST# on a Downstream PCIe Adapter, a Host Router shall:

1. Discard any queued Tunneled Packet in the PCIe Adapter Layer.
2. Send at least three PERST Active Tunneled Packets on the Downstream PCIe Adapter if its *Path Enable* bit is set to 1b.

11.1.1.4.3 PERST Activation in a Device Router

When a Device Router enters the Uninitialized Unplugged state, it shall assert PERST# on its internal PCIe upstream port.

When a Device Router receives a PERST Active Tunneled Packet, or the *Path Enable* bit in the Upstream PCIe Adapter is set to 0b, it shall:

1. Discard any Tunneled Packets that are queued in a PCIe Adapter Layer.
2. Send at least 3 PERST Active Tunneled Packets on all Downstream PCIe Adapters that have the *Path Enable* bit set to 1b.
3. Assert PERST# on its internal PCIe upstream port.

While PERST# is asserted, a Downstream PCIe Adapter Layer shall discard any received PCIe Tunneled Packets. The Adapter Layer shall not send any PCIe Tunneled Packets except for the PERST Active Tunneled Packets.

11.1.1.4.4 PERST Inactivation in a Host Router

Upon detecting a de-assertion of PERST# on a Downstream PCIe Adapter, a Host Router shall send at least 3 PERST Inactive Tunneled Packets on the Downstream PCIe Adapter if its *Path Enable* bit is set to 1b.

11.1.1.4.5 PERST Inactivation in a Device Router

After receiving a PERST Active Tunneled Packet, or after the *Path Enable* bit in the Upstream PCIe Adapter changes from 0b to 1b, if a Device Router receives any PCIe Tunneled Packet other than a PERST Active Tunneled Packet on its Upstream PCIe Adapter, it shall:

1. Send at least 3 PERST Inactive Tunneled Packets on all Downstream PCIe Adapters that have the *Path Enable* bit set to 1b.
2. De-assert PERST# on its internal PCIe upstream port.

After PERST# is de-asserted, a Downstream PCIe Adapter Layer shall not forward to the Internal PCIe Port any Ordered Sets, packets, or events that were received before or during PERST# assertion.

11.1.2 USB4 Hot-Plug

When a Device Router is hot-plugged, the Upstream PCIe Adapter in the hot-plugged Router shall maintain the Internal PCIe Port in PCIe Warm Reset. The Device Router shall maintain the Warm Reset until either a PERST Inactive Tunneled Packet or a PCIe TS Ordered Set is received by the Upstream PCIe Adapter.

11.1.3 Flow Control

A PCIe Adapter shall not discard a PCIe TLP or DLLP due to lack of credits in the USB4 Link. When credits are not available, the Router shall queue the PCIe TLP and shall transport it once sufficient credits become available. When credits are not available, a Router may hold off creation of new DLLPs.

**IMPLEMENTATION NOTE**

The amount of buffering at the PCIe Adapter is implementation specific as it balances the tradeoff between PCIe tunneling performance and PCIe link latency. It is recommended that implementations make the amount of buffers configurable.

11.1.4 PCIe Wake**11.1.4.1 Router is in the Sleep State**

A Device Router that detects a PCIe Wake event from any connected PCIe Endpoint or Switch, and the *Sleep Ready* bit in Router Configuration Space is set to 1b shall process the wake as defined in Section 4.5.

If a PCIe wake event happens after the *Sleep Ready* bit is set to 1b but before the Device Router is in sleep state, the Device Router shall wait for entry to sleep state and then process the wake as defined in Section 4.5.

11.1.4.2 Router is in the Enumerated state

A Device Router in the Enumerated state shall send a Notification Packet upstream with the Event Code = PCIE_WAKE (see Section 6.5) when all the following are true:

- The Upstream PCIe Adapter detects a PCIe Wake event from the connected PCIe Endpoint or Switch.
- The *Enumerated State PCIe Wake* bit in Router Configuration Space is set to 1b.
- The *Sleep Ready* bit in Router Configuration Space is set to 0b.

If the *Enter Sleep* bit is set to 1b while the Device Router is processing a wake event and a Notification Packet has not been sent yet, the Router shall finish processing the wake event (including sending a Notification Packet and receiving a Notification Acknowledgement) before it sets the *Sleep Ready* bit to 1b.

A Host Router that receives a Notification Packet with Event Code = PCIE_WAKE shall:

- Generate a PCIe wake indication to the host system. The mechanism for waking the host system is outside the scope of this specification.
- Forward the Notification Packet to the Connection Manager.

Note: Version 1.0 Routers do not support PCIe wake when the Router is not in the sleep state. If a Device Router sends a Notification Packet with Event Code = PCIE_WAKE to a Version 1.0 Host Router, the Host Router will not wake the host system.

11.2 Internal PCIe Ports

This section defines the functionality of an Internal PCIe Port that interfaces to a PCIe Adapter. An Internal PCIe Port shall be compatible with the PCI Express® Base Specification, Revision 4. An Internal PCIe Port may be compatible with the PCI Express® Base Specification, Revision 5.0. Each Internal PCIe Port that interfaces to a PCIe Adapter shall implement a Physical Layer Logical sub-block, a Data Link Layer, and a Transaction Layer as defined in the PCIe Specification with the modifications, configurations, and parameters described in this section.

The Logical sub-block only supports PCIe Gen 1. The PCIe link width can be any value supported by the PCIe Specification and may be different at the Upstream Adapter and Downstream Adapter.

11.2.1 PCIe Physical Layer Logical Sub-block

The Logical sub-block shall update the PCIe configuration registers with the following characteristics:

- PCIe Gen 1 protocol behavior.
- *Max Link Speed* field in the Link Capabilities Register set to 0001b (data rate of 2.5 GT/s only).

Note: These settings do not represent actual throughput. Throughput is implementation specific and based on the USB4 Fabric performance.

11.2.1.1 Encoding

The Physical Layer Logical sub-block shall:

- Not scramble the bits it delivers to the PCIe Adapter Layer.
- Not de-scramble the bits it receives from the PCIe Adapter Layer, regardless of the Disable Scrambling bit received in the TS Ordered Set.

11.2.1.2 Link Training and Status State Machine (LTSSM)

The Physical Layer Logical sub-block shall implement a Link Training and Status State Machine (LTSSM). The LTSSM shall support the L1 state. The LTSSM shall not support the following:

- Loopback state.
- L0s state.
- L1 PM substates.
- Changes in PCIe link speed.
- Lane-to-Lane de-skew.
- Inferring Electrical Idle in states other than L0.

- Inferring Electrical Idle in L0 state by absence of Flow Control Update DLLPs is optional.

Note: Negotiation and Reduction of PCIe link width is not applicable as the only TS which traverse over the tunnel are TS for Lane 0.

The following changes shall also apply to the LTSSM:

- A PCIe Upstream port in Recovery.idle shall transition to L0 state when it receives a TLP or DLLP. If the port does not receive any TLP or DLLP, it shall transition to the L0 state t_{Recovery} time after it entered the Recovery.idle state.

Note: The t_{Recovery} wait period is needed to detect a possible transition to Disabled state or to Hot Reset State.

A PCIe downstream port, shall immediately send UpdateFC after transitioning from L1 to L0.

It is recommended that a PCIe port transmit at least 16 TS1 after receiving the first TS1 during Recovery.RcvrLock.



IMPLEMENTATION NOTE

Idle Data Symbols are not sent over the USB4 Fabric. Therefore, a receiving Internal PCIe Port cannot depend on the reception of Idle Data Symbols in its LTSSM. One possible implementation is that the PCIe Adapter Layer generates the Idle Data Symbols towards the Internal PCIe Port before transitioning to L0 state. Another possible implementation is for the LTSSM to proceed from either Configuration.Idle state or Recovery.Idle state to L0 state without reception of any Idle Data Symbols. Note that TS2 Ordered Sets received after the transition to L0 state are ignored until a Tunneled Packet containing a construct other than a TS2 Ordered Set is received.

11.2.1.3 ASPM L1 Entry

The following rules shall be implemented in order to avoid ambiguity in ASPM L1 handshake termination when the PCIe downstream port responds with the PM_Active_State_Nak message:

- The PCIe upstream port shall send no more than 10 additional PM_Active_State_Request DLLPs after sending an ACK DLLP for the received PM_Active_State_Nak message.
- After receiving the ACK DLLP for the PM_Active_State_Nak message, the PCIe downstream port shall wait 9.5 microseconds as described in the PCIe Specification. The Port shall also drop the first 10 PM_Active_State_Request DLLPs it receives, including DLLPs received after expiration of the 9.5 microseconds period. However, if it receives a TLP or DLLP which is not a PM_Active_State_Request DLLP, it may optionally not drop the next PM_Active_State_Request DLLPs.

11.2.1.4 Clock Tolerance Compensation

Clock tolerance compensation shall not be performed.

11.2.1.5 Compliance Mode

Compliance Mode shall not be supported.

11.2.1.6 Clock Power Management

Clock Power Management shall not be supported.

11.2.2 PCIe Data Link Layer

An Internal PCIe Port shall implement a PCIe Data Link Layer as defined in the PCIe Specification.

11.2.3 PCIe Transaction Layer

The Transaction Layer shall support:

- The PCIe Latency Tolerance Reporting (LTR) mechanism. The Latency Tolerance Reporting LTR Capability shall be implemented in the PCIe upstream port.
- PCIe hot-add and hot-removal ("hot-plug").

In a USB4 Hub, the Transaction Layer shall additionally support:

- Access Control Services (ACS) as described in the PCIe Specification with ACS P2P Egress Control required. Note that support for ACS P2P Egress Control is optional in the PCIe Specification.
- Flattening Portal Bridge (FPB).

It is recommended that a Transaction Layer also support Downstream Port Containment (DPC) Extended Capability.

The Transaction Layer shall not support local TLP Prefix and Protocol MUXing.

A USB4 Host needs to be hardened against malicious devices and malformed requests. The Transaction Layer in an Internal PCIe Port in a USB4 Host, in conjunction with the System Software, needs to be able to provide appropriate protection against requests from rogue endpoints. The mechanism to provide such protection is implementation specific, but System Software needs certain functionality to be provided by the hardware.

In a USB4 Host, the Transaction Layer shall additionally provide functionality to:

- Ensure that a transaction received on the PCIe Root Port is appropriate for the Requester ID. This can be done using ACS Source Validation or by an implementation-specific mechanism that is more appropriate for the architecture of the Host.
- Allow blocking of Upstream Memory Requests with the *AT* field set to a value other than the default. This can be done using ACS Translation Blocking or by an implementation-specific mechanism that is more appropriate for the architecture of the Host. When Upstream Memory Requests are not blocked the following applies:
 - A Host supporting ATS Translation Services shall check and filter any request marked "Translated" to ensure that the transaction is from the provided SourceID and the PCIe Function is permitted to access the specific address range needed by the transaction.
 - A Host that is not supporting ATS and does not block Upstream Memory Requests delivered with non-default *AT* field values, may use a proprietary method for implementing external address translation, with equivalent (or improved) functionality to ATS, as long as it can authenticate the source, and guarantee that it is privileged for address translation.
 - A Host that is neither supporting ATS nor an equivalent scheme shall never agree to process Upstream Memory Requests without qualifying the source and translating the address accordingly.
- Provide per-source address filtering (and optionally translation). This can be done with an IOMMU or other implementation-specific structures. It is recommended that a USB4 Host use a mechanism that allows System Software to revoke mappings with low performance overhead.

It is recommended that the USB4 Host also provide:

- Flattening Portal Bridge or equivalent to improve the scalability and runtime reallocation of Routing ID and Memory Space resources.

11.2.3.1 PCIe Link Timers (Informative)

As the delay through PCIe tunnel may vary, it is recommended that a Router implement PCIe link timer ranges listed in Table 11-5.

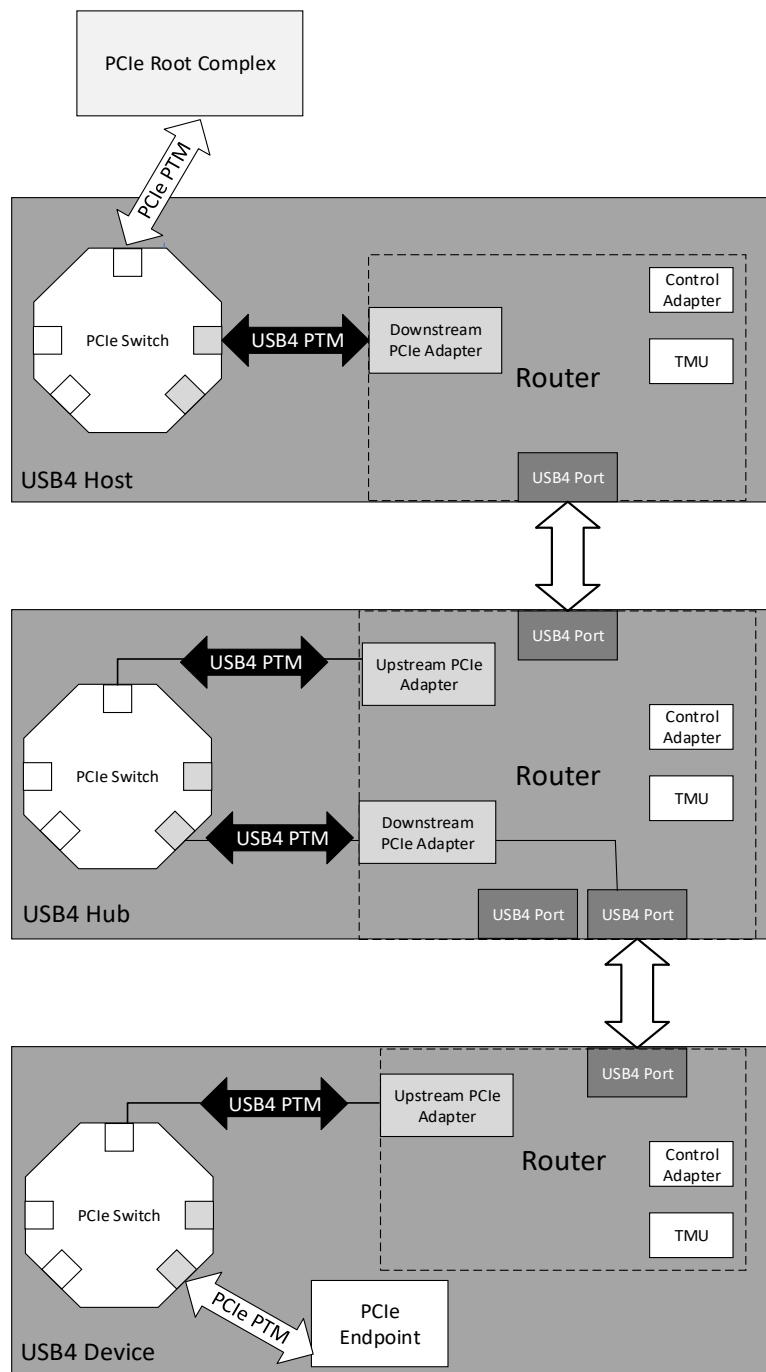
Table 11-5. PCIe Link Timer Ranges

Timer	Min	Max	PCIe Specification Reference
UpdateFC	30 [μs]	100 [μs]	2.6.1.2 FC Information Tracked by Receiver
Retrain Link	200 [μs]	1 [ms]	2.6.1.2 FC Information Tracked by Receiver
Replay	10 [μs]	256 [μs]	3.5.2.1 LCRC and Sequence Number Rules (TLP Transmitter)
L1 Reject	9.5 [μs]	128 [μs]	5.4.1.2.1. Entry into the L1 State See the PCIe Specification, Implementation Note titled <i>ASPM L1 Accept/Reject Considerations for the Upstream Component</i>

11.2.4 Precision Time Measurement (PTM) Mechanism

A USB4 Hub shall support PTM as defined in the PCIe Specification with the modifications in this section. It is recommended that a USB4 Host also support PTM. If a USB4 Host supports PTM, it shall do so as defined in this section.

The modified PTM link protocol runs between a PCIe Adapter Layer and an Internal PCIe Port within a Router. When PCIe traffic is tunneled through more than one Router, the PTM link protocol runs on each Router that the PCIe traffic traverses. Physical PCIe Ports perform the PCIe PTM link protocol without any modifications.

Figure 11-7: Example of PTM Relationships

A PTM link protocol that runs across a USB4 Fabric needs to be adjusted for the additional latency added by the Fabric. This is done by calculating a mathematical relationship between the PTM Master Time and the TMU Host Router Time at one Router, then using that relationship to reconstruct the PTM Master Time from TMU Host Router Time samples at downstream Device Routers.

There are two parameters that characterize the relationship between the PTM Master Time and the TMU Host Router Time. These parameters are called TMU_to_PTM_A and TMU_to_PTM_B. Together, they are referred to as the TMU_to_PTM Parameters.

Note: If the Domain operates in Inter-Domain mode and it is a follower, then the Host Router Time refers to the Inter-Domain Host Router Time defined in Section 7.4.2. Otherwise, it refers to Host Router Time defined in Section 7.4.1.

There is one Router that calculates the TMU_to_PTM Parameters. This Router is referred to as the Parameter Generator. A Router that reconstructs PTM Master Time is referred to as a Parameter Consumer. The TMU_to_PTM Parameters are propagated throughout a USB4 Fabric via ResponseD messages.

Note: USB4 buffering and arbitration methods can introduce random and varying delays in a USB4 Fabric. Furthermore, the propagation delay between PTM messages is not symmetrical. Because of this the PTM link protocol described in the PCIe specification does not give sufficient accuracy without modification.

11.2.4.1 Parameter Generator

The following Routers shall act as a Parameter Generator:

- A Host Router with its PTM function enabled.
- A Device Router with its PTM function enabled and the *Root Select* bit in its PTM Control Register set to 1b.

A Parameter Generator shall calculate the TMU_to_PTM Parameters as defined in Section 11.2.4.3.1. It is recommended that a Parameter Generator calculate the TMU_to_PTM Parameters periodically, similar to PTM periodic calculation. Periodic calculations increase accuracy.

Instead of the *PTM Master Time* and *Propagation Delay* fields defined in the PCIe Specification, a Parameter Generator shall include the most recent TMU_to_PTM Parameters in the PTM ResponseD Message. The format and example of a PTM ResponseD over the PCIe Tunnel is depicted in Figure 11-8.

Figure 11-8: PTM ResponseD Tunneled Packet Format

31

0

PDF = 3	*	HOP ID	Length = 1Ch	HEC
{TYPE,LEN[10:7]} = F0h		{LEN[6:0],CHK[4]} = 05h	{CHK[3:0],TLP Seq[11:8]} = 70h	TLP Seq[7:0] = 1Bh
Header 0 = 74h		Header 1 = 00h	Header 2 = 00h	Header 3 = 01h
Header 4 = 56h		Header 5 = 20h	Header 6 = 00h	Header 7 = 53h
TMU_to_PTM_B [63:56] = F2h		TMU_to_PTM_B [55:48] = 44h	TMU_to_PTM_B [47:40] = E9h	TMU_to_PTM_B [39:32] = 09h
TMU_to_PTM_B [31:24] = FDh		TMU_to_PTM_B [23:16] = 97h	TMU_to_PTM_B [15:8] = 7Eh	TMU_to_PTM_B [7:0] = 03h
TMU_to_PTM_A [7:0] = 5Dh		TMU_to_PTM_A [15:8] = F5h	TMU_to_PTM_A [23:16] = 1Ah	TMU_to_PTM_A [31:24] = 80h
LCRC[31:24] = EBh		LCRC[23:16] = 5Dh	LCRC[15:8] = E2h	LCRC[7:0] = 5Ah

* SupplID

Note: TMU_to_PTM_A[7:0] is sent first.

If the *Time Disruption* bit is set to 1b in Router Configuration Space, a Parameter Generator shall not reply with a PTM ResponseD Message to a PTM Request.

11.2.4.2 Parameter Consumer

A Device Router shall act as Parameter Consumer if its PTM function is enabled and the *Root Select* bit in its PTM Control Register is set to 0b.

The Parameter Consumer shall not reply with a PTM ResponseD Message to a PTM Request if any of the following conditions are true:

- The *Time Disruption* bit is set to 1b in Router Configuration Space.
- TMU_to_PTM Parameters were not received after the *Time Disruption* bit was cleared.
- A rule in the PCIe Specification forbids sending a PTM ResponseD Message.

When sending a PTM ResponseD Message through a Downstream PCIe Adapter, a Parameter Consumer shall use the PTM ResponseD Message format defined in Figure 11-8. The TMU_to_PTM Parameters in the ResponseD Message shall be the same as the last TMU_to_PTM Parameters received on the Upstream PCIe Adapter.

When sending a PTM ResponseD Message to a Native Downstream PCIe Port, a Parameter Consumer shall use the PTM ResponseD Message format defined in the PCIe Specification. The Parameter Consumer shall calculate the PTM Master Time for the PTM ResponseD Message as defined in Section 11.2.4.3.2.

11.2.4.3 PTM Calculations

11.2.4.3.1 TMU_to_PTM Parameters

The TMU_to_PTM Parameters represent the linear relationship between the PTM Master Time and the TMU Host Router Time. TMU_to_PTM_A is a 32-bit number that represents the slope of the linear line. TMU_to_PTM_B is a 64-bit number that represents the PTM Master Time intercept of the linear line. The TMU_to_PTM Parameters are formatted as follows:

- TMU_to_PTM_A
 - TMU_to_PTM_A is a 32-bit fixed-point value, with the binary point between bit 31 and bit 30.
 - TMU_to_PTM_A[31] is 0b for values in the range (0,1) (excluding 0 and 1) and is 1b for values in the range [1,2) (including 1 and excluding 2).
 - TMU_to_PTM_A[30:0] is a binary representation of the fraction part of TMU_to_PTM_A.
 - For example, the value 0.5 is represented by 400...0h and the value 1.5 is represented by C00...0h.
- TMU_to_PTM_B
 - TMU_to_PTM_B[63:0] value is in nanoseconds and is in 2's complement notation

The TMU_to_PTM Parameters are calculated from two samples of PTM Master Time and the *Nanosecond* field of the TMU Host Router Time ((tmu0, ptm0) and (tmu1, ptm1)). In general the TMU_to_PTM Parameters can be calculated by solving the following set of equations:

$$\text{ptm0} = \text{TMU_to_PTM_A} * \text{tmu0} + \text{TMU_to_PTM_B}$$

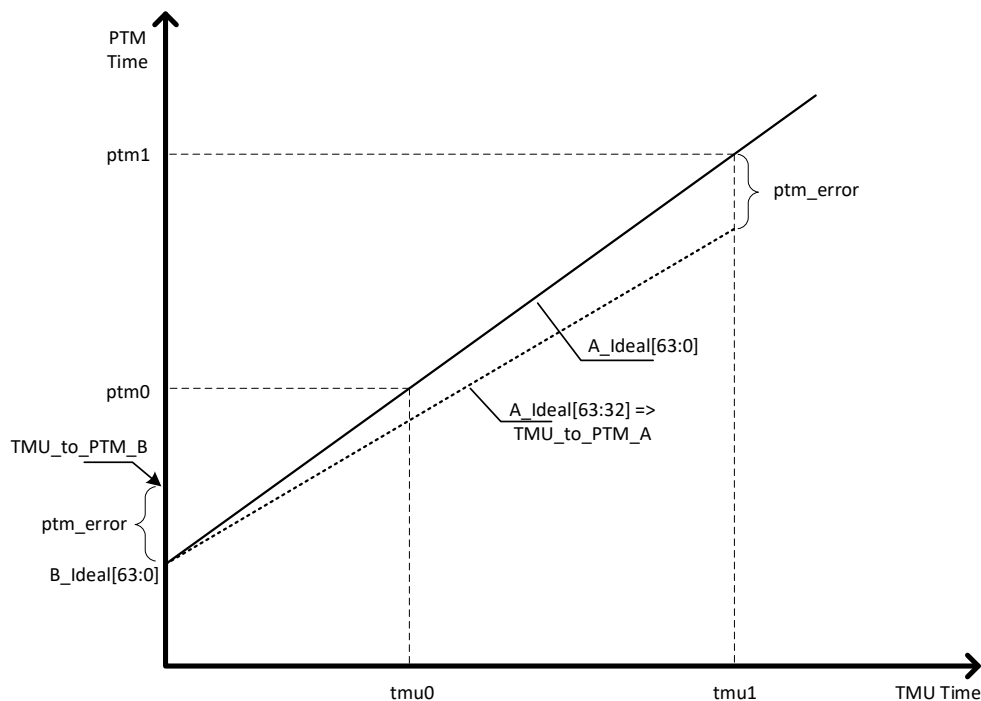
$$ptm1 = TMU_to_PTM_A * tmu1 + TMU_to_PTM_B$$

However, quantization error can occur when using the equations above because the TMU_to_PTMA is only 32 bits wide. To compensate for any quantization error, a Parameter Generator shall calculate the TMU_to_PTMA Parameters as follows:

1. Calculate the ideal 64-bit parameters:
 - $A_ideal[63:0] = (ptm1 - ptm0) / (tmu1 - tmu0)$
 - where $A_ideal[63:0]$ is a 64-bit fixed-point value with the binary point between bit 63 and bit 62.
 - $B_ideal[63:0] = ptm1 - A_ideal[63:0] * tmu1$
 - where B_ideal is a 64-bit signed integer in 2's complement notation.
2. Calculate the ptm_error at $ptm1$ point using the 32 bits representation of the slope:
 - $ptm_error = ptm1 - (A_ideal[63:32] * tmu1 + B_ideal[63:0])$
 - where ptm_error is a 64-bit signed integer in 2's complement notation.
3. Assign the TMU to PTM Parameters:
 - $TMU_to_PTM_A[31:0] = A_ideal[63:32]$
 - $TMU_to_PTM_B[63:0] = B_ideal[63:0] + ptm_error$

Figure 11-9 shows the relationships between the terms used in the calculation above.

Figure 11-9: TMU to PTM Parameters Illustration



IMPLEMENTATION NOTE

It is recommended that a Parameter Generator apply filtering to any measured values before calculating the TMU_to_PTM Parameters.

11.2.4.3.2 PTM Master Time Reconstruction

A Parameter Consumer shall reconstruct the PTM Master Time as follows:

$$\text{PTM_Master_Time}(t) = \text{TMU_to_PTM_A} * \text{TMU_time}(t) + \text{TMU_to_PTM_B}$$

where:

- TMU_time(t) is the *Nanosecond* field of the TMU Host Router Time.
- TMU_to_PTM_A and TMU_to_PTM_B are the most recent TMU_to_PTM Parameters received on the Upstream Facing Port.

11.2.5 Timing Parameters

Table 11-6 lists the timing parameters for an Internal PCIe Port.

Table 11-6. PCIe Adapter Timing Parameters

Parameter	Description	Min	Max	Units
tRecovery	Time in the Recovery.Idle state before transitioning to L0 state, in the absence of DLLP or TLP. Applicable only for a PCIe upstream port.	200	--	μs

11.3 Paths

A PCIe Adapter Layer shall put HopID = 8 in the header of an outgoing Tunneled Packet before handing it off to the Transport Layer for routing.



CONNECTION MANAGER NOTE

A Connection Manager shall configure PCIe Paths with the Dedicated Flow Control Buffer Allocation scheme.

A Connection Manager shall configure the Output HopID to be 8 for the segment of a PCIe Path that goes from a USB4 Port to a PCIe Adapter.

11.3.1 Path Set-Up

Before setting up a Path, the Router does not indicate in-band presence to the Internal PCIe Port. The Internal PCIe Port LTSSM is in the Detect state.

When the *Path Enable* bit is set to 1b, a Router shall indicate in-band presence to the Internal PCIe Port. The PCIe Adapter Layer shall also enable sending of PCIe Tunneled Packets to the Transport Layer.

When an Internal PCIe Port detects an in-band presence, it shall:

- Transition its LTSSM to the Polling state.
- Generate a PCIe interrupt to indicate a hot plug event to software.

**CONNECTION MANAGER NOTE**

A Connection Manager shall configure all PCIe Paths, then set the Path Enable bit to 1b in the PCIe Adapters at either end of the Path.

The Connection Manager shall wait for the following before it enables a PCIe Path in an Adapter:

- *The previous PCIe Path set for the Adapter (if any) completed its teardown flow.*
- *The LTSSM in the PCIe Port is in the Detect state, as reflected in PCIe Adapter Configuration Space. This allows stabilization of the PCIe link after the previous tunnel teardown, and to facilitate fast and reliable reconnect.*

11.3.2 Path Teardown

When the *Path Enable* bit is set to 0b in its PCIe Adapter Configuration Capability (including a DFP disconnect, see Section 4.4.5.2.1), a PCIe Adapter shall:

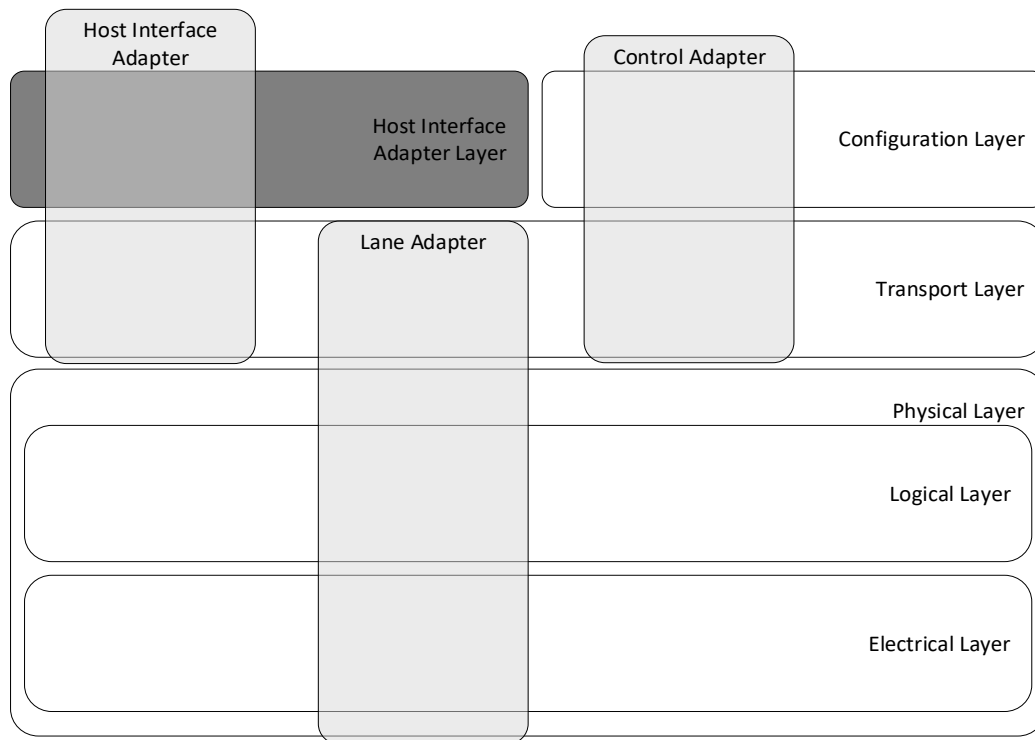
- Disable sending of PCIe Tunneled Packets from the PCIe Adapter Layer to the Transport Layer.
- If the PCIe Adapter is a Downstream PCIe Adapter, clear the In-band Presence indication to the Internal PCIe Port.
- If the PCIe Adapter is an Upstream PCIe Adapter, drive PERST# as defined in Section 11.1.1.4.
- Set the *Extended Encapsulation* bit to its default value.

When an Internal PCIe Port detects that the in-band presence indicator is cleared, it shall:

- Transition its LTSSM the Detect state. It is recommended that the LTSSM not wait the full amount of time defined in the PCIe Specification before transitioning to the Detect state.
- Generate a PCIe interrupt to indicate a hot removal event to software.

**CONNECTION MANAGER NOTE**

Before tearing down a PCIe Path, a Connection Manager shall set the Path Enable bit in the PCIe Adapter Configuration Capability to 0b.

12 Host Interface

This chapter defines the Host Interface Adapter Layer within a Host Interface Adapter.

A Host Router shall implement a single Host Interface Adapter Layer as defined in Sections 12.1 through 12.4 and Section 12.7. A PCIe Host Router shall also implement the PCIe-specific Host Interface Adapter Layer functionality defined in Sections 12.5 and 12.6. A non-PCIe Host Router shall implement functionality equivalent to that defined in Sections 12.5 and 12.6. The method to do so is system specific.

A Host Interface Adapter Layer shall implement N Transmit Descriptor Rings and N Receive Descriptor Rings, where $N \geq 3$. For any given HopID n (where $n = 0$ through $N - 1$), the Transmit Descriptor Ring is referred to as “Transmit Ring n ” and the Receive Descriptor Ring is referred to as “Receive Ring n ”. For example, the Transmit Descriptor Ring for HopID 0 is referred to as Transmit Ring 0 and the Receive Descriptor Ring for HopID 0 is referred to as Receive Ring 0.

A Host Router shall support operation with a Connection Manager that interfaces to the Router via Transmit Ring 0 and Receive Ring 0. The Connection Manager may be implemented in Host system software (an “external Connected Manager”), or it may be implemented in Host Router firmware or hardware (an “embedded Connection Manager”). If a Host Router has an embedded Connection Manager, it shall implement a mechanism to disable the embedded Connection Manager.

Note: A Host Router needs to operate with an external Connection Manager so that compliance testing can be performed. Transmit Ring 1 and Receive Ring 1 are used for compliance testing, but can be used for other purposes as well.

A Device Router shall not contain a Host Interface Adapter.

12.1 Descriptor Ring Mode

Transmit Ring 0 and Receive Ring 0 shall operate in Raw Mode only. All other Descriptor Rings shall support operation in both Raw Mode and Frame Mode. For a PCIe Host Interface Adapter Layer, the mode of operation for a Descriptor Ring is determined by the *Raw Mode* bit.

12.1.1 DW, Byte, and Bit Order

Data Buffers, Transmit Descriptors, and Receive Descriptors shall be stored in host memory in the following manner:

- For a Data Buffer: the lowest-addressed byte of data shall be mapped to bits [31:24] of the first payload DW depicted in Figure 5-1. The following addressed byte shall be mapped to bits [23:16] of the first payload DW depicted in Figure 5-1, and so on.
- For a Transmit Descriptor: the lowest-addressed byte of descriptor data in memory shall be mapped to bits [7:0] of the first DW of the Transmit Descriptor depicted in Figure 12-4. The following addressed byte shall be mapped to bits [15:8] of the first DW of the Transmit Descriptor depicted in Figure 12-4, and so on.
- For a Receive Descriptor: the lowest-addressed byte of descriptor data in memory shall be mapped to bits [7:0] of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6. The following addressed byte shall be mapped to bits [15:8] of the first DW of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6, and so on.
- Within each byte, bit[i] in host memory shall be mapped to bit[i] in the corresponding byte of the Data Buffer, Transmit Descriptor, or Receive Descriptor.

A PCIe Host Interface Adapter Layer shall map the payload of a PCIe TLP into a Transport Layer Packet payload, Transmit Descriptor, or a Receive Descriptor in the following manner:

- For a Transport Layer Packet: Data Byte 0 in the PCIe TLP payload, shall be mapped to bits [31:24] of the first payload DW depicted in Figure 5-1. Data Byte 1 in the PCIe TLP payload, shall be mapped to bits [23:16] of the first payload DW depicted in Figure 5-1, and so on.
- For a Transmit Descriptor: Data Byte 0 in the PCIe TLP payload shall be mapped to bits [7:0] of the first DW of the Transmit Descriptor depicted in Figure 12-4. Data Byte 1 in the PCIe TLP payload shall be mapped to bits [15:8] of the first DW of the Transmit Descriptor depicted in Figure 12-4, and so on.
- For a Receive Descriptor: Data Byte 0 in the PCIe TLP payload shall be mapped to bits [7:0] of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6. Data Byte 1 in the PCIe TLP payload shall be mapped to bits [15:8] of the first DW of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6, and so on.
- Within each byte, bit[i] in the PCIe TLP payload shall be mapped to bit[i] in the corresponding byte of the Transmit Descriptor, Receive Descriptor, or Transport Layer Packet payload.

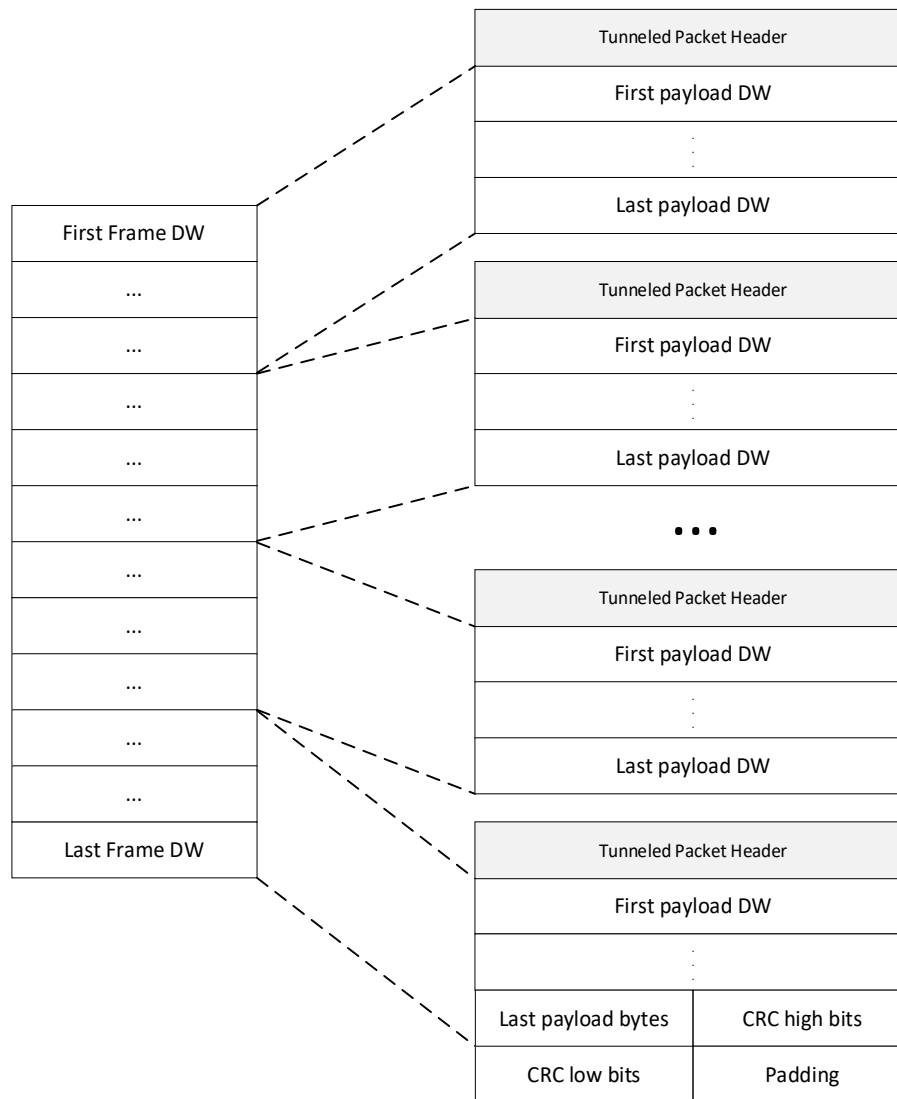
12.1.2 Raw Mode

In Raw Mode, the Host sends bytes over the USB4® Fabric by forming the payload of a Transport Layer Packet (either a Control Packet for Ring 0 or a Tunneled Packet for non-zero Rings) and posting it in a Data Buffer in Host Memory. The Host Router returns bytes to the Host by posting the payload of a Transport Layer Packet to a Data Buffer in Host Memory. Each Data Buffer holds the payload of one Transport Layer Packet.

12.1.3 Frame Mode

In Frame Mode, a Host groups bytes to be sent over the USB4 Fabric into Frames. A Frame shall be between 1 byte and 4096 bytes in length.

A Host Interface Adapter Layer segments a Frame into one or more Tunneled Packets as shown in Figure 12-1. The Tunneled Packet types used by a Host Interface Adapter in Frame Mode are defined in Table 12-1.

Figure 12-1. Segmentation of a Frame**Table 12-1. Frame Mode Tunneled Packet Format**

Type	Segment	PDF
<i>Start of Frame</i>	Payload shall contain the first segment of a Frame. This Tunneled Packet type shall only be used when the Frame is segmented into more than one Tunneled Packet.	PDF value shall be taken from the <i>SOF PDF</i> field in the first Transmit Descriptor of the Frame (see Section 12.3.1).
<i>Middle of Frame</i>	Payload shall contain an intermediate segment of a Frame. This Tunneled Packet type shall only be used when the Frame is segmented into more than two Tunneled Packet.	0h

Type	Segment	PDF
<i>End of Frame</i>	Payload shall contain the last segment of a Frame when the Frame is segmented into more than one Tunneled Packet. Payload shall contain the full Frame when the Frame is not segmented into more than one Tunneled Packet. Payload shall include the complete 32-bit CRC.	PDF value shall be taken from the <i>EOF PDF</i> field in the last Transmit Descriptor of the Frame (see Section 12.3.1).

12.2 End-to-End (E2E) Flow Control

The Host Interface Adapter Layer employs an end-to-end (E2E), credit-based flow control mechanism to prevent overflow of a Receive Descriptor Ring. Flow control is managed individually for each Receive Descriptor Ring and for each Transmit Descriptor Ring.

A Host Interface Layer shall not use E2E flow control for Transmit Ring 0 or Receive Ring 0.



CONNECTION MANAGER NOTE

The Connection Managers at either end of a Host-to-Host Path shall ensure that both ends of the Path to have the same flow control scheme.

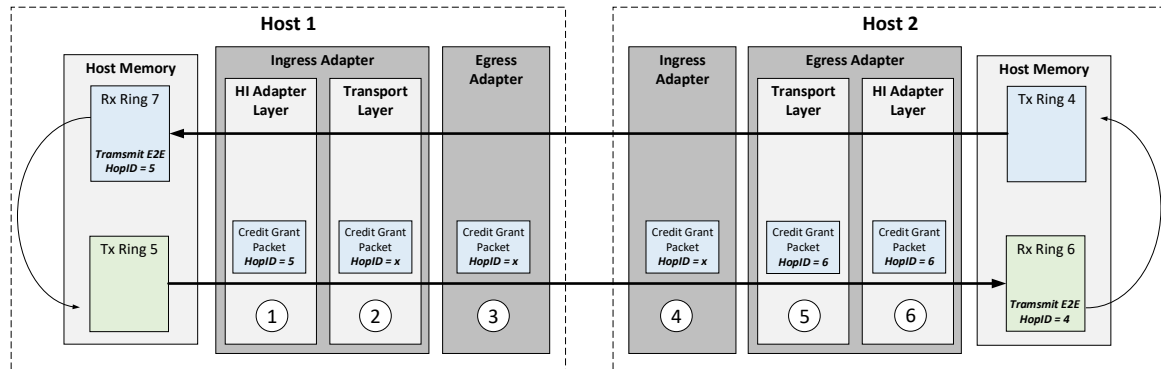
12.2.1 E2E Flow Control Packets

12.2.1.1 E2E Credit Grant Packet

This packet is used to transmit credit information from a Receive Descriptor Ring to a Transmit Descriptor Ring. An E2E Credit Grant Packet shall include the header in Table 12-2 followed by the payload defined in Table 12-3.

Figure 12-2 shows an example of how an E2E Credit Grant Packet is sent from a Receiving Host Interface (Host 1) to a Transmitting Host Interface (Host 2). The Receiving Host is the Host that received data in a Receive Descriptor Ring. The Transmitting Host is the Host that sends data from a Transmit Descriptor Ring. In the example, the following steps take place:

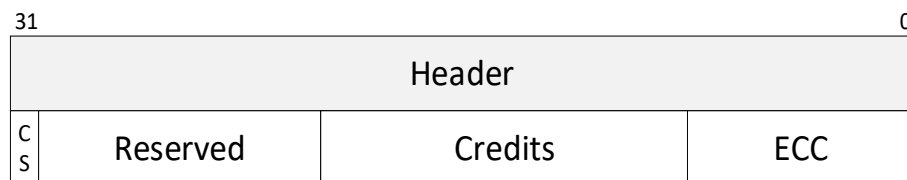
1. The Host Interface Layer in Host 1 generates an E2E Credit Grant Packet for Receive Ring 7. The HopID in the E2E Credit Grant Packet is equal to the *Transmit E2E HopID* field for Receive Ring 7 (HopID=5).
2. The HopID in the E2E Credit Grant Packet is updated according to the Routing Table in the Ingress Adapter. HopID x is set by the Connection Manager during Path Setup and can be any valid HopID.
3. The Ingress Adapter in Host 1 forwards the E2E Credit Grant Packet to the Egress Adapter indicated in its Routing Table. The Egress Adapter forwards the Packet to Host 2.
4. The E2E Credit Grant Packet is forwarded along the Inter-Domain Path between Transmit Ring 5 and Receive Ring 6. The Ingress Adapter in Host 2 receives the E2E Credit Grant Packet with HopID x.
5. The Ingress Adapter in Host 2 updates the HopID of the E2E Credit Grant Packet according to its Routing Table. The Connection Manager configures the Routing Table during Path Setup so that the new HopID is 6. After updating the HopID, the Ingress Adapter forwards the Packet to the Egress Adapter.
6. When the Host Interface Layer in Host 2 gets the E2E Credit Grant Packet, it looks at the *Transmit E2E HopID* field for Receive Ring 6 to see which Transmit Ring the Packet applies to. Because the value in the *Transmit E2E HopID* field is 4, the Host Interface Adapter Layer applies the Packet to Transmit Ring 4.

Figure 12-2. Example of Forwarding an E2E Credit Grant Packet**Table 12-2. E2E Credit Grant Packet Header**

Bits	Field	Value
7:0	<i>HEC</i>	See Section 5.1.2.1.1
15:8	<i>Length</i>	04h
22:16	<i>HopID</i>	Contains the HopID of a Path that terminates at the destination of this Credit Grant Packet and corresponds to the target Transmit Descriptor Ring. See Figure 12-2. For a PCIe Host Interface Adapter Layer, the inserted HopID value shall be the same value as in the <i>Transmit E2E HopID</i> field (Section 12.6.3.2.5).
26:23	<i>Rsvd</i>	Reserved
27	<i>SuppID</i>	0b
31:28	<i>PDF</i>	Fh

Table 12-3. E2E Credit Grant Packet Payload

Bits	Field	Value
7:0	<i>ECC</i>	Error Correction – Error correction field that is calculated over bits [31:8] of the E2E Credit Grant Packet payload. See Section 5.1.2.3 for calculation.
20:8	<i>Credits</i>	Credits – Indicates the total number (modulo 8192) of credits granted to the target Transmit Descriptor Ring since initialization.
30:21	<i>Rsvd</i>	Reserved
31	<i>CS</i>	Credit Sync – Shall be set to 0b.

Figure 12-3. E2E Credit Grant / Sync Packet Format

12.2.1.2 E2E Credit Sync Packet

This packet synchronizes the credit count between a Transmit Descriptor Ring and a Receive Descriptor Ring. An E2E Credit Sync Packet shall include the header in Table 12-4 followed by payload defined in Table 12-5.

Table 12-4. E2E Credit Sync Packet Header

Bits	Field	Value
7:0	<i>HEC</i>	See Section 5.1.2.1.1
15:8	<i>Length</i>	04h
22:16	<i>HopID</i>	Contains the HopID that corresponds to the Transmit Descriptor Ring that the packet applies to.
26:23	<i>Rsvd</i>	Reserved
27	<i>SuppID</i>	0b
31:28	<i>PDF</i>	Fh

Table 12-5. E2E Credit Sync Packet Payload

Bits	Field	Value
7:0	<i>ECC</i>	Error Correction – Error correction field that is calculated over bits [31:8] of the E2E Credit Sync Packet payload. See Section 5.1.2.3 for calculation.
20:8	<i>Credits</i>	Credits Raw Mode: Represents the number (modulo 8192) of credits consumed by the Transmit Descriptor Ring up to (and including) the last packet transmitted prior to this E2E Credit Sync Packet. Frame Mode: Represents the number (modulo 8192) of credits consumed by the Transmit Descriptor Ring. The number of credits includes all Frames sent prior to the E2E Credit Sync Packet. It does not include any partially sent Frames.
30:21	<i>Rsvd</i>	Reserved
31	<i>CS</i>	Credit Sync – Shall be set to 1b.

12.2.2 Flow Control Rules**12.2.2.1 Credit Update**

Credits are used to track the number of Receive Descriptors allocated for a Receive Descriptor Ring. Credits shall be given in units of Receive Descriptors where one credit corresponds to one Receive Descriptor.

12.2.2.2 Credit Counter Synchronization

If an E2E Credit Grant Packet is lost for any reason, the next successfully received E2E Credit Grant Packet corrects credit tracking in the transmitting Host Interface.

If an E2E flow controlled Tunneled Packet sent by a Host Interface is dropped or otherwise lost for any reason, the Receiving Host Interface credit counter loses synchronization with the Transmitting Host Interface. In order to re-establish synchronization, a Transmitting Host Interface sends E2E Credit Sync Packets periodically to the Receiving Host Interface.

12.2.2.3 Transmitting Host Interface Rules

The Host Interface Adapter Layer determines if sufficient credits have been advertised to permit the transmission of a Tunneled Packet from the Transmitting Host Interface:

- If E2E flow control is disabled for the Transmit Descriptor Ring, the Host Interface Adapter Layer shall not require any credits to be available before transmitting a Tunneled Packet from this Transmit Descriptor Ring.

- If E2E flow control is enabled for the Transmit Descriptor Ring and the Ring is in Raw Mode, the Host Interface Adapter Layer shall not transmit a Tunneled Packet unless at least one credit for the corresponding Transmit Descriptor Ring is available.
- If E2E flow control is enabled for the Transmit Descriptor Ring and the Ring is in Frame Mode, the Host Interface Adapter Layer shall not transmit a Tunneled Packet unless at least one credit for the corresponding Transmit Descriptor is available for the Frame.

A Transmitting Host Interface Adapter Layer shall not send E2E Credit Sync Packets for a Transmit Descriptor Ring with E2E flow control disabled or when the egress Link is in a Low Power state.

When a Transmitting Host Interface Adapter Layer receives a Credit Grant Packet, it shall verify the *ECC* field value in the Credit Grant Record.

- The Adapter Layer shall correct any single-bit errors. After correcting an error, the Adapter Layer shall continue on as if the error had never occurred.
- If an uncorrectable error is detected, the Credit Grant Packet shall be dropped.

The following is a recommended scheme using state variables to manage credits for each Transmit Descriptor Ring enabled with E2E flow control. The state variables are cleared to their default values when the Transmit Ring is enabled. Other implementations are possible as long as the requirements in Section 12.2 are met:

- *Credits Consumed*
 - Contains a count (modulo 8192) of the total number of flow control credits consumed by Tunneled Packets sent by the Transmitting Host Interface since the Ring was initialized.
 - Default value is 0.
 - In Raw Mode, incremented each time a Tunneled Packet is sent by the Transmitting Host Interface: $\text{Credits Consumed} = (\text{Credits Consumed} + 1) \bmod 8192$.
 - In Frame Mode, incremented each time a last Tunneled Packet is sent for a Frame by the Transmitting Host Interface: $\text{Credits Consumed} = (\text{Credits Consumed} + 1) \bmod 8192$.
 - Included in the *Credits* field of an E2E Credit Sync Packet each time an E2E Credit Sync Packet is sent.
- *Credit Limit*
 - Contains the most recent number of flow control credits received from the Receiving Host Interface at the other end.
 - Default value is 0.
 - Updated each time an E2E Credit Grant Packet is received for the Transmit Descriptor Ring by overwriting with the value contained in the *Credits* field of the E2E Credit Grant Packet.

12.2.2.4 Receiving Host Interface Rules

A Receiving Host Interface Adapter Layer shall track credits individually for each Receive Descriptor Ring enabled with E2E flow control.

A Receiving Host Interface Adapter Layer shall send an E2E Credit Grant Packet every $t_{E2ERate}$ for each Receive Descriptor Ring with E2E flow control enabled. It shall also send an E2E Credit Grant Packet each time additional Receive Descriptors are made available to the Receive Descriptor Ring in Host Memory. An E2E Credit Grant Packet shall carry the most recent credit count for the Descriptor Ring.

A Host Interface Adapter Layer shall not send E2E Credit Grant Packets for a Receive Descriptor Ring with E2E flow control disabled.

If the Adapter indicated by the *Transmit E2E HopID* field for a Receive Descriptor Ring is in a Low Power state, a Host Interface Adapter Layer shall only send an E2E Credit Grant Packet for the Receive Descriptor Ring when the credit count for the Receive Ring changes.

The number of available credits advertised for a Receive Descriptor Ring shall not exceed 8192.

When a Receiving Host Interface Adapter Layer receives a Credit Sync Packet, it shall verify the *ECC* field value in the Credit Sync Packet payload.

- The Adapter Layer shall correct any single-bit errors. After correcting an error, the Adapter Layer shall continue on as if the error had never occurred.
- If an uncorrectable error is detected, the Credit Sync Packet shall be dropped.

The following is a recommended scheme using state variables to manage credits for each Receive Descriptor Ring enabled with E2E flow control. The state variables are cleared to their default values when the Receive Ring is enabled. Other implementations are possible as long as the requirements in Section 12.2 are met:

- *Credits Allocated*
 - Contains the total number (modulo 8192) of flow control credits allocated to the Receive Descriptor Ring since initialization.
 - On initialization, set to the number of Receive Descriptors provided by the Host in the Receive Descriptor Ring.
 - Included in the *Credits* field of an E2E Credit Grant Record each time an E2E Credit Grant Packet is sent.
 - Incremented (modulo 8192) by the number of Receive Descriptors provided each time a Host provides additional Receive Descriptors.
 - Each time an E2E Credit Sync Packet is consumed by the Host Interface Adapter Layer, the *Credits Allocated* counter is be updated as follows:
$$\text{Credits Allocated} = (\text{Credits Allocated} + (\text{Credits Consumed} - \text{Credits Received})) \bmod 8192$$

where *Credits Consumed* is the value in the *Credits* field in the E2E Credit Sync Packet.
- *Credits Received*
 - Contains the total number (modulo 8192) of flow control credits used by the Receive Descriptor Ring since initialization.
 - Set to 0 on initialization.
 - Incremented (modulo 8192) each time the Host Interface Adapter Layer receives a Tunneled Packet (in Raw Mode) or the last Tunneled Packet of a Frame (in Frame Mode).
 - Each time an E2E Credit Sync Packet is consumed by the Host Interface Adapter Layer, the *Credits Received* variable is updated after the *Credits Allocated* variable has been updated:

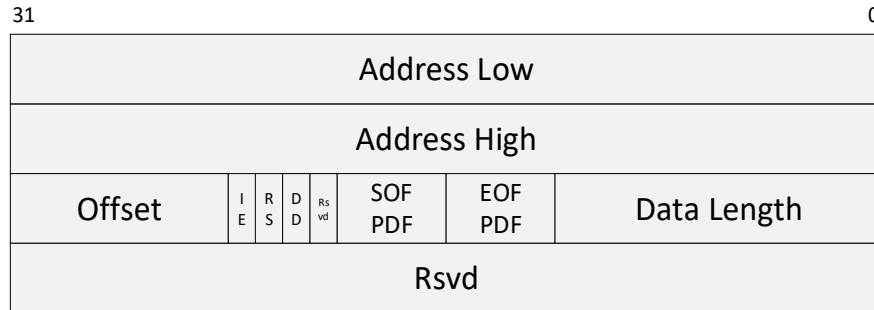
$\text{Credits Received} = \text{value in the Credits field in the E2E Credit Sync Packet}$

12.3 Transmit Interface

A Host Interface Adapter Layer shall implement a Transmit Descriptor Ring for each supported Path.

12.3.1 Transmit Descriptor Structure

The Host Interface Adapter Layer shall fetch Transmit Descriptors from Host Memory. A Transmit Descriptor shall have the format depicted in Figure 12-4 and listed in Table 12-6.

Figure 12-4. Transmit Descriptor Structure**Table 12-6. Transmit Descriptor Contents**

DW	Bits	Name	Function
0	31:0	<i>Address Low</i>	Address Low – Lower 32 bits of the physical address of a Data Buffer in Host Memory. The least significant 2-bits of the <i>Address Low</i> field shall be 00b. This field is written by the Host. An Adapter Layer shall not modify this field.
1	31:0	<i>Address High</i>	Address High – Upper 32 bits of the physical address of a Data Buffer in Host Memory. This field is written by the Host. An Adapter Layer shall not modify this field.
2	11:0	<i>Data Length</i>	Data Length – Number of bytes to be transmitted from this Data Buffer. A value of 0 indicates that 4096 bytes shall be fetched. This field is written by the Host. An Adapter Layer shall not modify this field.
	15:12	<i>EOF PDF</i>	EOF PDF Raw Mode: Contains the PDF value for the Transport Layer Packet carrying data from a Transmit Descriptor. Shall be set to a value between 0h and Eh. Frame Mode: Contains the PDF value for the last Tunneled Packet for a Transmit Descriptor. If the Transmit Descriptor is the last (or only) Transmit Descriptor for a Frame, shall be set to a value between 1h and Eh. Else, shall be set to 0h. This field is written by the Host. An Adapter Layer shall not modify this field.
2	19:16	<i>SOF PDF</i>	SOF PDF Raw Mode: A Router shall ignore this field. Frame Mode: Contains the PDF value for the first Tunneled Packet for a Transmit Descriptor that is segmented into more than one Tunneled Packet. If the Transmit Descriptor is the first (or only) Transmit Descriptor for a Frame, shall be set to a value between 1h and Eh. Else, shall be set to 0h. The SOF PDF shall be different than the EOF PDF for the Frame. This field is written by the Host. An Adapter Layer shall not modify this field.
	20	<i>Rsvd</i>	Reserved

DW	Bits	Name	Function
	21	<i>Descriptor Done</i>	Descriptor Done (DD) – This bit is set to 0b by the Host when posting a Data Buffer to be transmitted. If the <i>Request Status</i> bit is set to 1b, the Host Interface Adapter Layer shall set this bit to 1b after the last byte of the Data Buffer is sent to the Transport Layer. If the <i>Request Status</i> bit is set to 0b, the Host Interface Adapter Layer shall not write to this bit.
	22	<i>Request Status</i>	Request Status (RS) – This bit determines whether the Host Interface Adapter Layer updates transmission status in the <i>DD</i> bit. This field is written by the Host. An Adapter Layer shall not modify this field.
	23	<i>Interrupt Enable</i>	Interrupt Enable (IE) – If this bit is set to 1b, then the Host Interface Adapter Layer shall issue an interrupt indicating the completion of the Data Buffer after setting the <i>DD</i> bit to 1b. This field is written by the Host. An Adapter Layer shall not modify this field.
	31:24	<i>Offset</i>	Offset – The offset in bytes of the beginning of data to be transmitted. Offset is relative to the beginning of the Data Buffer as defined in the <i>Address Low</i> and <i>Address High</i> fields. This field is written by the Host. An Adapter Layer shall not modify this field.
3	31:0	<i>Rsvd</i>	Reserved



CONNECTION MANAGER NOTE

A Connection Manager shall not use PDF value Eh for SOF PDF or EOF PDF when the Host Interface Path is using a Lane Adapter which is also used for a Path that supports PM Packet (PMPS).

12.3.2 Transmit Flow

A Host Interface Adapter Layer shall only process a Transmit Descriptor Ring when both the Transmit Descriptor Ring is enabled and at least one Transmit Descriptor is pending. For a PCIe Host Interface Adapter Layer, Transmit Descriptors are pending when the *Producer Index* field for the Transmit Descriptor Ring has a different value than the *Consumer Index* field (see Section 12.6.3.2.3).

Section 12.3.2.1 describes how a Host Interface Adapter Layer processes Transmit Descriptor Ring in Frame Mode. Section 12.3.2.2 describes how a Host Interface Adapter Layer processes Transmit Descriptor Ring in Raw Mode.



CONNECTION MANAGER NOTE

A Connection Manager shall only post Control Packets to Transmit Ring 0. It shall not post Control Packets to any other Transmit Ring.

12.3.2.1 Frame Mode

A Frame shall reside in one or more Data Buffers. A Data Buffer shall not contain data from more than one Frame at a time. A Frame may span multiple Data Buffers.

A Host Interface Adapter Layer shall segment a Frame into one or more Tunneled Packets as follows:

- The Host Interface Adapter takes the Data Buffers of one or more Transmit Descriptors to form a Tunneled Packet payload. The Host Interface Adapter Layer prepends a Transport Layer Packet Header to the payload to generate a Tunneled Packet.
- If a Tunneled Packet contains multiple Data Buffers as payload, all Data Buffers shall contain data from the same Frame.
- If a Frame is sent in a single Tunneled Packet, the Tunneled Packet shall be of type *End of Frame*.
- If a Frame is sent in multiple Tunneled Packets:
 - The Tunneled Packet containing the first segment of the Frame shall be of type *Start of Frame* and shall be sent first.
 - Any following Tunneled Packets other than the last Tunneled Packet shall be of type *Middle of Frame*.
 - The Tunneled Packet containing the last segment of the Frame shall be of type *End of Frame* and shall be sent last.

The Router shall append a 32-bit CRC to each Frame. The CRC shall cover the entire Frame. The Router shall calculate the CRC as defined in Table 6-1. The CRC shall be calculated in increasing DW order. Within each DW, CRC shall be calculated from bit[31] to bit[0].

- The CRC shall be placed in the payload of an *End of Frame* Tunneled Packet immediately after the Frame bytes. See Appendix A.7 for an example of a Frame CRC.
 - Bits [7:0] of the calculated CRC shall be placed in bits [31:24] of the *CRC* field.
 - Bits [15:8] of the calculated CRC shall be placed in bits [23:16] of the *CRC* field.
 - Bits [23:16] of the calculated CRC shall be placed in bits [15:8] of the *CRC* field.
 - Bits [31:24] of the calculated CRC shall be placed in bits [7:0] of the *CRC* field.
- An *End of Frame* Tunneled Packet may contain just the 32-bit CRC without any preceding Frame bytes.
- If padding is added to any Tunneled Packets, it shall be added after the Frame CRC is calculated and the Frame and CRC are segmented into Tunneled Packet payload.

The Router shall set the *HopID* value of each Tunneled Packet to n, where n is the HopID associated with the Transmit Descriptor Ring.

If the *RS* bit in the Transmit Descriptor is set to 1b, a Host Interface Adapter Layer shall do the following after the last byte of the Data Buffer is sent to the Transport Layer:

- Set the *DD* bit to 1b in the Transmit Descriptor in Host Memory.
- If the *IE* bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer. See Section 12.5 for interrupt issuance and handling by a PCIe Host Interface Adapter Layer. Interrupt handling in non-PCIe-based systems is implementation specific.

After fetching a Data Buffer from Host Memory, a PCIe Host Interface Adapter Layer shall increment the *Consumer Index* for the Transmit Descriptor Ring by 1 (with wraparound to 0 when *Consumer Index* = *Ring Size*).

12.3.2.2 Raw Mode

A Host Interface Adapter Layer shall fetch the payload for a Transport Layer Packet from the Data Buffer referenced in the next available Transmit Descriptor.

The Host Interface Adapter Layer is responsible for prepending the Transport Layer Packet Header to the payload fetched from the Data Buffer.

The *PDF* field in the Transport Layer Packet shall match the *EOF PDF* field in the Transmit Descriptor.

If the *RS* bit in the Transmit Descriptor is set to 1b, a Host Interface Adapter Layer shall do the following after the last byte of the Data Buffer is sent to the Transport Layer:

- Set the *DD* bit to 1b in the Transmit Descriptor in Host Memory.

- If the *IE* bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer. See Section 12.5 for interrupt issuance and handling by a PCIe Host Interface Adapter Layer. Interrupt handling in non-PCIe-based systems is implementation specific.

After fetching a Data Buffer from Host Memory, a PCIe Host Interface Adapter Layer shall increment the *Consumer Index* for the Transmit Descriptor Ring by 1 (with wraparound to 0 when *Consumer Index* = *Ring Size*).

12.4 Receive Interface

A Host Interface Adapter Layer shall implement a Receive Descriptor Ring for each supported Path.

12.4.1 Receive Descriptor Structure

A Receive Descriptor that is fetched from Host Memory shall have the format depicted in Figure 12-5 and listed in Table 12-7. A Receive Descriptor that is posted to Host Memory shall have the format depicted in Figure 12-6 and listed in Table 12-8.

Figure 12-5. Receive Descriptor Structure (Posted by Host)

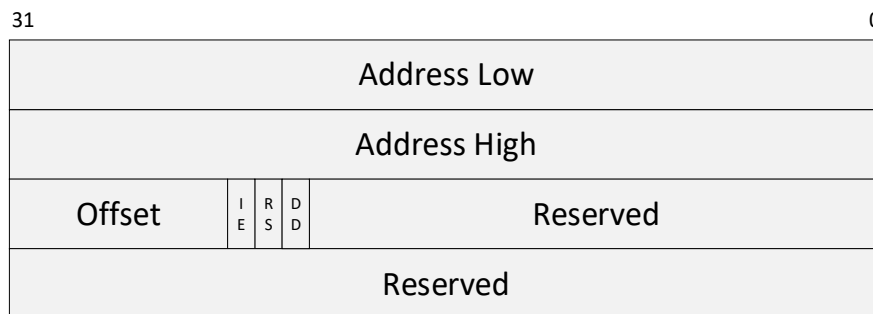
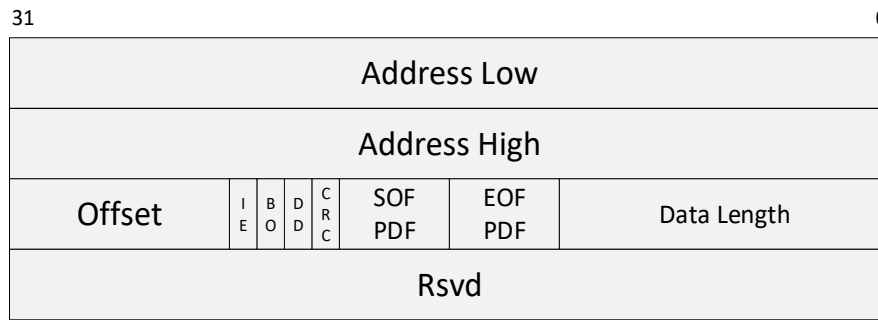


Table 12-7. Receive Descriptor Contents (Posted by Host)

DW	Bits	Name	Function
0	31:0	<i>Address Low</i>	Address Low – Lower 32 bits of the physical address of a Data Buffer in Host Memory. The least significant 2-bits of the <i>Address Low</i> field shall be 00b.
1	31:0	<i>Address High</i>	Address High – Upper 32 bits of the physical address of a Data Buffer in Host Memory.
2	20:0	<i>Reserved</i>	Reserved
	21	<i>Descriptor Done (DD)</i>	Descriptor Done – This bit shall be set to 0b.
	22	<i>Request Status (RS)</i>	Request Status – This bit is set to 1b to enable descriptor write-back by the Host Interface. Host shall always set this bit to 1b.
	23	<i>Interrupt Enable (IE)</i>	Interrupt Enable – This bit is set to 1b to enable interrupts indicating completion of the Data Buffer after the <i>DD</i> bit is set to 1b.
	31:24	<i>Offset</i>	Offset – The offset in bytes where the first byte of data shall be written to the Data Buffer. The offset is relative to the beginning of the Data Buffer as defined in the <i>Address Low</i> and <i>Address High</i> fields.
3	31:0	<i>Reserved</i>	Reserved

Figure 12-6. Receive Descriptor Structure (Posted by Host Interface Adapter Layer)**Table 12-8. Receive Descriptor Contents (Posted by Host Interface Adapter Layer)**

DW	Bits	Name	Function
0	31:0	<i>Address Low</i>	Address Low – Shall contain the same value as posted by the Host.
1	31:0	<i>Address High</i>	Address High – Shall contain the same value as posted by the Host.
2	11:0	<i>Data Length</i>	Data Length – Number of bytes posted to the Data Buffer. A value of 0 indicates that 4096 bytes were posted.
	15:12	<i>EOF PDF</i>	EOF PDF Raw Mode: Shall be set to the value in the <i>PDF</i> field of the Transport Layer Packet. Frame Mode: Shall be set to the value in the <i>PDF</i> field of the End of Frame Transport Layer Packet carrying the last (or only) segment of the Frame.
	19:16	<i>SOF PDF</i>	SOF PDF Raw Mode: Shall be set to 0h. Frame Mode: Shall be set to 0h if Frame is sent in a single Tunneled Packet. Else, shall be set to the value in the <i>PDF</i> field of the <i>Start of Frame</i> Transport Layer Packet carrying the first segment of the Frame.
	20	<i>CRC Error</i>	CRC Error – indicates if there is an error in the Frame CRC Raw Mode: This field shall be set to 0b. Frame Mode: This bit shall be set to 1b if the CRC check failed for the reassembled Frame. Otherwise, this bit shall be 0b.
	21	<i>Descriptor Done (DD)</i>	Descriptor Done If the <i>RS</i> bit is set to 1b when the Receive Descriptor is read from Host Memory, this bit shall be set to 1b after the last byte has been written to the Data Buffer.
	22	<i>Buffer Overflow (BO)</i>	Buffer Overflow Raw Mode: This bit shall be set to 1b if the size of the received Transport Layer Packet exceeds the available space in the Data Buffer. It shall be set to 0b otherwise. Frame Mode: This bit shall be set to 1b if the size of the reassembled Frame exceeds the available space in the Data Buffer. It shall be set to 0b otherwise.

2	23	<i>Interrupt Enable (IE)</i>	Interrupt Enable Shall contain the same value as posted by the Host.
	31:24	<i>Offset</i>	Offset Shall contain the same value as posted by the Host.
3	31:0	<i>Reserved</i>	Reserved

12.4.2 Receive Flow

This section defines how a Host Interface Adapter Layer processes a Transport Layer Packet received from the Transport Layer. When a Host Interface Adapter Layer receives a Transport Layer Packet from the Transport Layer it shall:

1. Select the Receive Descriptor Ring corresponding to the *HopID* field in the received Transport Layer Packet.
2. If the Receive Descriptor Ring is disabled, discard the Transport Layer Packet.
3. Else if the Receive Descriptor Ring operates in Frame Mode, process the Transport Layer Packet according to Section 12.4.2.1.
4. Else if the Receive Descriptor Ring operates in Raw Mode, process the Transport Layer Packet according to Section 12.4.2.2.

12.4.2.1 Frame Mode

A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows:

- All Tunneled Packets for a Frame shall be posted into the same Data Buffer.
- A Frame shall be posted using the next available Receive Descriptor. For a PCIe Host Interface Adapter Layer, a Receive Descriptor is available when the *Producer Index* field for the Receive Descriptor Ring has a different value than the *Consumer Index* field (see Section 12.6.3.3.3). The *Producer Index* field points to the next available Receive Descriptor.
 - If a Receive Descriptor is not available in Host Memory, discard the packet.
 - If a Receive Descriptor is not available for posting a *Start of Frame* packet, and potentially subsequent *Middle of Frame* packets, but is available for posting later packets for the same Frame, then subsequent Packets may be discarded.
- If the size of the packet payload exceeds the remaining available size of the Data Buffer:
 - Optionally write to the Data Buffer the part of the packet that fits into the Data Buffer. Any further received Tunneled Packets that belong to the same Frame shall be dropped and shall not be written to Host Memory.
 - Set the *Buffer Overflow* bit in the Receive Descriptor to 1b.
 - The *CRC Error* bit, the *SOF PDF* field, and the *EOF PDF* field shall represent the Frame as received, including packets not written to Host Memory.
- If a packet is a *Middle of Frame* packet and either no *Start of Frame* packet has been received for the Frame or the previous packet received for this Descriptor Ring was an *End of Frame* packet:
 - Post packet payload to a Data Buffer using the next available Receive Descriptor.
 - Set the *SOF PDF* field to 0b and the *CRC Error* bit to 1b in the Receive Descriptor after the Receive Descriptor is written back to Host Memory.
- If a packet is an *End of Frame* packet and either no *Start of Frame* packet has been received for the Frame or the previous packet received for this Descriptor Ring was an *End of Frame* packet:
 - Post packet payload to a Data Buffer using the next available Receive Descriptor.

- Set the *SOF PDF* field to 0b.
- However, if two *End of Frame* packets are received back-to-back, and the second received *End of Frame* packet contains only 32 bits of payload (representing 32 bits of appended CRC), it is recommended not to post a Receive Descriptor for the second *End of Frame* packet. If a Receive Descriptor is posted for the packet, then the *CRC Error* bit shall be set to 1b.
- If a packet is a *Start of Frame* packet and the previous packet received was a *Start of Frame* packet or a *Middle of Frame* packet, post the packet to the beginning of the Data Buffer (overwriting any previous packets).

Note: This applies even if the overwritten Frame overflowed the Data Buffer.

- Packet payload for a Frame shall be posted in the order received. If the Packet payload is from a *Start of Frame* packet, it shall be posted at the offset in the *Offset* field of the Receive Descriptor. Otherwise, payload shall be posted immediately after the previously received payload for the Frame.
 - The 32-bit CRC received with a Frame shall not be posted to the Data Buffer.
- If a packet is an *End of Frame* packet, and a Receive Descriptor is posted for the Frame:
 - If the *RS* bit in the Receive Descriptor is set to 1b, then:
 - Write back the Receive Descriptor with the contents defined in Table 12-8.
 - If the *IE* bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer.
 - For a PCIe Host Interface Adapter Layer, increment the *Producer Index* by 1 with wraparound to 0 when *Producer Index* = *Ring Size*.



CONNECTION MANAGER NOTE

When a Router writes a Receive Descriptor with the CRC Error bit set to 1b, software shall ignore the value written in the Data Length field of the receive descriptor.

12.4.2.2 Raw Mode

A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows:

- Each Transport Layer Packet payload shall be posted into a separate, single, Data Buffer. It shall be posted at the offset in the *Offset* field of the Receive Descriptor.
- A Transport Layer Packet shall be posted using the next available Receive Descriptor. For a PCIe Host Interface Adapter Layer, a Receive Descriptor is available when the *Producer Index* field for the Receive Descriptor Ring has a different value than the *Consumer Index* field (see Section 12.6.3.3.3). The *Producer Index* field points to the Receive Descriptor.
 - If a Receive Descriptor is not available in host memory, discard the packet.
- If the size of payload of the received Transport Layer Packet exceeds the available size of the Data Buffer:
 - Optionally, write the part of the packet that fits into the Data Buffer.
 - Set the *Buffer Overflow* bit in the Receive Descriptor to 1b.
 - If the *RS* bit in the Receive Descriptor is set to 1b, then:
 - Write back the Receive Descriptor with the contents defined in Table 12-8.

- If the *IE* bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer.
 - For a PCIe Host Interface Adapter Layer, increment the *Producer Index* by 1 with wraparound to 0 when *Producer Index* = *Ring Size*.
- When posting packet payload to a Data Buffer:
 - If the *RS* bit in the Receive Descriptor is set to 1b, then:
 - Write back the Receive Descriptor with the contents defined in Table 12-8.
 - If the *IE* bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer.
 - For a PCIe Host Interface Adapter Layer, increment the *Producer Index* by 1 with wraparound to 0 when *Producer Index* = *Ring Size*.

12.5 Interrupts

A PCIe Host Router shall support Message Signaled Interrupt (either MSI or MSI-X or both). Supporting PCI Compatible INTx interrupt emulation is optional.

12.5.1 Interrupt Causes

If the *Interrupt Enable* bit is set to 1b in a Transmit Descriptor, then after the Host Interface Adapter Layer writes back to that Transmit Descriptor, it shall set to 1b the *Transmit Data Buffer Interrupt* bit in the Interrupt Status Registers that corresponds to this Transmit Descriptor Ring.

If the *Interrupt Enable* bit is set to 1b in a Receive Descriptor, then after the Host Interface Adapter Layer has written back a Receive Descriptor, it shall set to 1b the *Receive Data Buffer Interrupt* bit in the Interrupt Status Registers that corresponds to this Receive Descriptor Ring.

The Host Interface Adapter Layer shall monitor how many unused Receive Descriptors are in each Receive Descriptor Ring. A Receive Descriptor is “unused” when the Host has indicated that the Receive Descriptor is available, but a Host Interface Adapter Layer has not yet posted a packet into its Data Buffer. For each Receive Descriptor Ring, a Host Interface Adapter Layer shall set to 1b the corresponding bit in the Receive Ring Vacancy Status register to 1b when either:

- The *Receive Ring Vacancy Control* field for that Receive Descriptor Ring is zero and Receive Descriptor Ring has no unused Receive Descriptors.
- The number of unused Receive Descriptors for a Receive Descriptor Ring is less than or equal to the value indicated by the *Receive Ring Vacancy Control* field for that Receive Descriptor Ring.

If a *Receive Ring Vacancy Status* bit is set to 1b, the Host Interface Adapter Layer shall set the corresponding bit to 1b in the Interrupt Status Registers.

12.5.2 Interrupt Masks

When the Host Interface Adapter Layer sets a bit in the *Interrupt Status* Registers to 1b, it shall initiate an interrupt request to the interrupt moderation function if the corresponding bit in the *Interrupt Mask* Registers is set to 1b. It shall not initiate an interrupt if the corresponding bit in the *Interrupt Mask* Registers is set to 0b.

12.5.3 Interrupt Vectors

In MSI mode of operation, the Host Interface Adapter Layer shall request a single interrupt vector. All interrupt causes are mapped to the single interrupt vector.

In MSI-X mode of operation, the Host Interface Adapter Layer shall support up to 16 interrupt vectors. When a bit is set to 1b in the *Interrupt Status* Registers and the corresponding bit in the *Interrupt Mask* Registers is set to 1b, the Host Interface Adapter Layer shall issue the interrupt vector associated with the interrupt cause in the *Interrupt Vector Allocation* Registers (IVAR).

12.5.4 Interrupt Moderation

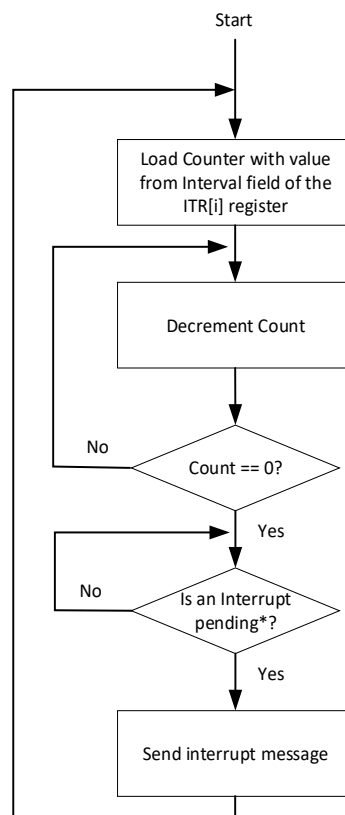
Interrupt moderation limits the rate of interrupts issued to the Host by delaying the time when an interrupt is issued to the Host. Each interrupt vector is moderated independently, where *Interrupt Throttling Rate Register i* (ITR[i]) moderates interrupt vector *i* ($i=0,\dots,15$). In INTx or MSI modes of operation, interrupt moderation only uses the ITR[0] register.

If the *Interval* field in the ITR[i] register ($i=0,\dots,15$) is set to 0, an interrupt of interrupt vector *i* shall not be moderated. An interrupt message shall be sent when the bit in the *Interrupt Status Registers* that is associated with interrupt vector *i* is set to 1b.

If the *Interval* field in the ITR[i] register ($i=0,\dots,15$) is set to a non-zero value, an interrupt message shall be sent according to the flow defined in Figure 12-7.

Section 12.6.3.4.7 defines the time interval for interrupt moderation.

Figure 12-7. Interrupt Moderation



* An interrupt is pending when a bit in the Interrupt Status Registers that is associated with interrupt vector *i* is set to 1b

12.6 Programming Interface

A PCIe Host Interface Adapter Layer shall support the programming interface defined in this section.

This section defines the Configuration Space of the Host Interface Adapter Layer. The Configuration Space resides in a single PCIe Memory BAR space.

The Host Interface Adapter Layer shall discard any write request to a non-implemented register within the memory BAR space.

The returned value by the Host Interface Adapter Layer to a read request for a non-implemented register within the memory BAR space, is implementation-specific.

The Host Interface Adapter Layer shall support aligned 32-bit accesses (with all Byte Enables set to 1b) to the Memory BAR space.

The Host Interface Adapter Layer shall expose a value of 0C 03 40h in the *Class Code* field of the PCI Configuration Space.



CONNECTION MANAGER NOTE

A Connection Manager shall limit the size of a read and write accesses from the PCIe Memory BAR space to a single DW.

12.6.1 Access Types

Table 12-9 defines the access types that are possible for a particular configuration field.

Table 12-9. Access Types

Access Type	Description
R/W	Read/Write. A field with this access type shall be capable of both read and write operations. The value read from this field shall reflect the last value written to it unless the field was reset in the interim.
R/W S	Read/Write Status. A field with this access type shall be capable of both read and write operations. The value read from this field may or may not reflect the last value written.
RO	Read Only. A write to a field with this access type shall have no effect. A read shall return a meaningful value.
R/Clr	Read Clear. A field with this access type shall be cleared to 0 after it is read. A write to a field with this attribute shall have no effect on its value.
W/Clr	Write Clear. A field with this access type shall be cleared to 0 after it is written to. A read shall return a meaningful value.
R/W SC	Read/Write Self Clearing. When set to 1b a field with this access type causes an action to be initiated. A field with this attribute shall read as 0b after the action is complete. The value returned prior to completion of the action is vendor defined.
WO	Write Only. A field with this access type shall be capable of write operations. Reading the field returns a vendor-defined value.
Rsvd	Reserved. Reserved for future implementation. A write to this field shall have no effect. A read shall return 0.
RsvdZ	Reserved and Zero. Reserved for future implementation. A Connection Manager shall only write 0 to this field. A read shall return 0.



CONNECTION MANAGER NOTE

The Connection Manager shall not write a register with a value that is marked as “Rsvd”.

12.6.2 Registers Summary

The Memory BAR space contains the 32-bit registers listed in Table 12-10.

Certain fields have one instance per Transmit or Receive Descriptor Ring. The offset of such fields is defined as function of n, where n equals the HopID of the Transmit or Receive Descriptor Ring. N is equal to the value in the *Total Paths* field and represents the number of Transmit or Receive Descriptor Rings.

Table 12-10. Summary of Memory BAR Registers

Offset	Register Name	Section
Host Interface Control		
39640h	Host Interface Capabilities	12.6.3.1.1
39898h	Host Router Reset	12.6.3.1.2
39858h	Host Interface Reset	12.6.3.1.3
39864h	Host Interface Control	12.6.3.1.4
39880h	Host Interface CL1 Enable	12.6.3.1.5
39884h	Host Interface CL2 Enable	12.6.3.1.6
Transmit Descriptor Rings		
00000h + n * 10h	Base Address Low	12.6.3.2.1
00004h + n * 10h	Base Address High	12.6.3.2.2
00008h + n * 10h	Producer & Consumer Indexes	12.6.3.2.3
0000Ch + n * 10h	Ring Size	12.6.3.2.4
19800h + n * 20h	Ring Control	12.6.3.2.5
Receive Descriptor Rings		
08000h + n * 10h	Base Address Low	12.6.3.3.1
08004h + n * 10h	Base Address High	12.6.3.3.2
08008h + n * 10h	Producer & Consumer Indexes	12.6.3.3.3
0800Ch + n * 10h	Ring & Buffer Size	12.6.3.3.4
29800h + n * 20h	Ring Control	12.6.3.3.5
29804h + n * 20h	PDF Bit Masks	12.6.3.3.6
Interrupts		
37800h : 37800h + (4 * ceiling(3N/32) – 1)	Interrupt Status (ISR)	12.6.3.4.1
37808h : 37808h + (4 * ceiling(3N/32) – 1)	Interrupt Status Clear (ISC)	12.6.3.4.2
37810h : 37810h + (4 * ceiling(3N/32) – 1)	Interrupt Status Set (ISS)	12.6.3.4.3
38200h : 38200h + (4 * ceiling(3N/32) – 1)	Interrupt Mask (IMR)	12.6.3.4.4
38208h : 38208h + (4 * ceiling(3N/32) – 1)	Interrupt Mask Clear (IMC)	12.6.3.4.5
38210h : 38210h + (4 * ceiling(3N/32) – 1)	Interrupt Mask Set (IMS)	12.6.3.4.6
38C00h : 38C3Ch	Interrupt Throttling Rate (ITR)	12.6.3.4.7
38C40h : 38C40h + (4 * ceiling(3N/8) – 1)	Interrupt Vector Allocation (IVAR)	12.6.3.4.8
18C00h : 18C00h + (4 * ceiling(N/8) – 1)	Receive Ring Vacancy Control	12.6.3.4.9
19400h : 19400h + (4 * ceiling(N/32) – 1)	Receive Ring Vacancy Status	12.6.3.4.10

12.6.3 Registers Description**12.6.3.1 Host Interface Control****12.6.3.1.1 Host Interface Capabilities**

The Host Interface Capabilities register specifies the parameters supported by the Host Interface Adapter Layer.

Table 12-11. Host Interface Capabilities Register

Bit(s)	Field Name and Description	Type	Default Value									
10:0	Total Paths The total number of transmit/receive Paths supported by the Host Interface Adapter Layer. This field shall not exceed a value of 21.	RO	Vendor defined									
15:11	Reserved	Rsvd	0									
23:16	Host Interface Version This field identifies the version of the USB4 specification supported by the Host Interface where: <table><tr><td></td><td>Major Version (Bits 23:21)</td><td>Minor Version (Bits 20:16)</td></tr><tr><td>USB4 Ver. 1.0 or TBT3</td><td>000b</td><td>00000b</td></tr><tr><td>USB4 Ver. 2.0</td><td>010b</td><td>00000b</td></tr></table> All other values are reserved. A Router shall set this field to 40h.		Major Version (Bits 23:21)	Minor Version (Bits 20:16)	USB4 Ver. 1.0 or TBT3	000b	00000b	USB4 Ver. 2.0	010b	00000b	RO	40h
	Major Version (Bits 23:21)	Minor Version (Bits 20:16)										
USB4 Ver. 1.0 or TBT3	000b	00000b										
USB4 Ver. 2.0	010b	00000b										
31:24	Reserved	Rsvd	0									

12.6.3.1.2 Host Router Reset

The Host Router Reset register is used to reset the Host Router.

Table 12-12. Host Router Reset Register

Bit(s)	Field Name and Description	Type	Default Value
0	Host Router Reset (HRR) When set to 1b, initiates a Host Router reset. Once the Host Router Reset is complete, the Host Router sets this bit to 0b. When this bit is 1b, it indicates that a Host Router Reset is in progress. When this bit is 0b, it indicates that a Host Router Reset is not in progress. The Connection Manager shall not read or write to this bit for 50 ms after setting it to 1b.	R/W SC	0b
31:1	Reserved	Rsvd	0

12.6.3.1.3 Host Interface Reset

The Host Interface Reset register resets the Host Interface Adapter Layer.

Table 12-13. Host Interface Reset Register

Bit(s)	Field Name and Description	Type	Default Value
0	RST When set to 1b, shall reset the Host Interface registers and the E2E flow control counters to their default values. The Host Interface Adapter Layer shall complete the reset within tHIReset time. It is recommended that a Ver. 2 Connection Manager does not issue a Host Interface Reset to a Ver. 2 Host Router. Instead, it may issue a Host Router Reset.	R/W SC	0b
31:1	Reserved	Rsvd	0

12.6.3.1.4 Host Interface Control**Table 12-14. Host Interface Control Register**

Bit(s)	Field Name and Description	Type	Default Value
16:0	Vendor Defined	Rsvd	Vendor Defined
17	Disable ISR Auto-Clear This bit controls the clearing of the Interrupt Status Registers. See Section 12.6.3.4.1.	R/W	0b
31:18	Vendor Defined	Rsvd	Vendor Defined

12.6.3.1.5 Host Interface CL1 Enable

The Host Interface CL1 Enable Register contains one bit per Transmit Descriptor Ring.

Table 12-15. Host Interface CL1 Enable

Bit(s)	Field Name and Description	Type	Default Value
31:0	Host Interface CL1 Enable bits When bit n (n=1,...,Total Paths – 1) is set to 0b, it prevents the Link associated with Transmit Descriptor Ring n from entering into CL1 state. When bit n is set to 1b it enables the Link associated with Transmit Descriptor Ring n to enter CL1 state. Bit[0] shall be reserved.	R/W	0

12.6.3.1.6 Host Interface CL2 Enable

The Host Interface CL2 Enable Register contains one bit per Transmit Descriptor Ring.

Table 12-16. Host Interface CL2 Enable

Bit(s)	Field Name and Description	Type	Default Value
31:0	Host Interface CL2 Enable bits When bit n (n=1,...,Total Paths – 1) is set to 0b, it prevents the Link associated with Transmit Descriptor Ring n from entering into CL2 state. When bit n is set to 1b it enables the Link associated with Transmit Descriptor Ring n to enter CL2 state. Bit[0] shall be reserved.	R/W	0

12.6.3.2 Transmit Descriptor Rings**12.6.3.2.1 Base Address Low****Table 12-17. Base Address Low Register**

Bit(s)	Field Name and Description	Type	Default Value
31:0	Base Address Low Lower 32 bits of the physical address of the corresponding Descriptor Ring in Host Memory. The Base Address is aligned to 16 bytes, so that the least significant 4-bits of the <i>Ring Base Address Low</i> field shall be 0h. Writing to this register sets the <i>Producer Index</i> field and the <i>Consumer Index</i> field to their default values.	R/W	0

12.6.3.2.2 Base Address High**Table 12-18. Base Address High Register**

Bit(s)	Field Name and Description	Type	Default Value
31:0	Base Address High Upper 32 bits of the physical address of the corresponding Descriptor Ring in Host Memory. Writing to this register sets the <i>Producer Index</i> field and the <i>Consumer Index</i> field to their default values.	R/W	0

12.6.3.2.3 Producer and Consumer Indexes**Table 12-19. Producer and Consumer Indexes Register**

Bit(s)	Field Name and Description	Type	Default Value
15:0	Consumer Index Index of the next Transmit Descriptor to be processed by the Host Interface Adapter Layer. The <i>Consumer Index</i> field counts in units of Descriptors. A value of 0 refers to the first Transmit Descriptor in the Descriptor Ring.	RO	0
31:16	Producer Index Index of the next Transmit Descriptor that Host writes to. The <i>Producer Index</i> field counts in units of Descriptors. A value of 0 refers to the first Transmit Descriptor in the Descriptor Ring. Router behavior is undefined if a Host writes a value larger than (<i>Ring Size</i> – 1). A Connection Manager shall not increment this field if the new value points to the location of the <i>Consumer Index</i> field (leaving one vacant space in the Ring).	R/W	0

12.6.3.2.4 Ring Size**Table 12-20. Ring Size Register**

Bit(s)	Field Name and Description	Type	Default Value
15:0	Ring Size The number of Transmit Descriptors in the Ring. Writing to this register sets the <i>Producer Index</i> field and the <i>Consumer Index</i> field to their default values. Ring Size shall not exceed 4096 descriptors.	R/W	0
31:16	Reserved	Rsvd	0

**CONNECTION MANAGER NOTE**

A Connection Manager shall write a non-zero value to the Ring Size field before setting the Ring Valid bit to 1b.

12.6.3.2.5 Ring Control**Table 12-21. Ring Control Register**

Bit(s)	Field Name and Description	Type	Default Value
27:0	Reserved	Rsvd	0
28	E2E Flow Control Enable When set to 0b, end-to-end flow control is disabled for this Transmit Descriptor Ring. When set to 1b, end-to-end flow control is enabled for this Transmit Descriptor Ring.	R/W	0b
29	No-snoop flag (NS) Determines the value to be set by the Host Interface Adapter Layer in the No Snoop attribute of a PCIe TLP associated with this Descriptor Ring.	R/W	0b
30	Raw Mode (RAW) When set to 0b, the Descriptor Ring shall operate in Frame Mode. When set to 1b, the Descriptor Ring shall operate in Raw Mode.	R/W	0b
31	Ring Valid When set to 0b, the Descriptor Ring is disabled. When set to 1b, the Descriptor Ring is enabled.	R/W	0b

**CONNECTION MANAGER NOTE**

When enabling a Transmit Descriptor Ring, the Connection Manager shall set all fields in this register to their proper values, including the Ring Valid bit, using a single DW write.

12.6.3.3 Receive Descriptor Rings**12.6.3.3.1 Base Address Low****Table 12-22. Base Address Low Register**

Bit(s)	Field Name and Description	Type	Default Value
31:0	Base Address Low Lower 32 bits of the physical address of the corresponding Descriptor Ring in Host Memory. The Base Address is aligned to 16 bytes, so that the least significant 4-bits of the <i>Ring Base Address Low</i> field shall be 0. Writing to this register sets the <i>Producer Index</i> field and the <i>Consumer Index</i> field to their default values.	R/W	0

12.6.3.3.2 Base Address High**Table 12-23. Base Address High Register**

Bit(s)	Field Name and Description	Type	Default Value
31:0	Base Address High Upper 32 bits of the physical address of the corresponding Descriptor Ring in Host Memory. Writing to this register sets the <i>Producer Index</i> field and the <i>Consumer Index</i> field to their default values.	R/W	0

12.6.3.3.3 Producer and Consumer Indexes**Table 12-24. Producer and Consumer Indexes Register**

Bit(s)	Field Name and Description	Type	Default Value
15:0	Consumer Index Index of the next Receive Descriptor that the Host provides to the Host Interface Adapter Layer. The <i>Consumer Index</i> field counts in units of Descriptors. A Host shall not write a value larger than (<i>Ring Size</i> – 1). A Connection Manager shall not increment this field if the new value points to the location of the <i>Producer Index</i> field (leaving one vacant space in the Ring).	R/W	0
31:16	Producer Index Index of the next Receive Descriptor that the Host Interface Adapter Layer writes to. The <i>Producer Index</i> field counts in units of Descriptors.	RO	0

**CONNECTION MANAGER NOTE**

A Connection Manager shall set the Consumer Index for a Ring to its default value after it sets the Ring Valid bit to 0b.

12.6.3.3.4 Ring and Buffer Size**Table 12-25. Ring Size Register**

Bit(s)	Field Name and Description	Type	Default Value
15:0	Ring Size Size of the Descriptor Ring in multiples of Receive Descriptors. Writing to this register sets the <i>Producer Index</i> field and the <i>Consumer Index</i> field to their default values. Ring Size shall not exceed 4096 descriptors.	R/W	0
27:16	Data Buffer Size A value of 0 indicates that 4096 bytes were posted. The Host Interface Adapter Layer shall not write to the <i>Data Length</i> field in a Receive Descriptor a value larger than <i>Data Buffer Size</i> minus the value of the <i>Offset</i> field provided by the Host in the Receive Descriptor.	R/W	0
31:28	Reserved	Rsvd	0

**CONNECTION MANAGER NOTE**

A Connection Manager shall write a non-zero value to the Ring Size field before setting the Ring Valid bit to 1b.

12.6.3.3.5 Ring Control**Table 12-26. Ring Control Register**

Bit(s)	Field Name and Description	Type	Default Value
11:0	Reserved	Rsvd	0
18:12	Transmit E2E HopID For a Receive Descriptor Ring sending an E2E Credit Grant Packet: This field specifies the value to be inserted into the HopID field of an E2E Credit Grant Packet for this Receive Descriptor Ring. See Table 12-2. For a Receive Descriptor Ring receiving an E2E Credit Grant Packet: This field specifies the Transmit Descriptor Ring that is the target of E2E Credit Grant Packets received by this Receive Descriptor Ring. See Section 12.2.1.1. This field is only valid if the <i>E2E Flow Control Enable</i> bit in this register is set to 1b. <i>Note: This field is only valid when the Ring Valid bit is 1b.</i>	R/W	0
27:19	Reserved	Rsvd	0
28	E2E Flow Control Enable When set to 0b, end-to-end flow control is disabled for this Receive Descriptor Ring. When set to 1b, end-to-end flow control is enabled for this Receive Descriptor Ring.	R/W	0b
29	No-snoop flag (NS) Determines the value to be set by the Host Interface Adapter Layer in the No Snoop attribute of a PCIe TLP associated with this Descriptor Ring.	R/W	0b
30	Raw Mode (RAW) When set to 0b, the Descriptor Ring shall operate in Frame Mode. When set to 1b, the Descriptor Ring shall operate in Raw Mode.	R/W	0b
31	Ring Valid When set to 0b, the Descriptor Ring is disabled. When set to 1b, the Descriptor Ring is enabled.	R/W	0b

**CONNECTION MANAGER NOTE**

When disabling a Receive Descriptor Ring, the Connection Manager shall set all fields in the register to their default values.

12.6.3.3.6 PDF Bit Masks**Table 12-27. PDF Bit Masks Register**

Bit(s)	Field Name and Description	Type	Default Value
15:0	EOF PDF Bitmask This field specifies the <i>PDF</i> values that shall be interpreted as <i>End of Frame PDF</i> . If the <i>Raw Mode</i> bit is set to 0b, then the Host Interface Adapter Layer shall treat a received Transport Layer Packet as an End of Frame packet if bit <i>i</i> (<i>i</i> =1,...,14) in this register is set to 1b, where <i>i</i> is the <i>PDF</i> value of the received Transport Layer Packet. If the <i>Raw Mode</i> bit is set to 1b, this field shall have no effect. A Host shall not set the same <i>PDF</i> value as both <i>EOF PDF</i> and <i>SOF PDF</i> . A Host shall always set bit 0 and bit 15 to 0b.	R/W	0

31:16	SOF PDF Bitmask This field specifies the <i>PDF</i> values that shall be interpreted as <i>Start of Frame PDF</i> . If the <i>Raw Mode</i> bit is set to 0b, then the Host Interface Adapter Layer shall treat a received Transport Layer Packet as a Start of Frame Packet if bit <i>i</i> ($i=17,\dots,30$) in this register is set to 1b, where ($i-16$) is the <i>PDF</i> value of the received Transport Layer Packet. If the <i>Raw Mode</i> bit is set to 1b, this field shall have no effect. A Host shall not set the same <i>PDF</i> value as both <i>SOF PDF</i> and <i>EOF PDF</i> . A Host shall always set bit 16 and bit 31 to 0b.	R/W	0
-------	---	-----	---

12.6.3.4 Interrupts

12.6.3.4.1 Interrupt Status

The Interrupt Status Registers illustrated in Figure 12-8, contain an *Interrupt Status* bit for each interrupt cause. The *Interrupt Status* bits are organized as a packed array of Doublewords. The last Doubleword may not necessarily be fully populated.

The first *N* bits are allocated to transmit Data Buffer interrupts, where each Transmit Descriptor Ring has its own interrupt. The second *N* bits are allocated to receive Data Buffer interrupts where each Receive Descriptor Ring has its own interrupt. The last *N* bits are allocated for Receive Descriptor Ring Vacancy interrupts, where each Receive Descriptor Ring has its own interrupt.

Figure 12-8. Structure of the Interrupt Status Registers

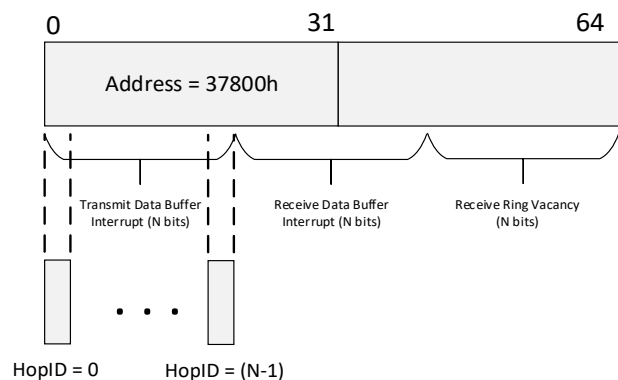


Table 12-28. Interrupt Status

Bit(s)	Field Name and Description	Type	Default Value
31:0	Interrupt Status bits Setting a bit in this register indicates that an interrupt is pending for the corresponding interrupt cause. If the <i>Disable ISR Auto-Clear</i> bit is set to 0b, then a read operation returns the current value and then clears the register to 0. If the <i>Disable ISR Auto-Clear</i> bit is set to 1b, then a read operation returns the current value and does not change the register contents. When a bit is set to 1b in the Interrupt Status Clear Registers, the corresponding bit in the Interrupt Status Registers shall be set to 0b. When a bit is set to 1b in the Interrupt Status Set Registers, the corresponding bit in the Interrupt Status Registers shall be set to 1b. A Host shall not write to this register.	See Description	0

12.6.3.4.2 Interrupt Status Clear

The Interrupt Status Clear Registers have the same structure as the Interrupt Status Registers. Each bit in the Interrupt Status Clear Registers corresponds to a bit at the same relative location in the Interrupt Status Registers.

Table 12-29. Interrupt Status Clear

Bit(s)	Field Name and Description	Type	Default Value
31:0	Interrupt Status Clear bits When a bit is set to 1b, the corresponding bit in the Interrupt Status Registers is set to 0b. Writing 0b to a bit in this register has no effect.	WO	Vendor Defined

12.6.3.4.3 Interrupt Status Set

The Interrupt Status Set Registers have the same structure as the Interrupt Status Registers. Each bit in the Interrupt Status Set Registers corresponds to a bit at the same relative location in the Interrupt Status Registers.

Table 12-30. Interrupt Status Set

Bit(s)	Field Name and Description	Type	Default Value
31:0	Interrupt Status Set bits When a bit is set to 1b, the corresponding bit in the Interrupt Status Registers is set to 1b. Writing 0b to a bit in this register has no effect.	WO	Vendor Defined

12.6.3.4.4 Interrupt Mask

The Interrupt Mask Registers have the same structure as the Interrupt Status Registers. Each bit in the Interrupt Mask Registers corresponds to a bit at the same relative location in the Interrupt Status Registers.

Table 12-31. Interrupt Mask

Bit(s)	Field Name and Description	Type	Default Value
31:0	Interrupt Mask bits When a bit is set to 0b, the corresponding interrupt cause is masked and does not generate an interrupt. When a bit is set to 1b, the corresponding interrupt cause generates an interrupt.	R/W	0

12.6.3.4.5 Interrupt Mask Clear

The Interrupt Mask Clear Registers have the same structure as the Interrupt Mask Registers. Each bit in the Interrupt Mask Clear Registers corresponds to a bit at the same relative location in the Interrupt Mask Registers.

Table 12-32. Interrupt Mask Clear

Bit(s)	Field Name and Description	Type	Default Value
31:0	Interrupt Mask Clear bits Writing 1b to a bit in this register sets the corresponding bit in the Interrupt Mask Registers to 0b. Writing 0b to a bit in this register does not have any effect.	WO	Vendor Defined

12.6.3.4.6 Interrupt Mask Set

The Interrupt Mask Set Registers have the same structure as the Interrupt Mask Registers. Each bit in the Interrupt Mask Set Registers corresponds to a bit at the same relative location in the Interrupt Mask Registers.

Table 12-33. Interrupt Mask Set

Bit(s)	Field Name and Description	Type	Default Value
31:0	Interrupt Mask Set bits Writing 1b to a bit in this register sets the corresponding bit in the Interrupt Mask Registers to 1b. Writing 0b to a bit in this register does not have any effect.	WO	Vendor Defined

12.6.3.4.7 Interrupt Throttling Rate (ITR)

Each of the ITR registers defines one MSI-X vector. ITR register n at offset $38C00h + 4 * n$ corresponds to MSI-X vector n ($n=0, \dots, 15$).

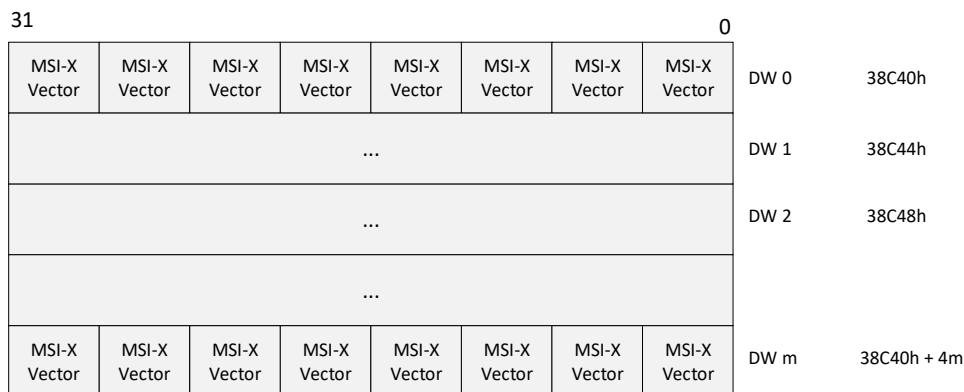
Table 12-34. Interrupt Throttling Rate (ITR)

Bit(s)	Field Name and Description	Type	Default Value
15:0	Interval Defines the initial value of the <i>Counter</i> field in increments of 256 ns. When set to 0, the interrupt throttling mechanism is disabled.	R/W	0
31:16	Counter A decrementing counter for interrupt throttling. When initialized following the issue of an interrupt, it starts counting with the value written to the <i>Interval</i> field and stops at zero. When written to, starts counting from the value written.	R/W	0

12.6.3.4.8 Interrupt Vector Allocation (IVAR)

The Interrupt Vector Allocation Registers, illustrated in Figure 12-9, contain a 4-bit MSI-X vector number for each interrupt cause. The MSI-X vector values are organized as a packed array of Doublewords. The last Doubleword may not necessarily be fully populated.

Each *MSI-X Vector* field correspond to one interrupt cause. The entry for interrupt cause n is located in DW $\lfloor n / 8 \rfloor$ starting at bit $4 * [n - 8 * \lfloor n / 8 \rfloor]$, where the interrupt causes are ordered as in the Interrupt Status Registers.

Figure 12-9. Structure of the Interrupt Vector Allocation Registers (IVAR)

$$m = \text{ceiling}(3N/8) - 1$$

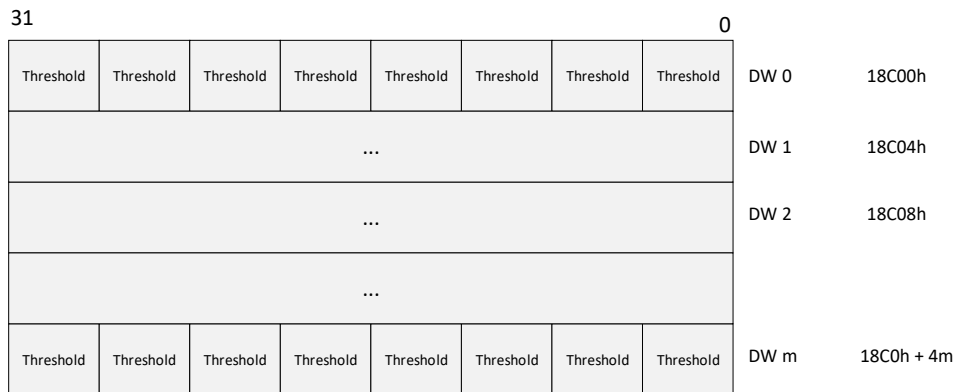
Table 12-35. Interrupt Vector Allocation (IVAR)

Bit(s)	Field Name and Description	Type	Default Value
3:0	Interrupt Vector Allocation (IVAR) Identifies the MSI-X vector issued when the corresponding interrupt cause is asserted.	R/W	0
...
31:28	Interrupt Vector Allocation (IVAR) Identifies the MSI-X vector issued when the corresponding interrupt cause is asserted.	R/W	0

12.6.3.4.9 Receive Ring Vacancy Control

The Receive Ring Vacancy Control Registers, illustrated in Figure 12-10, contain a 4-bit threshold value for each Receive Descriptor Ring. The values are organized as a packed array of Doublewords. The last Doubleword may not necessarily be fully populated.

Each *Threshold* field corresponds to one Receive Descriptor Ring. The entry for Receive Descriptor Ring n is located in DW $\lfloor n / 8 \rfloor$ starting at bit $4 * [n - 8 * \lfloor n / 8 \rfloor]$.

Figure 12-10. Structure of the Receive Ring Vacancy Control Register

$$m = \text{ceiling}(N/8) - 1$$

Table 12-36. Receive Ring Vacancy Control

Bit(s)	Field Name and Description	Type	Default Value
3:0	Threshold Identifies the vacancy threshold. An interrupt is issued when the corresponding Receive Descriptor Ring vacancy is less than or equal to the threshold (see Section 12.5.1). A value of 0 means the Receive Descriptor Ring does not have any available Receive Descriptors. A value of j ($j > 0$) corresponds to $2^{(j-1)}$ available Receive Descriptors.	R/W	0
...
31:28	Threshold Identifies the vacancy threshold. An interrupt is issued when the corresponding Receive Descriptor Ring vacancy is less than or equal to the threshold (see Section 12.5.1). A value of 0 means the Receive Descriptor Ring does not have any available Receive Descriptors. A value of j ($j > 0$) corresponds to $2^{(j-1)}$ available Receive Descriptors.	R/W	0

12.6.3.4.10 Receive Ring Vacancy Status

The Receive Ring Vacancy Status Registers contain a bit for each Receive Descriptor Ring. The *Receive Ring Vacancy Status* bits are organized as a packed array of Doublewords. The last Doubleword may not necessarily be fully populated.

Each *Receive Ring Vacancy Status* bit corresponds to one Receive Descriptor Ring. Bit n corresponds to Receive Descriptor Ring n .

Table 12-37. Receive Ring Vacancy Status

Bit(s)	Field Name and Description	Type	Default Value
31:0	Receive Ring Vacancy Status bits Setting a bit in this register indicates that the number of unused Receive Descriptors for a Receive Descriptor Ring is less than or equal to the threshold defined by the respective field in the Receive Ring Vacancy Control registers. See Section 12.5.1.	RO	0

12.7 Timing Parameters

Table 12-38 lists the timing parameters for the Host Interface Adapter Layer.

Table 12-38. Host Interface Timing Parameters

Parameter	Description	Min	Max	Units
tE2ERate	The time interval between periodic E2E Credit Grant Packets.	1	1000	ms
tE2ESync	The time interval between E2E Credit Sync Packets.	10	20	sec
tHIReset	Time to complete a Host Interface Reset.	-	10	ms

13 Interoperability with Thunderbolt™ 3 (TBT3) Systems

This chapter defines requirements for a USB4 Product to be TBT3-Compatible. A USB4 Product that is TBT3-Compatible can operate in a USB4® Fabric that includes any combination of the following:

- A Thunderbolt 3 Router.
- A Thunderbolt 3 Connection Manager.
- A Thunderbolt 3 Active Cable.

A USB4 Host and USB4 Peripheral Device may optionally support TBT3-Compatibility. If a USB4 Host or USB4 Peripheral Device supports TBT3-Compatibility, it shall do so as defined in this chapter.

A USB4 Hub shall support TBT3-Compatibility as defined in this chapter. A USB4 Hub shall support TBT3-Compatibility on all of its Downstream Facing Ports. A USB4 Hub may optionally support TBT3-Compatibility on its Upstream Facing Port.

13.1 Electrical Layer

When TBT3 Mode is established, an Adapter shall run at a TBT3-Compatible speed.

A Router Assembly shall support TBT3-Compatible Gen 2 Speed (10.3125Gbps). A Router Assembly may also optionally support TBT3-Compatible Gen 3 Speed (20.625Gbps).

A Router Assembly shall meet the specifications described in chapter 3, except for the following set of parameters that shall be used instead of the values specified in chapter 3:

Table 13-1. Thunderbolt 3 Parameters

Parameter Name	Min	Max	Units
USB4_SSC_DOWN_SPREAD_RATE_TX	See Table 3-2		KHz
USB4_SSC_PHASE_DEVIATION_TX	See Table 3-2		ns
TBT3_SSC_DOWN_SPREAD_RATE_TX	30	37	KHz
TBT3_SSC_PHASE_DEVIATION_TX	--	22	ns
SSC_DOWN_SPREAD_RATE_RX	30	37	KHz
SSC_PHASE_DEVIATION_RX	2.5	22	ns
UI (Gen 2 Speed)	96.9406	96.9988	ps
UI (Gen 3 Speed)	48.4703	48.4994	ps

The transmit average UI (measured over windows at the size of one SSC cycle) shall be at the range of 97.1348ps to 97.2420ps.

The receiver shall tolerate input signals with maximum SSC down spreading of 5800ppm.

Additional receiver “Case 2a” test setup shall be supported, addressing optical interconnects with limiting modules. Case 2a setup is identical to Case 2 setup described in Section 3.1.4.2 except that the passive cable is replaced with worst-case limiting optical cable (corresponding to the USB Type-C Specification). A receiver shall operate at BER of 1E-12 or lower with neither Forward Error Correction nor Pre-Coding applied when a stressed signal is driven at its input.

13.2 Logical Layer

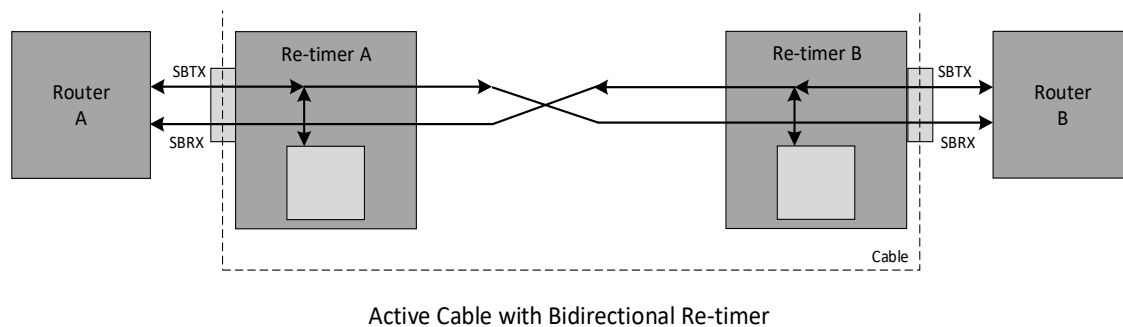
13.2.1 Sideband Channel

This section applies to a USB4 Port that is TBT3-Compatible.

13.2.1.1 Bidirectional Re-timer

A TBT3 Active Cable can contain two bidirectional Re-timers. A bidirectional Re-timer is a TBT3 Cable Re-timer that sends AT Responses on its SBRX wire. A Router shall implement a bidirectional Sideband Channel when attached directly to a bidirectional Cable Re-timer (i.e. when there are no On-Board Re-timers between the Router and the bidirectional Re-timer). A Router shall implement a unidirectional Sideband Channel when not attached directly to a bidirectional Cable Re-timer.

Figure 13-1 depicts SBTX and SBRX connectivity between two Routers that are connected via an Active Cable with bidirectional Re-timers. The Sideband Channel between Router A and Re-timer A in Figure 13-1 allows Router A to receive Transactions from Re-timer A on SBTX and receive Transactions from Router B on SBRX.

Figure 13-1. Bidirectional Re-timer Topology

A Router that is connected directly to a bidirectional Re-timer shall support concurrent reception of Transactions on SBTX and on SBRX.

A Router shall drive its SBTX for up to 2 bit times after the last Stop bit of an AT Command.

13.2.1.2 Transactions

This section applies to a TBT3-Compatible Sideband Channel unless specified otherwise. Section 13.2.1.2.3 applies when the Link is in TBT3 Mode.

13.2.1.2.1 LT Transactions

A Router shall support the additional LT Transaction types defined in Table 13-2.

Table 13-2. TBT3 LT Transaction Types

Bit(s)	Name	Function
[3:0]	<i>LSESymbol</i>	This field defines the LT Transaction Type. Undefined Values are Rsvd. 0001b: LT_Gen_2 (Gen 2 speed selected) 0101b: LT_Gen_3 (Gen 3 speed selected) 0110b: LT_Resume2 (Cable Re-timer started TBT3 transmission of recovered data with recovered clock in the direction of the cable)

13.2.1.2.2 AT Transactions

The structure of the STX Symbol within an AT Transaction shall be as defined in Table 13-3.

Table 13-3. STX Symbol

Bits	Name	Function
[7:6]	<i>StartAT</i>	See Table 4-7.
[5]	<i>Rsvd</i>	See Table 4-7.

Bits	Name	Function
[4]	<i>Responder</i>	Indicates that the Transaction originated from a responding Re-timer in an active cable with bidirectional Re-timers. Shall be set to 1b by a Re-timer in an AT Response when operating in an active cable with bidirectional Re-timers. Shall be set to 0b in all other cases.
[3]	<i>Bounce</i>	Together with the <i>ReturnBounce</i> bit, serves to forward an AT Transaction from a Router to a Cable Re-timer at the remote end of a cable that can only be accessed by its Link Partner. See Section 13.2.1.2.2.1 for more details.
[2]	<i>Recipient</i>	Identifies the intended final recipient of the Transaction. For an AT Command: shall be 0b if a Cable Re-timer is the intended final recipient or 1b if a Router is the intended final recipient. For an AT Response: shall be set to 1b.
[1]	<i>ReturnBounce</i>	Together with the <i>Bounce</i> bit, serves to forward an AT Transaction from a Router to a Cable Re-timer at the remote end of a cable that can only be accessed by its Link Partner. See Section 13.2.1.2.2.1 for more details.
[0]	<i>CmdNotResp</i>	See Table 4-7.

A Router shall not send an AT Command that targets Register 13 of a Re-timer or Router SB Register Space (see Table 4-20) unless the Re-timer or Router is directly attached to it.

13.2.1.2.2.1 Bounce Mechanism

The Bounce mechanism is used when a Router needs to access the Register Space of a Cable Re-timer that can only be accessed by its Link Partner. A Router shall support the Bounce Mechanism. The Bounce Mechanism consists of the following rules:

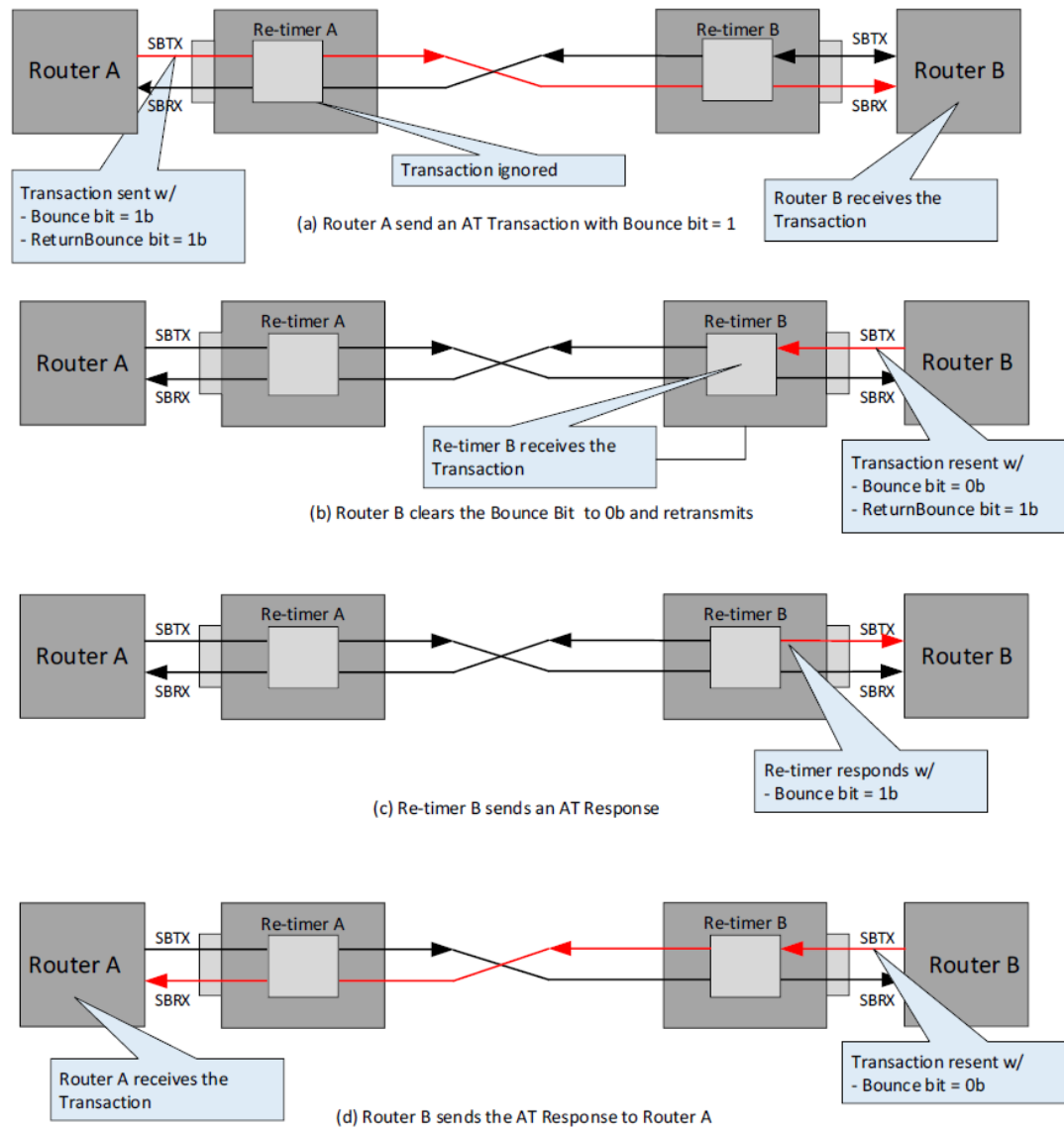
- A Router shall set the *Bounce* bit to 1b and the *ReturnBounce* bit to 1b to target a Cable Re-timer that is adjacent to the Router's Link Partner.
- A Router that receives an AT ~~TransactionCommand~~ with the *Bounce* bit set to 1b ~~and the ReturnBounce bit to 1b~~ shall set the *Bounce* bit to 0b, then forward the AT Transaction towards its adjacent Cable Re-timer.

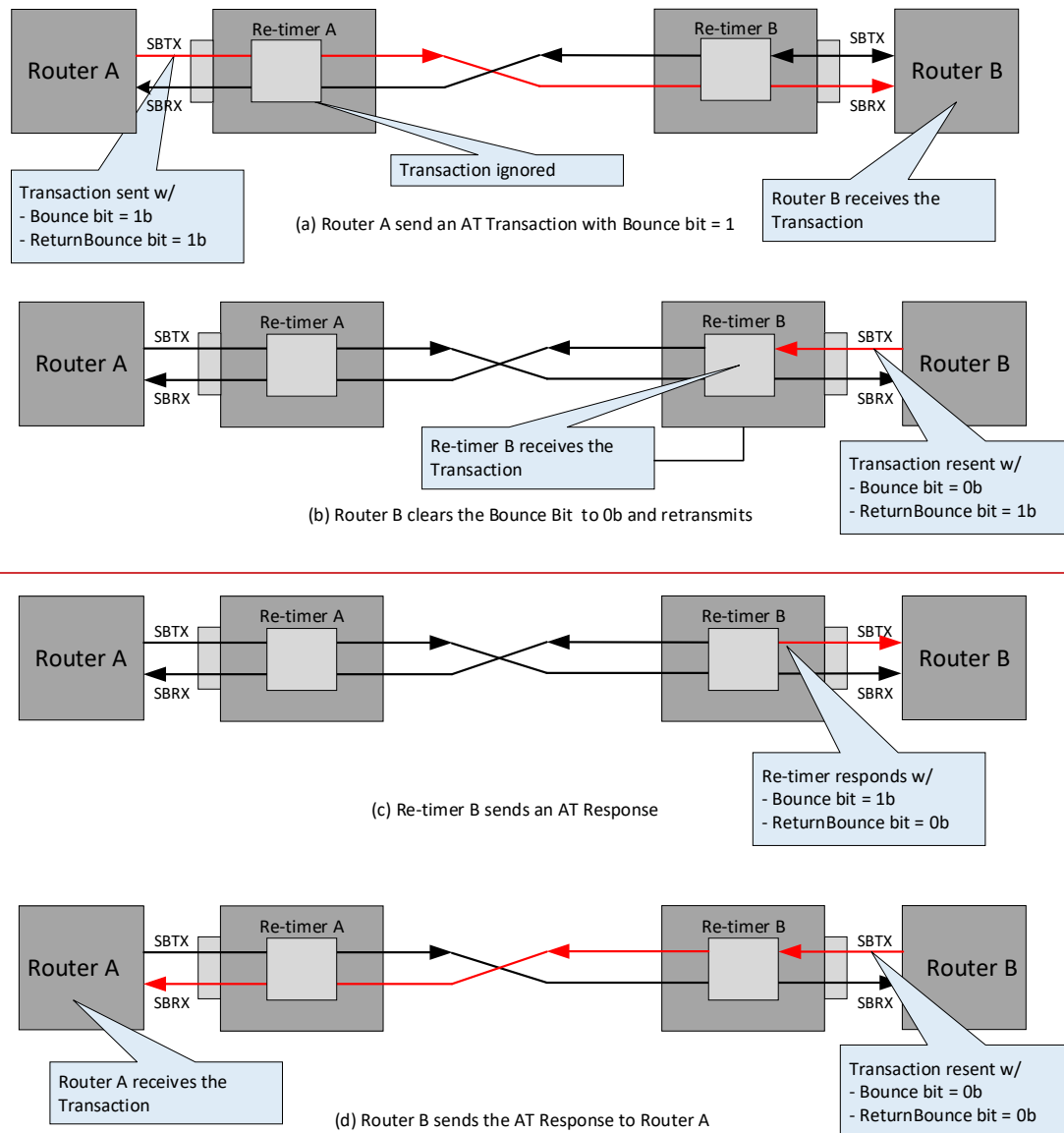
Note: A Cable Re-timer responds to an AT ~~TransactionCommand that has with~~ the *Bounce* bit set to 0b ~~and the ReturnBounce bit to 1b~~. The AT Response from the Cable Re-timer has the *Bounce* Bit set to the value of the ReturnBounce in the Command it received ~~1b and the ReturnBounce bit set to 0b~~.

- A Router that receives an AT Response with the *Bounce* bit set to 1b ~~and the ReturnBounce bit to 0b~~ shall set the *Bounce* bit to 0b, then forward the AT Response to its Link Partner.

An example of the Bounce Mechanism is shown in Figure 13-2 where Router A is accessing the Configuration Space of Cable Re-timer B.

Note: The Bounce Mechanism is only used when operating with a bi-directional Re-timer.

Figure 13-2. Bounce Mechanism



13.2.1.2.3 RT Transactions

Byte 2 in a Broadcast RT Transaction shall have the format in Table 4-10 with the changes in Table 13-4.

Table 13-4. Contents of Byte 2 in a Broadcast RT Transaction

Bits	Name	Function
0	<i>USB4</i>	When sending a Broadcast RT Transaction on a USB4 Sideband Channel, the <i>USB4</i> bit shall be set to 1b. When sending a Broadcast RT Transaction on a TBT3-Compatible Sideband Channel, the <i>USB4</i> bit shall be set to 0b. The <i>USB4</i> bit shall match the <i>TBT3-Compatible Sideband Channel</i> attribute defined in Table 13-7.
4	<i>TBT3-CompatibleSpeed</i>	Set to 1b.

13.2.1.3 SB Register Space

A TBT3 Router may respond to a read from Register 12 with either 2 or 3 bytes. In the case of a 2-byte response, a Router shall infer that the *USB4 Sideband Channel Support* bit is 0b and the *TBT3-Compatible Speeds Support* bit is 1b.

A Router shall support the additional registers and register fields in Table 13-5 and Table 13-6.

Table 13-5. SB Registers

Register	Size (Bytes)	Name	Description
3	4	Mode	A FourCC string indicating the operating mode of the Router.
4	4	Type	A FourCC string indicating the type of USB4 Device.
10	1	Rsvd	Reserved.

Table 13-6. SB Registers Fields

Register	Name	Byte	Bits	Description	Type
3	Mode	0	7:0	Contains the ASCII value "A" = 41h	RO
3	Mode	1	7:0	Contains the ASCII value "P" = 50h	RO
3	Mode	2	7:0	Contains the ASCII value "P" = 50h	RO
3	Mode	3	7:0	Contains the ASCII value "Space" = 20h	RO
4	Type	0	7:0	Contains the ASCII value "E" = 45h	RO
4	Type	1	7:0	Contains the ASCII value "M" = 4Dh	RO
4	Type	2	7:0	Contains the ASCII value "Space" = 20h	RO
4	Type	3	7:0	Contains the ASCII value "Space" = 20h	RO
10	Rsvd	0	7:0	Contains the value 00h	RO

13.2.1.4 Lane Initialization**13.2.1.4.1 Phase 1 – Determination of Initial Conditions**

During Phase 1, Router A determines whether TBT3 Mode is established on the Link and whether the Cable connected supports CLx states. See the USB PD Specification and the USB Type-C Specification for how to determine if TBT3 Mode is established and if the Cable supports CLx states.

A Router shall not continue on to Phase 2 until it has obtained the connection information described in this section and in Section 4.1.2.1. If TBT3 Mode is established on the Link, a Router shall proceed with Lane Initialization as defined in Section 4.1.2 with the changes defined in this chapter.

13.2.1.4.2 Phase 3 – Determination of USB4 Port Characteristics

A Router shall decide the Lane attributes using the decision criteria in Table 4-30 with the changes defined in Table 13-7.

Table 13-7. Lane Attributes

Attribute	Action
RS-FEC	<p>Gen 2 speed:</p> <p>Router A shall enable RS-FEC if at least one side of the Link requests it (i.e. the <i>RS-FEC Request (Gen 2)</i> bit is set to 1b in the SB Register Space of the local USB4 Port and/or its Link Partner). Otherwise, RS-FEC shall not be enabled.</p> <p>Router A shall set the <i>RS-FEC Enabled (Gen 2)</i> bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.</p>
TBT3-Compatible Sideband Channel	<p>The Sideband Channel of Router A shall operate as a TBT3-Compatible Sideband Channel (as defined in Section 13.2.1) if any of the following are true:</p> <ul style="list-style-type: none"> The <i>USB4 Sideband Channel Support</i> bit in the SB Register Space of one of the Routers is 0b. The Link is over an Active Cable with bidirectional Re-timers. <p>Else, the Sideband Channel of Router A shall operate as a USB4 Sideband Channel (as defined in Section 4.1).</p>

13.2.1.4.3 Phase 4 – Lane Parameters Synchronization and Transmit Start

For a TBT3-Compatible Sideband Channel, this section replaces Step 2 in Section 4.1.2.4.

- Router A shall do the following for each enabled Lane to indicate that it is ready to start transmission on a given Lane:
 - If the Router Assembly for Router A does not include any On-Board Re-timers, and if operating at Gen 2 speed, Router A shall send an LT_Gen_2 Transaction for each enabled Lane every tLaneParams. Router A shall continue sending LT_Gen_2 Transactions until all the following are true, then continue to Step 2:
 - At least tLTPhase4 time has passed from completion of Phase 2.
 - Router A has sent LT_Gen_2 Transactions at least twice.
 - Router A has received an LT_Gen_2 Transaction from Router B.
 - If the Router Assembly for Router A does not include any On-Board Re-timers, and if operating at Gen 3 speed, Router A shall send an LT_Gen_3 Transaction for each enabled Lane every tLaneParams. Router A shall continue sending LT_Gen_3 Transactions until all the following are true, then continue to Step 2:
 - At least tLTPhase4 time has passed from completion of Phase 2.
 - Router A has sent LT_Gen_3 Transactions at least twice.
 - Router A has received an LT_Gen_3 Transaction from Router B.
 - If the Router Assembly for Router A includes one or more On-Board Re-timers, and if operating at Gen 2 speed, Router A shall send a Broadcast RT Transaction every tLaneParams. The Broadcast RT Transaction shall have the parameter values in Table 4-30. Router A shall also send an LT_Gen_2 Transaction for each enabled Lane.
 - Router A shall continue sending the Broadcast RT and LT_Gen_2 Transactions until all the following conditions are true:
 - At least tLTPhase4 time has passed from completion of Phase 2.
 - Router A has sent LT_Gen_2 Transactions at least twice.
 - Router A has received an LT_Gen_2 Transaction from Router B.
 - If the Router Assembly for Router A includes one or more On-Board Re-timers, and if operating at Gen 3 speed, Router A shall send a Broadcast RT Transaction every tLaneParams. The Broadcast RT Transaction shall have the parameter values in Table 4-30. Router A shall also send an LT_Gen_3 Transaction for each enabled Lane.

- Router A shall continue sending the Transactions until all the following conditions are true:
 - At least tLTPhase4 time has passed from completion of Phase 2.
 - Router A has sent LT_Gen_3 Transactions at least twice.
 - Router A has received an LT_Gen_3 Transaction from Router B.

13.2.1.4.4 Phase 5 – Link Equalization

For a TBT3-Compatible Sideband Channel, this section replaces Section 4.1.2.5.

The fifth phase of Lane Initialization consists of negotiating transmitter Feed-Forward Equalization (TxFFE) parameters between each Router or Re-timer and a Router or Re-timer adjacent to it. During TxFFE negotiation, the receiver cycles through one or more of the potential Preset numbers defined in Table 3-4. The receiver examines its behavior for each Preset and selects one Preset value to use. The receiver may follow any order while cycling through the Preset numbers.

The TxFFE flow that Router A's transmitter performs depends on whether Router A is connected to an On-Board Re-timer, a Cable Re-timer, or another Router:

- If Router A connects to an On-Board Re-timer in the same Router Assembly, then Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1. The Router and Re-timer use Addressed RT Transactions (with the *Index* field set to 0) to access each other's SB Register Space.
- If Router A connects to a Cable Re-timer:
 - Router A's transmitter shall perform the Primary Partner flow in the Asymmetric TxFFE Parameter Negotiation with a transmitting Primary Partner defined in Section 13.2.1.4.4.1. The Router uses AT Transactions (with the *Recipient* bit set to 0b) to access the Re-timer's SB Register Space.
 - Once a transmitter completes TxFFE negotiation with the Cable Re-timer's receiver, Router A shall send an LT_Resume2 Transaction on the USB4 Port that completed negotiation with the *LSELane* field matching the Lane number that completed negotiation.
- If Router A either connects directly to Router B or connects to an On-Board Re-timer in the Router Assembly of Router B (through a Passive Cable or Cable with re-driver), then Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1. Router A uses AT Transactions (with the *Recipient* bit set to 1b) to access the TxFFE Register of the adjacent USB4 Port.

The TxFFE flow that Router B's receiver performs depends on whether Router B is connected to an On-Board Re-timer, a Cable Re-timer, or another Router. Router B polls the *Tx Active* bit in the SB Register Space of the adjacent Router or Re-timer to identify when the transmitter of the adjacent Router or Re-timer is on.

- If Router B connects to an On-Board Re-timer, then Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1. The Router and Re-timer use Addressed RT Transactions (with the *Index* bit set to 0b) to access each other's SB Register Space.
 - When a receiver's equalization flow is complete on a Lane, the Router shall set the Lane's *Clock Switch Done* bit to 1b.
- If Router B connects to a Cable Re-timer, then Router B's receiver shall perform the Primary Partner flow in the Asymmetric TxFFE Parameter Negotiation with a Receiving Primary Partner defined in Section 13.2.1.4.4.2. The Router uses AT Transactions (with the *Recipient* bit set to 0b) to access the Re-timer's SB Register Space.

- If Router B either connects directly to Router A or connects to an On-Board Re-timer in the Router Assembly of Router A, then Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1. Router B uses AT Transactions (with the *Recipient* bit set to 1b) to access the SB Register Space of the adjacent USB4 Port.

The equalization flow for Re-timers is defined in the USB4 Re-Timer Specification.

13.2.1.4.4.1 Asymmetric TxFFE Parameter Negotiation with a Transmitting Primary Partner

During TxFFE negotiation, the transmitter negotiates TxFFE parameters with the receiver at the other end. The transmitting end is defined as the Primary Partner and it is capable of issuing AT Commands. The receiving end is defined as the Subordinate Partner and it is capable of issuing AT Responses.

Transmitting Primary Partner flow:

The steps that the transmitter shall perform are listed below:

1. The transmitter shall start with the *TX Active* bit set to 1b (default value) in the *Tx Status* byte of the TxFFE register.
2. The transmitter shall send an AT Transaction with a write Command to the receiver that sets the *Tx Active* bit to 1b in the *Partner Tx Status* byte in the TxFFE register.
3. The transmitter shall read the local *Rx Status & TxFFE Request* byte from the receiver. To do this, the transmitter sends an AT Transaction with a read Command targeting the TxFFE register of the receiver.
4. On reception of an AT Response from the receiver, the transmitter shall take the following actions:
 - If *Rx Locked* = 1b, then negotiation is complete and no further TxFFE negotiation steps shall be taken.
 - Else if *New Request* = 0b and *TxFFE Request* is the same as the previous *TxFFE Request*, the receiver has not provided a new request yet. The Router shall go to Step 3. The Router shall perform Step 3 within tPollTXFFE of receiving the AT Response.
 - Else, this is a new request to update TxFFE parameters. Continue on to Step 5.
5. The transmitter shall update its transmitter parameters based on the new parameters received in the AT Response. To do this, the transmitter loads one of 16 predefined TxFFE configurations that matches the *TxFFE Request* field in the *Rx Status & TxFFE Request* byte.
 - If both Lane Adapters in the USB4 Port are enabled and have not yet completed TxFFE negotiation, both transmitters shall complete Step 5 before continuing to Step 6. A Lane Adapter shall not continue to Step 6 until one of the following occurs:
 - The other Lane Adapter completes Step 5.
 - tTxFFETimeout has passed since starting Step 5.
6. The transmitter shall inform the receiver that it has updated to new parameters by sending an AT Transaction with a write Command to the receiver targeting its *Partner Tx Status* byte in the TxFFE register with the following contents:
 - *Tx Active* = 1b.
 - *TxFFE Setting* = value received in Step 4.
7. The transmitter shall read the local *Rx Status & TxFFE Request* byte from the receiver. To do this, the transmitter sends an AT Transaction with a read Command targeting the TxFFE register of the receiver.

8. On reception of an AT Response from the receiver, the transmitter shall take the following actions:
 - If *New Request* = 1b and *TxFxE Request* is the same as the previous *TxFxE Request*, the Router shall return to and perform Step 7 within tPollTXFFE of receiving the AT Response.
 - Else, go to Step 3.

Note: The Partner Tx Status byte is defined in the USB4 Re-Timer Specification.

13.2.1.4.4.2 Asymmetric TxFxE Parameter Negotiation with a Receiving Primary Partner

During TxFxE negotiation, the receiver negotiates TxFxE parameters with the transmitter at the other end. The receiving end is defined as the Primary Partner and can issue AT Commands. The transmitting end is defined as the Subordinate Partner and can issue AT Responses.

Receiving Primary Partner flow:

The receiver shall execute the following flow with the transmitter:

1. The receiver shall start with the following default values in the *Rx Status & TxFxE Request* byte of the TxFxE register:
 - *Rx Locked* = 0b.
 - *New Request* bit = 0b.
 - *Rx Active* bit = 0b.
2. The receiver shall read the *Local Tx Status* byte of the transmitter.
 - The receiver sends an AT Command with a read Command to the *Local Tx Status* byte of the TxFxE register of the transmitter.
 - On reception of an AT Response from the transmitter, the receiver shall do the following:
 - If *Tx Active* = 1b (i.e. the transmitter is transmitting), then enable the receiver, set *Rx Active* to 1b, and go to Step 3.
 - Else, repeat Step 2 within tPollTXFFE of receiving the AT Response.
3. The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the *Rx Locked* field to 1b.
4. The receiver shall do the following:
 - If *Rx Locked* = 1, then go to Step 5.
 - Else, go to Step 6.
5. TxFxE negotiation is complete.
6. The receiver shall select a new set of TxFxE parameters.
7. The receiver shall write the *Partner Rx Status & TxFxE Request* byte at the transmitter as follows:
 - If the Transmitting Primary Partner finished TxFxE on both Lanes, then the receiver sends an AT Command with a write Command targeting the *Partner Rx Status & TxFxE Request* byte of the TxFxE register of the transmitter. Else, the receiver will wait for the next AT Command with a write Command to the TxFxE Register from the Transmitting Primary Partner and use it to write the *Partner Rx Status & TxFxE Request* byte of the TxFxE register of the transmitter. The AT command shall write to following values to the following fields:
 - *New Request* = 1b.
 - *Rx Active* = 1b.
 - *TxFxE Request* = index of selected set of TxFxE parameters.

8. The receiver shall wait for a write Response indicating the transmitter is using the new requested TxFFE settings.
9. The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the *Rx Locked* field to 1b.
10. The receiver shall write the *Partner Rx Status & TxFFE Request* byte at the transmitter as follows:
 - If the Transmitting Primary Partner finished TxFFE on both Lanes, then the receiver sends an AT Command with a write Command targeting the *Partner Rx Status & TxFFE Request* byte of the TxFFE register of the transmitter.
 - Else, the receiver will wait for the next AT Command with a write Command to the TxFFE Register from the Transmitting Primary Partner and use it to write the *Partner Rx Status & TxFFE Request* byte of the TxFFE register of the transmitter. The AT Command shall write to following values to the following fields:
 - *New Request* = 0b.
 - *Rx Active* = 1b.
11. The receiver shall do the following:
 - If *Rx Locked* = 1, then go to Step 5.
 - Else, go to Step 6.

Note: The Transmitting Primary Partner and the Receiving Primary Partner are both on the same Router.

Note: The Partner Rx Status & TxFFE Request byte is defined in the USB4 Re-Timer Specification.

13.2.2 Logical Layer State Machine

13.2.2.1 TS1 and TS2 Ordered Sets

When operating in TBT3 mode, TS1 and TS2 Ordered Sets shall have the format shown in Table 4-25 with the changes in Table 13-8.

Table 13-8. TS1 and TS2 Ordered Set Structure

Bits	Name	Description
28:26	<i>Lane Bonding Target 2</i>	Lane Bonding Target 2. Transmitter shall either set this value to match the <i>Lane Bonding Target</i> field or shall set this value to 001b. A Receiver shall ignore this field.

13.2.2.2 Low Power States (CL0s, CL1, and CL2)

If the *CLx Protocol Support* bit in the USB4 Port Capability is set to 1b, the USB4 Port shall support the Low Power protocol as defined in Section 4.2.1.6. Else, the USB4 Port does not support the Low Power protocol and shall not initiate Low Power Transactions.

13.2.3 USB4 Link Operation

13.2.3.1 USB4 Link Transitions

When TBT3 Mode is established on the Link, a USB4 Port shall support the transitions described in Section 4.2.1.6.5.4 with the following changes:

- For a Device Router that supports TBT3 Mode on its Upstream Facing Port, all USB4 Ports shall support operation with two Single-Lane Links. Unlike Section 4.2.2, this configuration is not just a transient state between Link Initialization and Lane Bonding. When operating with two Single Lane Links, a USB4 Port is only required to support traffic on Lane 0.



CONNECTION MANAGER NOTE

A Connection Manager shall not set the Lane Bonding bit to 1b if a Path other than Path 0 is enabled across the Lanes being bonded.

13.2.3.2 Pre-Coding

In addition to the conditions defined in Section 4.3.1.6.2, Pre-Coding shall be off when the Link uses a TBT3-Compatible Sideband Channel.

13.2.4 Sleep and Wake

This section only applies to a Device Router that supports TBT3-Compatibility on its Upstream Facing Port.

If bits 15:12 in the Connection Manager *USB4 Version* field in Router Configuration Space are 0b (indicating a TBT3 Connection Manager), a Router shall support sleep and wake per Section 4.5 with the changes defined in this section.

13.2.4.1 Entry to Sleep

After the Enter Sleep bit is set to 1b in all Ports, a Device Router operating with a TBT3 Connection Manager shall follow the steps mentioned in Section 4.5.1 with the following differences:

- The *Lane 0 is Inter-Domain* bit shall be checked instead of the *USB4 Port is Inter-Domain* bit.
- The *Lane 0 Configured* bit shall be checked instead of the *USB4 Port is Configured* bit.
- The *Inter-Domain Disconnect on Sleep* bit = 1b shall be checked instead of the *Enable Wake on Inter-Domain* bit = 0b.

13.2.4.2 Behavior in Sleep State

A Device Router shall retain a copy of the state information listed in Table 13-9 separate from Configuration Space.

Table 13-9. Router State Retained During Sleep

Field Copied	Configuration Space / Capability
Upstream Adapter	Router Configuration Space.
Lane 0 is Inter-Domain	USB4 Port Region in Vendor Specific Extended 6 Capability of the Router Configuration Space.
Lane 1 Configured	USB4 Port Region in Vendor Specific Extended 6 Capability of the Router Configuration Space.
Lane 0 is Inter-Domain	USB4 Port Region in Vendor Specific Extended 6 Capability of the Router Configuration Space.
Lane 1 is Inter-Domain	USB4 Port Region in Vendor Specific Extended 6 Capability of the Router Configuration Space.
Inter-Domain Disconnect on Sleep	USB4 Port Region in Vendor Specific Extended 6 Capability of the Router Configuration Space.
Enable Wake on Inter-Domain	USB4 Port Region in Vendor Specific Extended 6 Capability of the Router Configuration Space.
Enable Wake Events	USB4 Port Region in Vendor Specific Extended 6 Capability of the Router Configuration Space.

If the USB4 Port is disconnected while in sleep state, then the internal Lane 0 is Inter-Domain state, Lane 0 Configured state, Lane 1 is Inter-Domain state, and Lane1 Configured state listed in Table 13-9 shall all transition to 0b.

13.2.4.3 Wake Events

A Device Router shall support all the wake events listed in the *Enable Wake Events* field of the USB4 Port Region in the Vendor Specific Extended 6 Capability of the Router Configuration Space.

13.2.4.4 Exit from Sleep

A Device Router shall not start Lane Initialization for Lane 0 until the *Start Link Initialization* bit is set to 1b, if either of the following is true on exit from sleep:

- The *Lane 0 Configured* state is set to 0b.
- The *Lane 0 is Inter-Domain* bit is 1b.

A Device Router shall not start Lane Initialization for Lane 1 until the *Start Link Initialization* bit is set to 1b, if either of the following is true on exit from sleep:

- The *Lane 1 Configured* state is set to 0b.
- The *Lane 1 is Inter-Domain* bit is 1b.

13.2.5 Timing Parameters

Table 13-10 lists changes in timing parameters for the Logical Layer.

Table 13-10. Logical Layer Timing Parameters

Parameter	Description	Min	Max	Units
tLTPhase4	The amount of time that Broadcast RT Transactions, LT_Gen_2 Transactions, or LT_Gen_3 Transactions are sent after completion of Lane Initialization Phase 2.	25		ms
tLaneParams	The time interval between transmissions of LT_Gen_2 Transactions, between the transmissions of LT_Gen_3 Transactions, or between the transmissions of Broadcast RT Transactions.	1	5	ms
tTxFFETimeout	The amount of time that a Lane Adapter waits for the other Lane Adapter to update its TxFFE parameters before continuing negotiation.	80		ms
tTrainingAbort1	The amount of time in Training state following Lane Initialization.	2	--	sec

13.3 Transport Layer

13.3.1 Adapter Numbering Rules

This section only applies to a Device Router that supports TBT3-Compatibility on its Upstream Facing Port.

If bits 15:12 in the *Connection Manager USB4 Version* field in Router Configuration Space Basic Attributes are 0b (indicating a TBT3 Connection Manager), a Device Router shall expose either one or two USB4 Ports. If the Device Router supports PCIe Tunneling, it shall only expose the PCIe Adapters that are related to the exposed USB4 Ports. The method to signify that an Adapter is invalid is defined in Section 5.2.1. The Lane Adapters in the exposed USB4 Ports shall be assigned consecutive Adapter Numbers, starting from 1.

If any of bits 15:12 in the *Connection Manager USB4 Version* field are 1b (indicating a Connection Manager that supports USB4 Version 1.0 or higher), a Device Router may expose additional USB4 Ports and/or additional PCIe Adapters. A Router that exposes additional USB4 Ports and/or additional PCIe Adapters shall do so immediately when the *Connection Manager USB4 Version* field is set to a non-zero value.

13.3.2 Maximum HopID

This section applies to Host Routers and Device Routers.

The *Max Input HopID* and *Max Output HopID* fields in a Lane Adapter shall be at least 15 for USB4 Hosts and USB4 Hubs.

The *Max Input HopID* and *Max Output HopID* fields in a Lane Adapter of a USB4 Device supporting one DisplayPort tunneled stream shall be at least 11.

The *Max Input HopID* and *Max Output HopID* fields in a Lane Adapter of a USB4 Device supporting two DisplayPort tunneled streams shall be at least 14.

13.3.3 Buffer Allocation

This section only applies to a Device Router that supports TBT3-Compatibility on its Upstream Facing Port.

A TBT3 Connection Manager sets the buffer allocation in a static manner, according to Table 13-11.

Table 13-11. Buffer Allocation by TBT3 Connection Manager

	Aggregated Link	Single Lane Link
Control Path	Assumes 2 buffers	
PCIe Path	32 buffers	16 buffers
Host-to-Host Path	14 buffers	6 buffers
DP Aux Path	1 buffer	
DP Main-Link Path	The remaining buffers = Total Buffers – 50 ¹	The remaining buffers = Total Buffers – 26 ¹
<i>Note 1: A TBT3 CM assumes two DP Tunnels through a port, therefore it will keep 2 buffers for DP Aux Path.</i>		

13.4 Configuration Layer

This section only applies to a Device Router that supports TBT3-Compatibility on its Upstream Facing Port.

13.4.1 Domain Topology

A Spanning Tree contains up to seven levels (depths 0 through 6). The Host Router is at the top of the Spanning Tree (depth = 0). Device Routers are connected at depths 1 through 6 (inclusive). A Connection Manager accesses a Domain through the Host Router of that Domain.

13.4.2 Router Addressing

A Connection Manager assigns each Router in its Domain a unique topological address called a TopologyID. The TopologyID represents the position of the Router within the Domain's Spanning Tree.

The TopologyID is a sequence of seven Adapter numbers representing the Lane 0 Adapter in the Downstream Facing Ports at each level of the Spanning Tree between the Host Router and the Router. The TopologyID of a Host Router is always 0,0,0,0,0,0. The TopologyID for a Device Router at depth X (where X is from 1 to 6) is denoted as 0,...,0,Px-1,Px-2,...,P0 where Pn is the Adapter Number of the Adapter in the Downstream Facing Port at level n.

13.4.3 Router Enumeration

On transition to the Uninitialized state, a Router shall:

- Expose USB4 Ports and PCIe Adapters as defined in Section 13.3.1.
- Set its sleep and wake behavior as defined in Section 13.2.4.

- Expose the additional registers defined in Section 13.6.

The Router is enumerated when the *TopologyID Valid* bit is set to 1b.

Following enumeration, if bits 15:12 in the *Connection Manager USB4 Version* field in Router Configuration Space Basic Attributes are 0b (indicating a TBT3 Connection Manager), then the Router shall maintain the configuration listed above. The Router may set the *Router Ready* bit to 1b.

Following enumeration, if any of bits 15:12 in the *Connection Manager USB4 Version* field are 1b (indicating a Connection Manager that supports USB4 Version 1.0 or higher), then the Router shall follow Section 6.7.

13.4.4 Notification Packet

If bits 15:12 in the *Connection Manager USB4 Version* field in Router Configuration Space are 0b (indicating a TBT3 Connection Manager), a Hot Plug Acknowledgment Packet may have the *PG* bit set to 00b.

13.4.5 Bit Banging Interface

A Router shall support the “bit banging” interface defined in Vendor Specific 1 Capability (see Section 13.6.1.1).

A Router shall respond when the byte at address 0Ah is read. The Router may return any value.

A Router shall return the value 00000080h when the 32 bits at addresses [78h:75h] are read.

A Router shall return the value 01h when the byte at address 0148h is read.

A Router shall return the value 00000111h when the 32 bits at addresses [1A7h:1A4h] are read.



CONNECTION MANAGER NOTE

A Connection Manager reads the contents of a DROM attached to a TBT3 Router using the “bit banging” interface. The bit banging interface uses four bits (FL_SK, FL_CS, FL_DI, and FL_DO) to read from the flash memory of a device. The Connection Manager toggles the FL_CS, FL_CK, and FL_DI bits as defined in DW 4 of the Vendor Specific 1 Capability (see Section 13.6.1.1). The Connection Manager reads the resulting data output from the FL_DO bit.

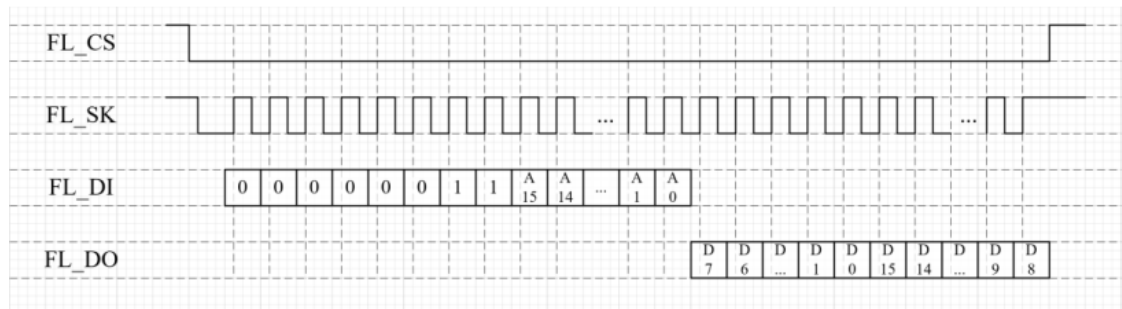
When using the bit banging interface, a Connection Manager sends the following bytes on FL_DI:

- *Byte 1 is a read command (03h)*
- *Byte 2 is bits [15:8] of the address to be read*
- *Byte 3 is bits [7:0] of the address to be read*

The Connection Manager then reads the resulting data from the FL_DO bit as follows:

- *Byte 1 is bits [7:0] of the read data*
- *Byte 2 is bits [15:8] of the read data (if present)*

The waveform below shows an example of how the FL_SK, FL_CS, FL_DI, and FL_DO are used:

Figure 13-3. Bit Banging Waveform Example

Note that all bytes are sent and received with the most significant bit first.

A Connection Manager can read from DROM or from any of the addresses listed in this section. When reading DROM, the base address can be read from the DROM Base Address field.

13.5 Time Synchronization

This section only applies to a Device Router that supports TBT3-Compatibility on its Upstream Facing Port.

When a USB4 Port is operating as two Single-Lane Links in TBT3 mode, the Time Sync Handshake shall occur on Lane 0.

A Device Router shall implement an additional *Time Disruption* bit as defined in Section 13.6.1.3. This bit is used by the TBT3 Connection Manager to indicate to the Router when a time disruption event is occurring. A Router shall OR the two *Time Disruption* bits to conclude if a time disruption event is occurring.

A Device Router shall implement an additional set of Time Posting registers as defined in Section 13.6.1.3. Those registers are used by the TBT3 Connection Manager to post the time to a Router. A Router shall react to Time Posting if one of the register sets are used. Both register sets have the same effect on LocalTime.

13.6 Configuration Spaces

This section only applies to a Device Router that supports TBT3-Compatibility on its Upstream Facing Port.

This section defines the additional registers and register fields that are used by a TBT3 Connection Manager. If the Link on the Router's Upstream Facing Port is TBT3 Mode and bits 15:12 in the *Connection Manager USB4 Version* field in Router Configuration Space are 0b (indicating a TBT3 Connection Manager), the register definitions in this section replace the register definitions in Chapter 8.



CONNECTION MANAGER NOTE

Only a TBT3 Connection Manager should use the registers defined in this section. A Connection Manager that supports USB4 Version 1.0 or higher shall not use the registers in this section.

Table 13-12 defines additional access types that are allowed for a particular configuration register field.

Table 13-12. Configuration Register Fields Access Types

Access Type	Description
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TBT3	TBT3-Compatible. TBT3 Connection Managers uses this field. A write to this field shall have no effect. A read returns a vendor-defined value.
------	--

13.6.1 Router Configuration Space



CONNECTION MANAGER NOTE

A Connection Manager shall not change the value in the Upstream Adapter field of a Host Router.

Table 13-13 lists the TBT3-Compatible Capabilities in Router Configuration Space. A Capability listed as “Required” shall be present in Router Configuration Space.

Table 13-13. List of TBT3-Compatible Router Configuration Capabilities

Capability	Required / Optional	Capability ID
<i>TMU Router Configuration</i>	Required	03h
<i>Vendor Specific 1 Capability</i>	Required	05h
<i>Vendor Specific 3 Capability</i>	Required	05h
<i>Vendor Specific 4 Capability</i>	Optional	05h
<i>Vendor Specific Extended 6 Capability</i>	Required	05h

13.6.1.1 Basic Configuration Registers

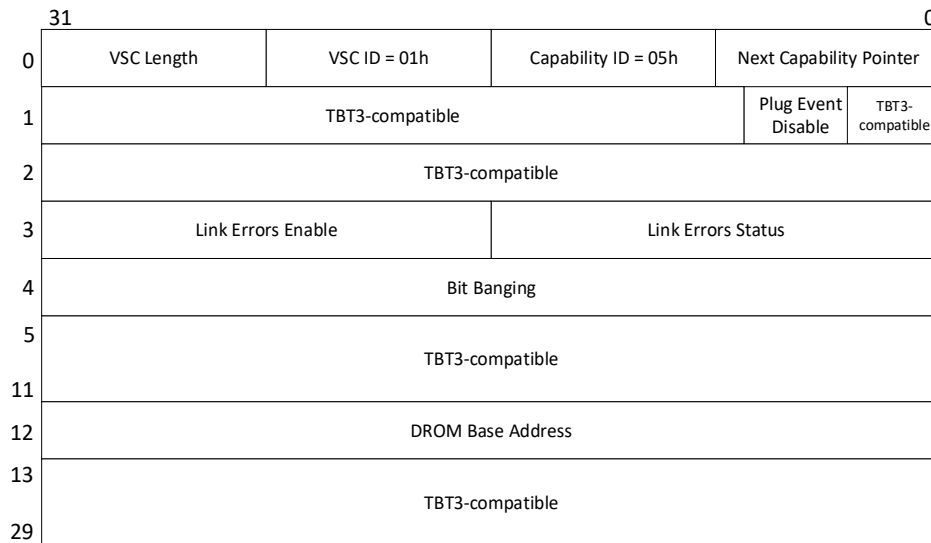
A Router shall support the Router Configuration Space Basic Attributes in Table 13-14.

Table 13-14. Router Configuration Space Basic Attributes

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	ROUTER_CS_1	22:20	Depth This field contains the number of hops from the Router to the Host Router in the Spanning Tree topology. A Router shall support Depths up to and including 5. It is recommended that a Router support depth of 6.	R/W	0

13.6.1.2 Vendor Specific 1 Capability

A Vendor Specific 1 Capability shall have the structure depicted in Figure 13-4 and the fields defined in Section 13.6.1.5.1. The Absolute address of the VSC_CS_0 register shall be 0x28.

Figure 13-4. Structure of the Vendor Specific 1 Capability**Table 13-15. Vendor Specific 1 Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSC_CS_0	7:0	Next Capability Pointer This field contains the Doubleword index of the next Capability in Router Configuration Space. It shall be set to 00h if the Vendor Specific Capability is the final Capability in the linked list of Capabilities in Router Configuration Space.	RO	Vendor Defined
		15:8	Capability ID This field shall contain the value 05h indicating this is the start of a Vendor Specific Capability.	RO	05h
		23:16	VSC ID This field shall contain the value 01h indicating this is a Vendor Specific 1 Capability.	RO	01h
		31:24	VSC Length This field shall contain the total number of Doublewords in the VSC structure including Doubleword 0 and the Vendor Specific Doublewords that follow.	RO	30
1	VSC_CS_1	2:0	TBT3-Compatible	TBT3	0
		6:3	Plug Event Disable This field is used by a Connection Manager to stop a Router from sending Hot Plug Event Packets for a specific type of Adapter. When a bit in this field is set to 1b, a Router shall not send a Hot Plug Event Packet when a Hot Plug or a Hot Unplug takes place on an Adapter with the Adapter Type specified by the bit. Bit definitions within this field are: Bit 3: Lane Adapter Bit 4: DP OUT Adapter Bit 5: DP IN Adapter (lowest numbered DP IN Adapter) Bit 6: DP IN Adapter (next numbered DP IN Adapter)	R/W	0
		31:7	TBT3-Compatible	TBT3	0
2	VSC_CS_2	31:0	TBT3-Compatible	TBT3	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
3	VSC_CS_3	0	Link Errors – Adapter A* A Router shall set this field to 1b when the <i>Link Errors Enable – Adapter A</i> bit is 1b and one of the bits in the <i>Logical Layer Errors of Adapter A</i> is set to 1b. This bit is not valid if the <i>Link Errors Enable – Adapter A</i> bit is 0b. * Adapter A is the lowest-numbered Lane Adapter.	W/Clr	0b
		1	HEC Error – Adapter A A Router shall set this field to 1b when the <i>HEC Errors Enable – Adapter A</i> bit is 1b and a Transport Layer Packet is received on Adapter A with an uncorrectable HEC error in the header. This bit is not valid if the <i>HEC Error Enable – Adapter A</i> bit is 0b.	W/Clr	0b
		2	Flow Control Error – Adapter A A Router shall set this field to 1b when the <i>Flow Control Errors Enable – Adapter A</i> bit is 1b and a Transport Layer Packet is received on Adapter A for a flow controlled Path where the appropriate buffer (dedicated or shared) has no space for the Packet or is not enabled. This bit is not valid if the <i>Flow Control Error Enable – Adapter A</i> bit is 0b.	W/Clr	0b
		3	Reserved	Rsvd	0b
		4	Link Errors – Adapter B* A Router shall set this field to 1b when the <i>Link Errors Enable – Adapter B</i> bit is 1b and one of the bits in the <i>Logical Layer Errors of Adapter B</i> is set to 1b. This bit is not valid if the <i>Link Errors Enable – Adapter B</i> bit is 0b. * Adapter B is the second lowest-numbered Lane Adapter	W/Clr	0b
		5	HEC Error – Adapter B A Router shall set this field to 1b when the <i>HEC Errors Enable – Adapter B</i> bit is 1b and a Transport Layer Packet is received on Adapter B with an uncorrectable HEC error in the header. This bit is not valid if the <i>HEC Error Enable – Adapter B</i> bit is 0b.	W/Clr	0b
3	VSC_CS_3	6	Flow Control Error – Adapter B A Router shall set this field to 1b when the <i>Flow Control Errors Enable – Adapter B</i> bit is 1b and a Transport Layer Packet is received on Adapter B on a flow controlled Path and the appropriate buffer (dedicated or shared) has no space for the Packet or is not enabled. This bit is not valid if the <i>Flow Control Error Enable – Adapter B</i> bit is 0b.	W/Clr	0b
		7	Reserved	Rsvd	0b
		8	Link Errors – Adapter C* A Router shall set this field to 1b when the <i>Link Errors Enable – Adapter C</i> bit is 1b and one of the bits in the <i>Logical Layer Errors of Adapter C</i> is set to 1b. This bit is not valid if the <i>Link Errors Enable – Adapter C</i> bit is 0b. * Adapter C is the third lowest-numbered Lane Adapter	W/Clr	0b

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		9	HEC Error – Adapter C A Router shall set this field to 1b when the <i>HEC Errors Enable – Adapter C</i> bit is 1b and a Transport Layer Packet is received on Adapter C with an uncorrectable HEC error in the header. This bit is not valid if the <i>HEC Error Enable – Adapter C</i> bit is 0b.	W/Clr	0b
		10	Flow Control Error – Adapter C A Router shall set this field to 1b when the <i>Flow Control Errors Enable – Adapter C</i> bit is 1b and a Transport Layer Packet is received on Adapter C on a flow controlled Path and the appropriate buffer (dedicated or shared) has no space for the Packet or is not enabled. This bit is not valid if the <i>Flow Control Error Enable – Adapter C</i> bit is 0b.	W/Clr	0b
		11	Reserved	Rsvd	0b
		12	Link Errors – Adapter D* A Router shall set this field to 1b when the <i>Link Errors Enable – Adapter D</i> bit is 1b and one of the bits in the <i>Logical Layer Errors of Adapter D</i> is set to 1b. This bit is not valid if the <i>Link Errors Enable – Adapter D</i> bit is 0b. * Adapter D is the fourth lowest-numbered Lane Adapter	W/Clr	0b
		13	HEC Error – Adapter D A Router shall set this field to 1b when the <i>HEC Errors Enable – Adapter D</i> bit is 1b and a Transport Layer Packet is received on Adapter D with an uncorrectable HEC error in the header. This bit is not valid if the <i>HEC Error Enable – Adapter D</i> bit is 0b.	W/Clr	0b
		14	Flow Control Error – Adapter D A Router shall set this field to 1b when the <i>Flow Control Errors Enable – Adapter D</i> bit is 1b and a Transport Layer Packet is received on Adapter D on a flow controlled Path and the appropriate buffer (dedicated or shared) has no space for the Packet or is not enabled. This bit is not valid if the <i>Flow Control Error Enable – Adapter D</i> bit is 0b.	W/Clr	0b
		15	Reserved	Rsvd	0b
3	VSC_CS_3	16	Link Errors Enable – Adapter A A Connection Manager uses this field to enable Link error reporting for Adapter A.	R/W	0b
		17	HEC Error Enable – Adapter A A Connection Manager uses this field to enable HEC error reporting for Adapter A.	R/W	0b
		18	Flow Control Error Enable – Adapter A A Connection Manager uses this field to enable Flow Control error reporting for Adapter A.	R/W	0b
		19	Reserved	Rsvd	0b
		20	Link Errors Enable – Adapter B A Connection Manager uses this field to enable Link error reporting for Adapter B.	R/W	0b
		21	HEC Error Enable – Adapter B A Connection Manager uses this field to enable HEC error reporting for Adapter B.	R/W	0b

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		22	Flow Control Error Enable – Adapter B A Connection Manager uses this field to enable Flow Control error reporting for Adapter B.	R/W	0b
		23	Reserved	Rsvd	0b
		24	Link Errors Enable – Adapter C A Connection Manager uses this field to enable Link error reporting for Adapter C.	R/W	0b
		25	HEC Error Enable – Adapter C A Connection Manager uses this field to enable HEC error reporting for Adapter C.	R/W	0b
		26	Flow Control Error Enable – Adapter C A Connection Manager uses this field to enable Flow Control error reporting for Adapter C.	R/W	0b
		27	Reserved	Rsvd	0b
		28	Link Errors Enable – Adapter D A Connection Manager uses this field to enable Link error reporting for Adapter D.	R/W	0b
		29	HEC Error Enable – Adapter D A Connection Manager uses this field to enable HEC error reporting for Adapter D.	R/W	0b
		30	Flow Control Error Enable – Adapter D A Connection Manager uses this field to enable Flow Control error reporting for Adapter D.	R/W	0b
		31	Reserved	Rsvd	0b
4	VSC_CS_4	0	FL_SK When the <i>Bit Banging Enable</i> bit is set to 1b, a Router shall drive the value of this bit to the clock pin of the Flash memory device.	R/W	0b
		1	FL_CS When the <i>Bit Banging Enable</i> bit is set to 1b, a Router shall drive the value of this bit to the chip select pin of the Flash memory device.	R/W	0b
		2	FL_DI When the <i>Bit Banging Enable</i> bit is set to 1b, a Router shall drive the value of this bit to the data input pin of the Flash memory device.	R/W	0b
4	VSC_CS_4	3	FL_DO When the <i>Bit Banging Enable</i> bit is set to 1b, a Router shall set the value of this bit to reflect the data output pin of the Flash memory device.	RO	0b
		4	Bit Banging Enable A Connection Manager sets this bit to 1b to map the FL_SK, FL_CS, FL_DI, and FL_DO bits to the respective pins on the Flash memory interface. When this bit is set to 0b, the values of the FL_SK, FL_CS, FL_DI, and FL_DO bits are not valid.	R/W	0b
		5	Invalid Flash Memory A Router shall set this bit to 0b if it has a Flash Memory that can be accessed via bit banging. Otherwise, this bit shall be set to 1b.	RO	Vendor Defined
		31:6	TBT3-Compatible	TBT3	0
5 to 11		31:0	TBT3-Compatible	TBT3	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
12	VSC_CS_12	31:0	DROM Base Address This field shall contain the base address (in bytes) of the DROM within the Flash Memory address space. This field shall be between 0000_0001h and (0000_FFFFh minus the DROM size).	RO	Vendor Defined
13 to 29		31:0	TBT3-Compatible	TBT3	0

13.6.1.3 Vendor Specific 3 Capability

A Vendor Specific 3 Capability shall have the structure depicted in Figure 13-5 and the fields defined in Table 13-16.

Figure 13-5. Structure of the Vendor Specific 3 Capability

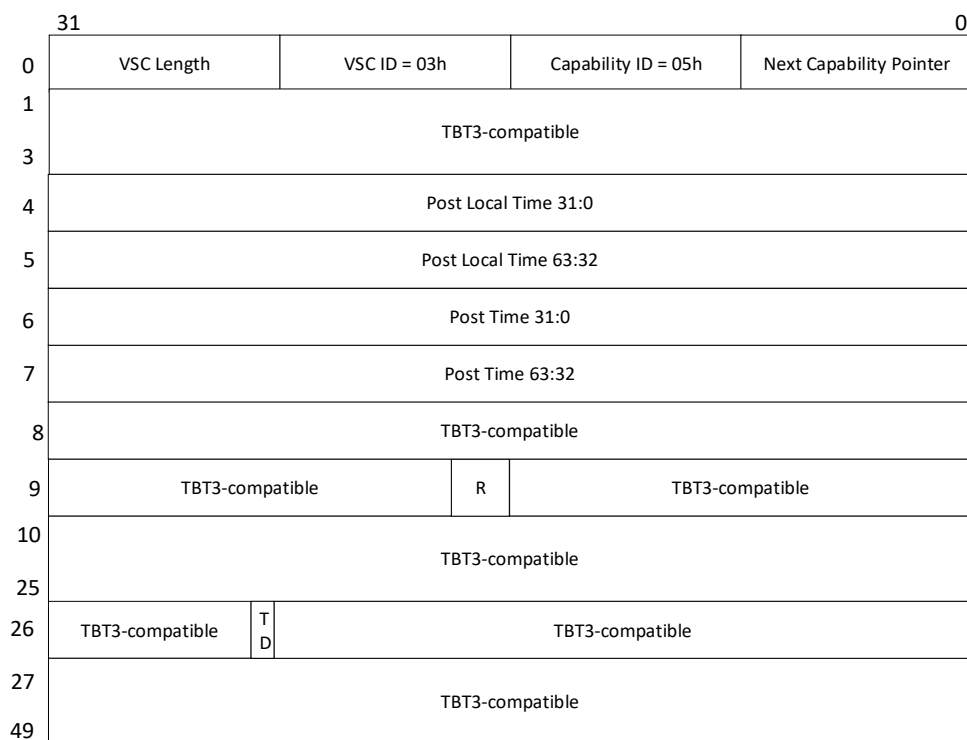


Table 13-16. Vendor Specific 3 Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSC_CS_0	7:0	Next Capability Pointer This field contains the Doubleword index of the next Capability in Router Configuration Space. It shall be set to 00h if the Vendor Specific Capability is the final Capability in the linked list of Capabilities in Router Configuration Space.	RO	Vendor Defined
		15:8	Capability ID This field shall contain the value 05h indicating this is the start of a Vendor Specific Capability.	RO	05h
		23:16	VSC ID This field shall contain the value 03h indicating this is a Vendor Specific 3 Capability.	RO	03h

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		31:24	VSC Length This field shall contain the total number of Doublewords in the VSC structure including Doubleword 0 and the Vendor Specific Doublewords that follow.	RO	50
1 to 3		31:0	TBT3-Compatible	TBT3	0
4	VSC_CS_4	31:0	Post Local Time Low This field contains the value that is used to update the least significant 32 bits of the <i>nanoseconds</i> field (i.e. bits 47 to 16) of the LocalTime register when the Post Time (VSC_CS_6/VSC_CS_7) is less or equal to the Host Router Time.	R/W	0
5	VSC_CS_5	31:0	Post Local Time High This field contains the value that is used to update the most significant 32 bits of the <i>nanoseconds</i> (i.e. bits 79 to 48) field of the LocalTime register when the Post Time (VSC_CS_6/VSC_CS_7) less or equal to the Host Router Time.	R/W	0
6	VSC_CS_6	31:0	Post Time Low This field contains the least significant 32 bits of the <i>Nanoseconds</i> field of the Host Router Time register at which the software updates to the LocalTime register are applied. The update occurs when the Post Time is greater than zero and is less or equal to the Host Router Time. When the Local Time is updated, this register is nullified <u>A Router shall set this field to 0 after updating its Local Time.</u>	R/W	0
7	VSC_CS_7	31:0	Post Time High This field contains the most significant 32 bits of the <i>Nanoseconds</i> field of the Host Router Time register at which the software updates to the LocalTime register are applied. The update occurs when the Post Time is greater than zero and is less or equal to the Host Router Time. To activate Time Posting, this register should be the last to be written. When the Local Time is updated, this register is nullified <u>A Router shall set this field to 0 after updating its Local Time.</u>	R/W	0
8	VSC_CS_8	31:0	TBT3-Compatible	TBT3	0
9	VSC_CS_9	15:0	TBT3-Compatible	TBT3	0
		17:16	Reserved	RO	0b
		31:18	TBT3-Compatible	TBT3	0
10 to 25		31:0	TBT3-Compatible	TBT3	0
26	VSC_CS_26	21:0	TBT3-Compatible	TBT3	0
		22	Time Disruption (TD) The Connection Manager sets this bit to 1b before any of the following time disruptions: <ul style="list-style-type: none"> • TMU mode changes (TSPacketInterval, Direction, Filters, Frequency Measurement Window) • Inter-Domain time sync is enabled • Time Posting is applied After the time disruption has passed, the Connection Manager sets this bit to 0b.	R/W	0b

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		31:23	TBT3-Compatible	TBT3	0
27 to 49		31:0	TBT3-Compatible	TBT3	0

13.6.1.4 Vendor Specific 4 Capability

If a Router implements Vendor Specific 4 Capability, the first 11 Doublewords shall have the structure depicted in Figure 13-6 and the fields defined in Table 13-17.

Figure 13-6. Structure of the Vendor Specific 4 Capability

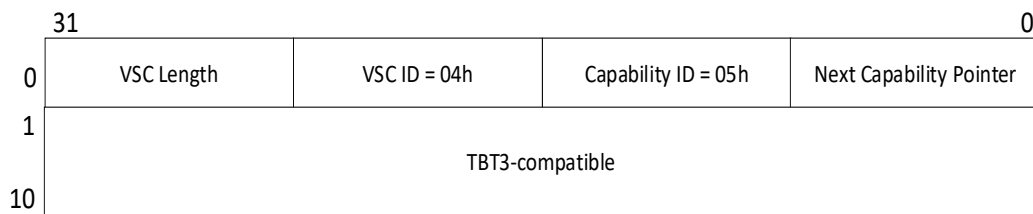


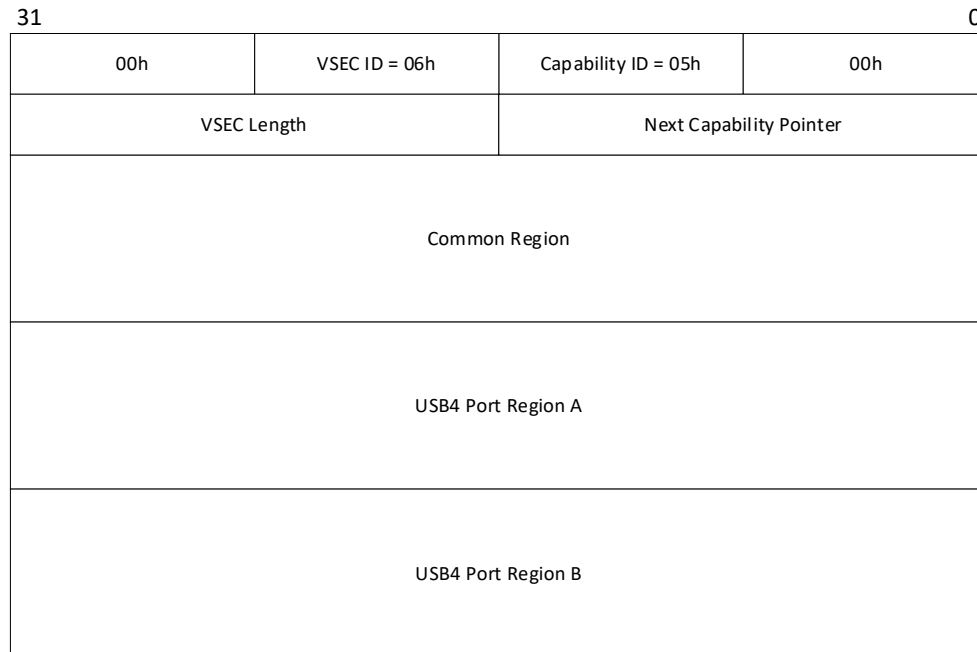
Table 13-17. Vendor Specific 4 Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSC_CS_0	7:0	Next Capability Pointer This field contains the Doubleword index of the next Capability in Router Configuration Space. It shall be set to 00h if the Vendor Specific Capability is the final Capability in the linked list of Capabilities in Router Configuration Space.	RO	Vendor Defined
		15:8	Capability ID This field shall contain the value 05h indicating this is the start of a Vendor Specific Capability.	RO	05h
		23:16	VSC ID This field shall contain the value 04h indicating this is a Vendor Specific 4 Capability.	RO	04h
		31:24	VSC Length This field shall contain the total number of Doublewords in the VSC structure including Doubleword 0 and the Vendor Specific Doublewords that follow.	RO	Vendor Defined
1 to 10		31:0	TBT3-Compatible	TBT3	0

13.6.1.5 Vendor Specific Extended 6 Capability

A Vendor Specific Extended 6 Capability shall have the structure depicted in Figure 13-7 and the fields defined in Section 13.6.1.5.1 and Section 13.6.1.5.2.

Figure 13-7. Structure of the Vendor Specific Extended 6 Capability



A USB4 Port Region shall exist for the two USB4 Ports with the lowest Adapter Numbers. The first USB4 Port Region (USB4 Port Region A) shall contain information about the USB4 Port with the lowest Adapter Numbers. The second USB4 Port Region (USB4 Port Region B) shall contain information about the USB4 Port with the next lowest Adapter Numbers. If a Router implements a single USB4 Port, it may respond to a Read Request or a Write Request to USB4 Port Region B with a Notification Packet with Event Code = ERR_ADDR. Such a Router may instead implement the registers in USB4 Port Region B as Rsvd. A Router shall not use the address space of USB4 Port Region B for other usage.

13.6.1.5.1 Common Region

A Common Region shall have the structure depicted in Figure 13-8 and the fields defined in Table 13-18.

Figure 13-8. Structure of the Common Region

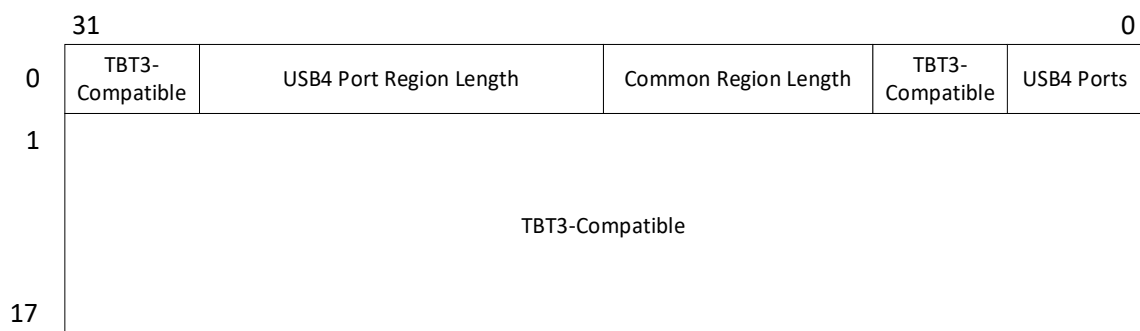


Table 13-18. Common Region Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	CAP_STRUCT	3:0	USB4 Ports This field shall contain the number of USB4 Ports supported by the Router. 1h – Single USB4 Port 2h – More than one USB4 Port All other values are reserved.	RO	Vendor Defined
		7:4	TBT3-Compatible	TBT3	0
		15:8	Common Region Length This field shall contain the size (in Doublewords) of the Common Region + 2.	RO	14h
		27:16	USB4 Port Region Length This field shall contain the size (in Doublewords) of a single USB4 Port Region.	RO	100h
		31:28	TBT3-Compatible	TBT3	0
1 to 17		31:0	TBT3-Compatible	TBT3	0

13.6.1.5.2 USB4 Port Regions

A USB4 Port Region shall have the structure depicted in Figure 13-9 and the fields defined in Table 13-19.

When a field in the USB4 Port Region has the same name as a register field in Configuration Space (as defined in Chapter 8), the field in the USB4 Port Region is used instead of the field in Configuration Space. For example, when operating with a TBT3 Connection Manager, a Device Router uses the *Enter Sleep* bit in the USB4 Port Region below instead of the *Enter Sleep* bit in Router Configuration Space to determine sleep and wake (see Section 4.4.7 and Section 13.2.4 for use of *Enter Sleep* bit).

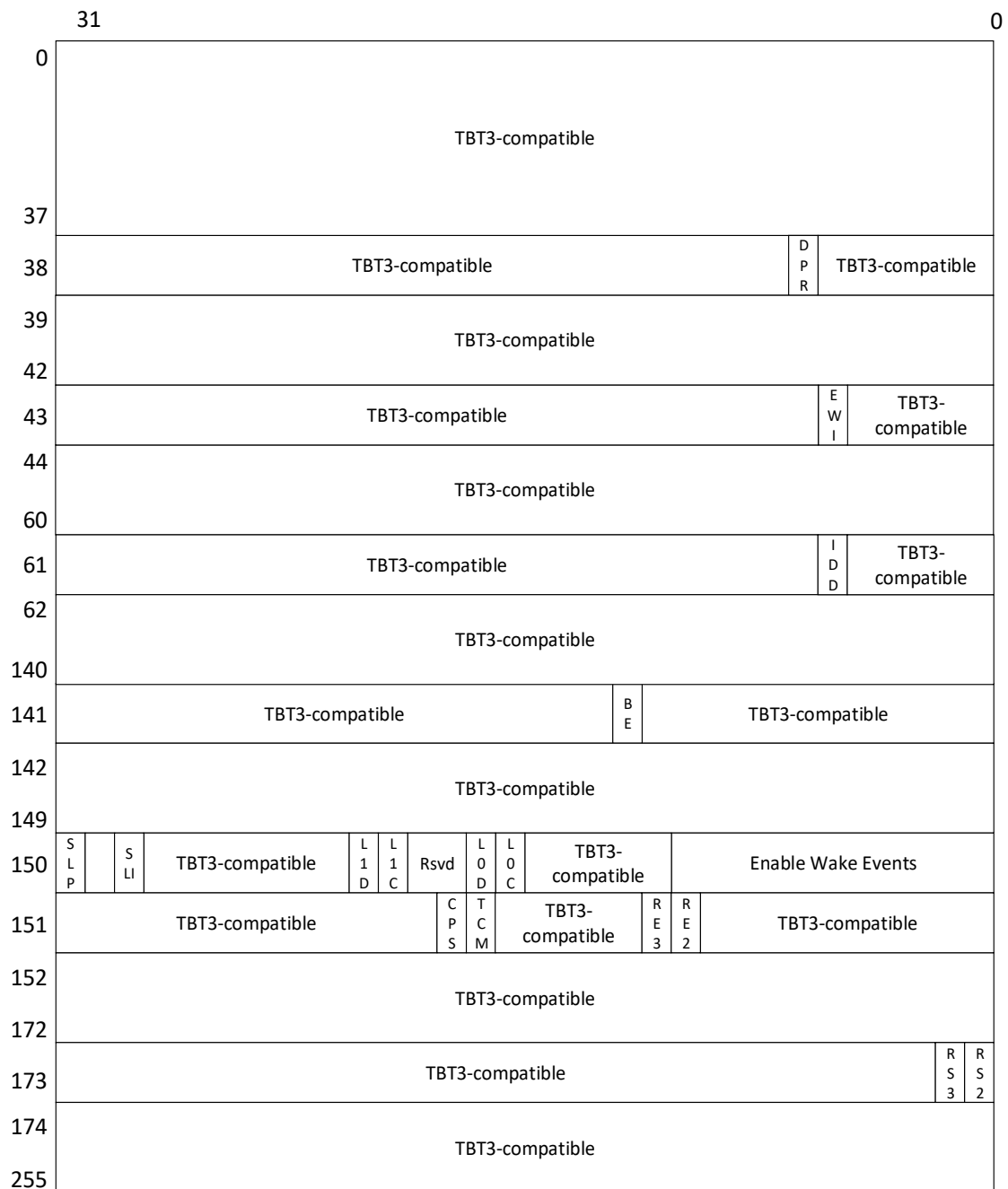
Figure 13-9. Structure of a USB4 Port Region

Table 13-19. USB4 Port Region Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0 to 37	-	31:0	TBT3-Compatible	TBT3	0
38	PORT_MODE	5:0	TBT3-Compatible	TBT3	0
		6	Downstream Port Reset (DPR) For a Downstream Facing Port: Setting this bit to 1b initiates a Downstream Port Reset. Setting this bit to 0b brings the USB4 Port out of a Downstream Port Reset. For an Upstream Facing Port: A read or write to this bit shall have no effect.	R/W	0b
		31:7	TBT3-Compatible	TBT3	0
39 to 42	-	31:0	TBT3-Compatible	TBT3	0
43	ID_WAKE	4:0	TBT3-Compatible	TBT3	0
		5	Enable Wake on Inter-Domain (EWI) A Connection Manager sets this bit to 1b to cause a Router to exit from sleep state when it detects an Inter-Domain Wake on the USB4 Port. The Connection Manager sets the <i>Inter-Domain Disconnect on Sleep</i> bit to 1b when this bit is 0b.	R/W	Vendor Defined
		31:6	TBT3-Compatible	TBT3	0
44 to 60	-	31:0	TBT3-Compatible	TBT3	0
61	ID_SLEEP	4:0	TBT3-Compatible	TBT3	0
		5	Inter-Domain Disconnect on Sleep (IDD) A Connection Manager sets this bit to 1b to cause a disconnect on the USB4 Port if the USB4 Port is connected to an Inter-Domain Link when the Router enters sleep state. When this field is 0b, the Connection Manager disables wake on a USB4 Wake in the <i>Enable Wake Events</i> field and sets the <i>Enable Wake on Inter-Domain</i> bit to 1b.	R/W	0b
		31:6	TBT3-Compatible	TBT3	0
62 to 140	-	31:0	TBT3-Compatible	TBT3	0
141	PORT_ATTR	11:0	TBT3-Compatible	TBT3	0
		12	Bonding Enabled (BE) An Adapter shall set this bit to 1b when the conditions for Lane bonding are met. See Section 4.1.2.3. An Adapter shall set this bit to 0b when the conditions for Lane bonding are not met.	RO	0
		31:13	TBT3-Compatible	TBT3	0
142 to 149	-	31:0	TBT3-Compatible	TBT3	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
150	LC_SX_CTRL	10:0	Enable Wake Events A Connection Manager uses this field to enable the various types of wake events. When a bit is set to 1b, the corresponding event shall cause a Router to exit from sleep. When a bit is set to 0b, the corresponding event shall not cause a Router to exit from sleep. bit 0: vendor specific event bit 1: wake on connect of a Router to the USB Type-C® connector bit 2: wake on disconnect of a Router to the USB Type-C connector bit 3: wake on connect of a DisplayPort device to the USB Type-C connector A Router may exit sleep on connect of a DisplayPort device to any DP connector if this bit is set in one of the USB4 Ports bit 4: wake on disconnect of a DisplayPort device to the USB Type-C connector bit 5: wake on a USB4 Wake detected on this Port bit 6: wake on a PCIe Wake indication bit 7: vendor specific event bit 8: vendor specific event bit 9: wake on connect of a USB device to the USB Type-C connector bit 10: wake on disconnect of a USB device to the USB Type-C connector	R/W	Host Router: 180h Else: 140h
		15:11	TBT3-Compatible	TBT3	0
150	LC_SX_CTRL	16	Lane 0 Configured (L0C) The Connection Manager sets this bit to 1b to indicate that the Router connected to Lane 0 of the USB4 Port is configured and that entry to sleep state and exit from sleep state shall be supported on the Lane. The Connection Manager sets this bit to 0b to indicate that the Router connected to Lane 0 of the USB4 Port is not configured and therefore the USB4 Port is disconnected on entry to sleep state.	R/W	0b
		17	Lane 0 is Inter-Domain (L0D) A Connection Manager sets this bit to 0b when Lane 0 is not part of an Inter-Domain Link. A Connection Manager sets this bit to 1b when Lane 0 is part of an Inter-Domain Link.	R/W	0b
		19:18	TBT3-Compatible	TBT3	0
		20	Lane 1 Configured (L1C) The Connection Manager sets this bit to 1b to indicate that the Router connected to Lane 1 of the USB4 Port is configured and that entry to sleep state and exit from sleep state shall be supported on the Lane. The Connection Manager sets this bit to 0b to indicate that the Router connected to Lane 1 of the USB4 Port is not configured and therefore the USB4 Port is disconnected on entry to sleep state.	R/W	0b
		21	Lane 1 is Inter-Domain (L1D) A Connection Manager sets this bit to 0b when Lane 1 is not part of an Inter-Domain Link. A Connection Manager sets this bit to 1b when Lane 1 is part of an Inter-Domain Link.	R/W	0b
		28:22	TBT3-Compatible	TBT3	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		29	Start Link Initialization (SLI) A Connection Manager uses this bit to delay Lane Initialization on a USB4 Port when a Router exits sleep state (See Section 13.2.4.4) 1b – The USB4 Port shall start Lane Initialization 0b – The USB4 Port shall not start Lane Initialization	R/W	0b
		30	TBT3-Compatible	TBT3	0
		31	Enter Sleep (SLP) A Connection Manager sets this bit to 1b to let the Router know that the system is preparing for entry to sleep state.	R/W	0b
151	LINK_ATTR	9:0	TBT3-Compatible	TBT3	0
		10	RS-FEC Enabled (Gen 2) (RE2) An Adapter shall set this bit to 1b when the USB4 Port is operating at Gen 2 speed and RS-FEC is enabled. This bit is set to 0b otherwise.	RO	0
		11	RS-FEC Enabled (Gen 3) (RE3) An Adapter shall set this bit to 1b when the USB4 Port is operating at Gen 3 speed and RS-FEC is enabled. This bit is set to 0b otherwise.	RO	0
		16:12	TBT3-Compatible	TBT3	0
		17	TBT3-Compatible Mode (TCM) An Adapter shall set this bit to 1b when the Link is operating in TBT3-Compatible Mode. This bit is set to 0b otherwise.	RO	0
151	LINK_ATTR	18	CLx Protocol Support (CPS) This bit indicates that the Router and the Cable support the Low Power protocol. When a Router supports the Low Power protocol, it either accepts or rejects entry to a CLx state as defined in Section 4.2.1.6. A Router shall set this bit to 1b if the Sideband Channel operates as a USB4 Sideband Channel and the Cable supports CLx states. Otherwise, Router shall set this bit to 0b. The value of this bit is applicable when the Adapter is not in CLd nor Disabled state.	RO	Vendor Defined
		31:19	TBT3-Compatible	TBT3	0
152 to 172	-	31:0	TBT3-Compatible	TBT3	0
173	LINK_REQ	0	Request RS-FEC Gen 2 (RS2) A Connection Manager sets this bit to 1b to enable RS-FEC encoding at 10G speeds. If this bit is set to 1b, the Router shall enable RS-FEC encoding at 10G speeds on the Links of this USB4 Port during the next Lane Initialization. If this bit is set to 0b, then RS-FEC enabling at 10G speeds is determined by the setting of the Link Partner.	R/W	0b

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		1	Request RS-FEC Gen 3 (RRS3) A Connection Manager sets this bit to 1b to enable RS-FEC encoding at 20G speeds. If this bit is set to 0b, the Router shall disable RS-FEC encoding at 20G speeds on the Links of this USB4 Port during the next Lane Initialization. If this bit is set to 1b, then RS-FEC enabling at 20G speeds is determined by the setting of the Link Partner.	R/W	1b
		31:2	TBT3-Compatible	TBT3	0
174 to 255	-	31:0	TBT3-Compatible	TBT3	0

13.6.2 Adapter Configuration Space

The Absolute address of the ADP_DP_CS_0 register in a DP Adapter Configuration Capability shall be 0x39.

A Device Router shall ignore an attempt to modify bit 8 in ADP_DP_CS_3 register of a DP OUT Adapter.

A TBT3 Connection Manager assumes that a Router has implemented a register at absolute address 0x10 in the DP OUT Adapter Configuration Space. When a DP OUT Adapter receives a Write Request that targets address 0x10, it shall send a Write Response. A DP OUT Adapter shall not implement a Capability Register at address 0x10 in its Adapter Configuration Space.

A DP IN Adapter shall not have a Vendor Specific Capability with VSC ID = 0 or VSC ID = 1.

A DP OUT Adapter shall not have a Vendor Specific Capability with VSC ID = 1.

A TBT3 Connection Manager may initiate a Read Request to the Basic Configuration Registers in the Adapter Configuration Space of the Control Adapter. A Device Router shall respond to such a request in one of the following two ways:

1. Send a Notification Packet with Event Code = ERR_ADP, as defined in Table 6-11.
2. Send a Read Response with the following values:
 - For ADP_CS_2, respond with value 0x01000001.
 - For any other address respond with any value.

13.6.2.1 Basic Attributes

An Adapter shall support the Adapter Configuration Space Basic Attributes in Table 13-20. A Lane 1 Adapter may optionally set any of the the *HEC Errors*, *Flow Control Error*, and/or *Shared Buffering Capable* bits to 1b.

Table 13-20. Adapter Configuration Space Basic Attributes (ADP_CS_4)

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
4	ADP_CS_4	31	Lock (LCK) This bit controls whether a Connection Manager can access a Router that is downstream of the Adapter. This bit is only used for the Adapters in a Downstream Facing Port. When the bit is 1b, the Adapter is “locked”, which means that Control Packets are not forwarded to the downstream Router. When the bit is 0b, the Adapter is “unlocked”, and Control Packets can be forwarded to the downstream Router. If the value in the <i>Connection Manager USB4 Version</i> field is greater than 0, an Adapter shall set this bit to 1b after the Adapter goes through a disconnect. If the value in the <i>Connection Manager USB4 Version</i> field is 0, an Adapter shall keep this bit set to 0b. An Adapter may ignore a write to this bit if the Adapter does not have a Router connected downstream. <i>Note: A TBT3 Connection Manager does not use this bit and the Adapter remains “unlocked” by default.</i>	R/W	0b

If a Router is a Device Router that supports DP Tunneling, an Adapter shall also support the Adapter Configuration Space Basic Attributes in Table 13-21.

Table 13-21. Adapter Configuration Space Basic Attributes (ADP_CS_3)

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
3	ADP_CS_3	9:0	TBT3 Total Buffers This field shall be equal to the <i>Total Buffers</i> field.	RO	Vendor Defined

13.6.2.2 USB4 Port Capability

An Adapter shall support the USB4 Port Capability fields in Table 13-22.

Table 13-22. USB4 Port Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	PORT_CS_1	18:16	Target This field defines which SB Register Space to access. <u>In addition to the Targets described in Table 8-13, a TBT3-Compatible Router shall also support these Targets:</u> 110b – Near-end Cable Re-timer (via AT Transaction) 111b – Far-end Cable Re-timer (via AT Transaction and using the Bounce mechanism)	R/W	0
19	PORT_CS_19	1	Request RS-FEC Gen 2 (RS2) A Connection Manager uses this bit to request enabling of RS-FEC encoding at Gen 2 speeds. If a Link is Active, the Link shall be re-initialized before RS-FEC can be enabled. If this bit is set to 1b, the USB4 Port shall enable RS-FEC at Gen 2 speeds during the next Lane Initialization. If this bit is set to 0b, then the Link Partner response determines whether RS-FEC is enabled at Gen 2 speeds.	R/W	1b

13.7 PCI Express Tunneling

A TBT3-Compatible Host Router shall support PCIe Tunneling.

13.7.1 PCIe Power Management

13.7.1.1 L1

If TBT3 Mode is established on a Link and the *USB4 Sideband Channel Support* bit at the Link Partner is set to 0b, then ASPM L1 operation over PCIe Tunneling is not supported. When ASPM L1 operation is not supported:

- If TBT3 Mode is established on a Downstream Facing Port, the state of the downstream port of the internal PCIe Switch that is connected to that Downstream Facing Port may be ignored when determining the conditions to enter L1 state on the upstream port of the internal PCIe Switch.
- If TBT3 Mode is established on the Upstream Facing Port, the upstream port of the internal PCIe Switch that is connected to that Upstream Facing Port shall disable L1.

If TBT3 Mode is established on a Link and the *USB4 Sideband Channel Support* bit of the Link Partner is set to 1b, then ASPM L1 operation over PCIe Tunneling is supported.

Note: Software L1 is always supported.

Note: The internal upstream PCIe port of a TBT3 Device, implements an L1 handshake timeout of 10 μ s for ASPM L1 and 2 μ s for Software L1, starting from sending EIOS and ending when an EIOS is received. If timeout expires, the internal upstream PCIe port enters Recovery state.

13.7.1.2 L2

Note: The internal upstream PCIe port of a TBT3 Device implements an L2 handshake timeout of 2 μ s, starting from sending EIOS and ending when an EIOS is received. If timeout expires, the internal upstream PCIe port enters either the Detect or Recovery states.

13.8 DisplayPort Tunneling

A DP Adapter shall operate in Non-LTTPR (TBT3-Compatible) mode when the *DP_COMMON_CAP.Protocol Adapter Version* value is less than 4. TBT3-Compatible mode is Non-LTTPR mode as defined in Chapter 10 with the modifications defined in this section.

13.8.1 AUX Handling

13.8.1.1 DP IN Adapter Requirements

A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.2 except the following:

- The Link Status DPCD registers, as defined in Table 10-10, shall be mapped statically as internal registers.
- DPCD address 00600h is mapped as internal register.
- An AUX Read Transaction to the LTTPR DPCD field (addresses F0000h-F02FFh) is mapped as internal registers. A DP IN Adapter shall set the data of the AUX Response to 0h.

A DP IN Adapter operating in TBT3-compatible mode follows the requirements listed in Section 10.4.4.5 except the following:

- *DSC Support* field in the DSC SUPPORT DPCD register shall always be set to 0b.
- *FEC_CAPABLE* field in FEC_CAPABILITY DPCD register shall always be set to 0b.

13.8.1.2 DP OUT Adapter Requirements

A DP OUT Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.3 except the following:

- Initiation of an AUX Transaction occurs for the following processes:
 - DPRX Capability Discovery – Defined in Section 13.8.3.2.
 - IRQ Handling – Defined in Section 13.8.2.
- A DP OUT Adapter operating in TBT3-Compatible mode shall set the Reserved field in an AUX Response Tunnel Packet to be equal to value it received in the corresponding AUX Request Tunnel Packet.

Note: A DP OUT Adapter operating in TBT3-Compatible mode could receive the Reserved byte at the end of the AUX Tunneled Packet with value other than zero.

13.8.2 IRQ Handling

When a DP OUT Adapter operating in TBT3-Compatible Mode detects an IRQ, it shall determine if the IRQ was issued to signify a DP Link loss. If the IRQ was initiated to signify a DP Link loss, the TBT3-Compatible DP OUT Adapter shall:

- Disable its Main-Link transmitters.
- Send a SET_CONFIG Packet of MSG type STATUS_LOST_CONNECTION.
- Transition to IDLE state as described in Section 13.8.6.2.

If the IRQ was not initiated to signify a DP Link loss, the DP OUT Adapter shall send a SET_CONFIG Packet of MSG type IRQ.

When a DP IN Adapter receives a SET_CONFIG Packet of MSG type STATUS_LOST_CONNECTION, it shall:

- Disable its Main-Link receivers and issue an IRQ to the DPTX.
- Transition to IDLE state as described in Section 13.8.6.1.

Note: It is expected that the system recovers from a DP Link failure as follows:

1. *DPTX receives an IRQ, reads the DP-Link status and discovers the DP-Link failure.*
2. *DPTX retrains the DP-Link.*

13.8.3 Connection Manager Discovery

13.8.3.1 TBT3 Connection Manager

The methods for detecting whether a TBT3 Connection Manager is present in a system is defined in Section 10.4.2.1. After determining that a system contains a TBT3 Connection Manager, a TBT3-Compatible DP OUT Adapter shall perform the following steps:

1. Send a Hot Removal Event Packet to the TBT3 Connection Manager.
2. Read DPRX capabilities by initiating an AUX read Request.
3. Update each field in the DP_LOCAL_CAP register to reflect the lowest common capabilities of:
 - DP OUT Adapter capabilities.
 - DPRX capabilities.
 - The capabilities defined in the DisplayPort Standard, Version 1.2.
4. Wait at least 150 ms.
5. Send a Hot Plug Event Packet to the TBT3 Connection Manager.

13.8.3.2 TBT3 Router Discovery

The methods for detecting whether a TBT3 Router is present in a system is defined in Section 10.4.2.1. After determining that the DP IN Adapter at the end of a Path is part of a TBT3 Router, a TBT3-Compatible DP OUT Adapter shall perform the following steps:

1. Read DPRX capabilities by initiating, at minimum, AUX read Requests to the following DPCD addresses.
 - 0000h-0000Eh
 - 00021h
 - 00200h
2. Update each field in the DP_LOCAL_CAP register to reflect the lowest common capabilities of:
 - DP OUT Adapter capabilities
 - DPRX capabilities
3. Reset DP_STATUS_CTRL.CMHS to zero.

**CONNECTION MANAGER NOTE**

When a Connection Manager detects a TBT3 Router with a DP Adapter, it shall do the following:

- *Set the Video HopID field in the DP Adapter Configuration Capability to 9.*
- *Set the AUX Tx HopID field in the DP Adapter Configuration Capability to 8.*
- *Set the AUX Rx HopID field in the DP Adapter Configuration Capability to 8.*

Note that in a TBT3 Router, the Video HopID, AUX Tx HopID, and AUX Rx HopID fields are R/W and default to 0.

13.8.4 Sink Count Read

A DP OUT Adapter, operating in TBT3-Compatible mode, shall read DPCD address 00200h as part of DPRX capability discovery. If the SINK_COUNT value read from the DPRX is 0b, the DP OUT Adapter shall follow the steps defined in Section 10.4.6.3, and shall not wait for a SINK_COUNT SET_CONFIG to be sent by the DP IN Adapter.

A DP IN Adapter, operating in TBT3-Compatible mode, may send a SET_CONFIG Packet of type SET_SINK_COUNT to query the value of the SINK COUNT.

A DP OUT Adapter, receiving a SET_CONFIG Packet of type SET_SINK_COUNT, shall respond to the DP IN Adapter with in tDPInit with a SET_CONFIG Packet of type SET_SINK_COUNT with the SINK_COUNT value equal to the value that was read from DPCD address 00200h.

13.8.5 Power States Set

When DPTX either reads or writes to DPCD address 00600h, a DP IN Adapter, operating in TBT3-Compatible mode shall:

- In case it is a write, respond with an AUX ACK and update its internal power state according to the SET_POWER_STATE of the write request.
- In case it is a read, respond with an AUX Response carrying its internal power state.
- Send a SET_CONFIG Packet of type SET_POWER, carrying the internal power state.

A DP OUT Adapter in TBT3-Compatible mode, receiving a SET_CONFIG Packet of type SET_POWER, shall initiate an AUX Write Request to DPCD address 00600h with the value written equal to the *MSG Data* received by the SET_CONFIG Packet.

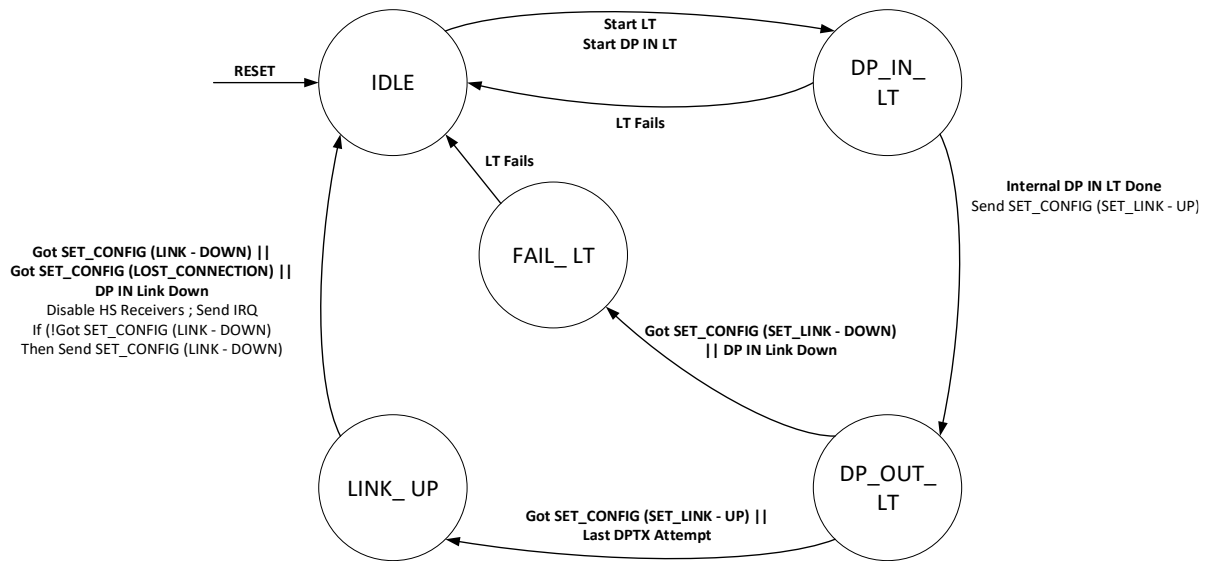
13.8.6 DisplayPort Link Training

The DisplayPort link training process in TBT3-Compatible is similar to the Non-LTTPR mode in that the DPTX is not aware of the second DisplayPort link being trained. However, it is different in that the two DisplayPort links are trained sequentially; the DP OUT Adapter starts its DisplayPort link training only when the DP IN Adapter has internally finished training its DisplayPort link.

A DP Adapter in TBT3-Compatible mode shall perform DisplayPort link training according to the DisplayPort Specification with the modifications and requirements defined in Section 13.8.6.1 and Section 13.8.6.2.

13.8.6.1 DP IN Adapter Requirements

DP IN Adapter shall follow the state machine described in Figure 13-10 and the transition table described in Table 13-23.

Figure 13-10. DP IN Adapter Link Training State Machine**Table 13-23. DP IN Adapter Link Training State Machine Transition Table**

Current State	Next State	Condition	Action
IDLE	DP_IN_LT	DPTX initiates DisplayPort link training as defined in the DisplayPort Specification.	DP IN Adapter performs DisplayPort link training.
DP_IN_LT	IDLE	DisplayPort link training between DPTX and the DP IN Adapter fails.	None.
DP_IN_LT	DP_OUT_LT	DP IN Adapter achieves LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK and INTERNAL_LANE_ALIGN on all active lanes.	DP IN Adapter sends a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR that matches the DisplayPort link training parameters set by the DPTX.
DP_OUT_LT	FAIL_LT	DP IN Adapter receives a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR equal to zero or the DisplayPort link between DPTX and the DP IN Adapter fails.	None.
DP_OUT_LT	LINK_UP	DP IN Adapter receives a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR not equal to zero or DPTX issues its last AUX status read attempt.	None.
LINK_UP	IDLE	Either: DP IN Adapter receives a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR equal to zero. or: DP IN Adapter receives a SET_CONFIG Packet of type STATUS_LOST_CONNECTION. or: The DisplayPort link between DPTX and the DP IN Adapter fails.	DP IN Adapter disables its Main-Link receivers, then sends an IRQ. If the transition is due to a failure of the DisplayPort link between DPTX and the DP IN Adapter, the DP IN Adapter sends a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR equal to zero.
FAIL_LT	IDLE	DisplayPort link training between DPTX and the DP IN Adapter fails.	None.

A DP IN Adapter shall respond to an AUX status read with LANEx_CHANNEL_EQ_DONE = 1b, LANEx_SYMBOL_LOCKED = 1b and INTERLANE_ALIGN_DONE = 1b on all active lanes is while in LINK_UP state. It shall not respond to an AUX status read with LANEx_CHANNEL_EQ_DONE = 1b, LANEx_SYMBOL_LOCKED = 1b and INTERLANE_ALIGN_DONE = 1b in any other states.

While in the DP_OUT_LT state or FAIL_LT state, a DP IN Adapter shall respond to AUX status read with LANEx_CHANNEL_EQ_DONE = 0 for all lanes.

13.8.6.2 DP OUT Adapter Requirements

A TBT3-Compatible DP OUT Adapter shall follow the state machine described in Figure 13-11 and the transition table described in Table 13-24.

Figure 13-11. DP OUT Adapter Link Training State Machine

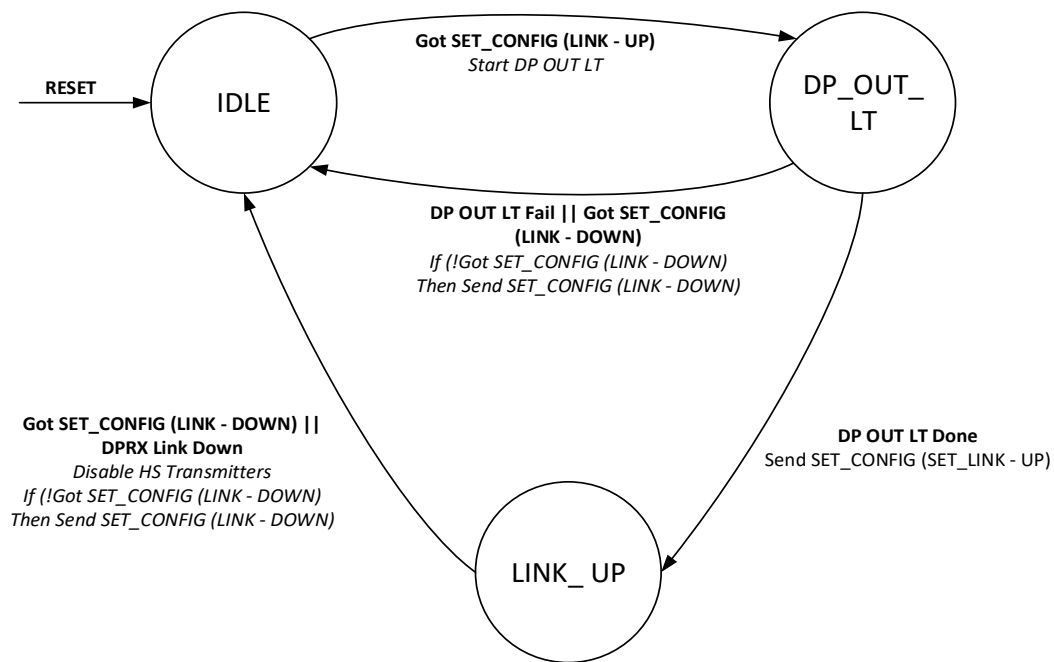


Table 13-24. DP OUT Adapter Link Training State Machine Transition Table

Current State	Next State	Condition	Action
IDLE	DP_OUT_LT	DP OUT Adapter receives a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR not equal to zero.	DP OUT Adapter performs DisplayPort link training.
DP_OUT_LT	IDLE	Either: DisplayPort link training between DPRX and the DP OUT Adapter fails to train the DisplayPort Link to the target LC and LR. or: DP OUT Adapter receives a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR equal to zero.	If the transition is due to failure of the DisplayPort link between DPRX and the DP OUT Adapter, The DP OUT Adapter sends a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR equal to zero.
DP_OUT_LT	LINK_UP	DPRX and DP OUT Adapter successfully train the DisplayPort link.	DP OUT Adapter sends a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR that matches the Link training parameters which were sent by the DP IN Adapter.

LINK_UP	IDLE	DP OUT Adapter receives a SET_CONFIG Packet of type 8B10B_SET_LINK with LC and LR equal to zero or DPRX reports link failure.	DP OUT Adapter disables its high speed transmitters. If the transition is due to DPRX reporting DisplayPort link failure, the DP OUT Adapter sends a SET_CONFIG packet of type 8B10B_SET_LINK with LC and LR equal to zero.
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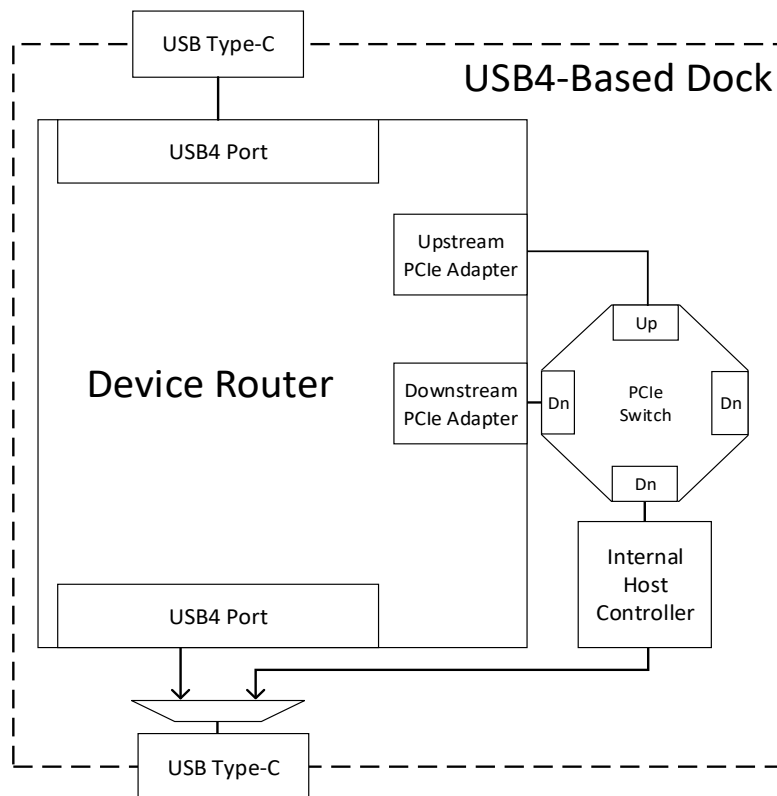
While performing DisplayPort link training, DP OUT Adapter shall use the target Link Rate and Lane Count received from the DP IN Adapter. If a DP OUT Adapter fails to train the DisplayPort link to the target parameters, it shall report DisplayPort link failure to the DP IN Adapter. It shall not attempt to apply the fallback mechanisms defined in the DisplayPort Specification.

13.9 USB3 Functionality

This section only applies to USB4-Based Docks and USB4 Hubs that support TBT3-Compatibility on their Upstream Facing Port.

A USB4-Based Dock or USB4 Hub shall incorporate an Internal USB3 Host Controller to support USB3 functionality. Figure 13-12 shows an example of a USB4-Based Dock that incorporates an Internal USB3 Host Controller.

Figure 13-12. Example of a USB4-Based Dock with an Internal Host Controller



The Device Router in a USB4-Based Dock or USB4 Hub shall set the *HCI* field to 1b.

During Router enumeration and initialization, after the Device Router sets the *Router Ready* bit to 1b and the Connection Manager sets the *Configuration Valid* bit to 1b, a Device Router in a USB4-Based Dock or USB4 Hub shall do the following in addition to the requirements defined in Section 6.7 before setting the *Configuration Ready* bit to 1b:

- If the *Internal Host Controller On* bit is set to 1b, establish USB3 functionality to/from the Internal USB3 Host Controller using PCIe tunneling.

**IMPLEMENTATION NOTE**

A Device Router may decide to establish USB3 functionality to/from the Internal USB3 Host Controller using PCIe tunneling when its Upstream Facing Port operates in TBT3 Mode.

**CONNECTION MANAGER NOTE**

If a Connection Manager intends to use the Internal USB3 Host Controller to establish USB3 functionality, then before setting up a PCIe Tunneling Path, the Connection Manager shall set the Internal Host Controller On bit to 1b and the Configuration Valid bit to 1b in Router Configuration Space Basic Attributes in the Device Router in the USB4-Based Dock or USB4 Hub. The Connection Manager then polls the Configuration Ready bit until it is set to 1b by the Device Router.

When a Connection Manager is going to tunnel USB3 traffic through a USB4-Based Dock or USB4 Hub, it can either enable USB3 functionality using the Internal USB3 Host Controller as described in this section (for TBT3 Mode only) or enable USB3 Tunneling using the Internal USB3 Component as described in Chapter 9 (for USB4 Mode only). It cannot enable both at the same time.

13.10 Host-to-Host Tunneling

No additional requirements.

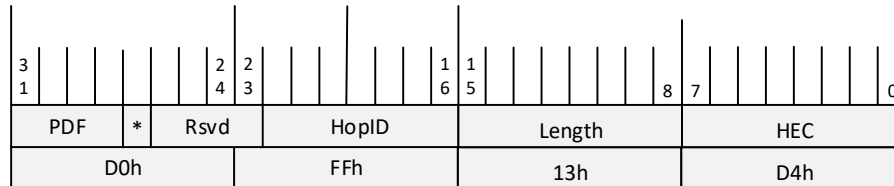
A Verification of CRC, Scrambling, and FEC Calculations

This Appendix gives several examples of CRC and FEC calculations.

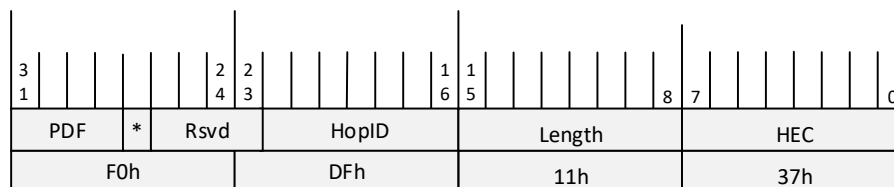
A.1 Transport Layer Packet HEC

Figure A-1 provides examples of HEC calculations for the Transport Layer Packet Header. In each example, the second line contains the values for the header depicted in the line above it.

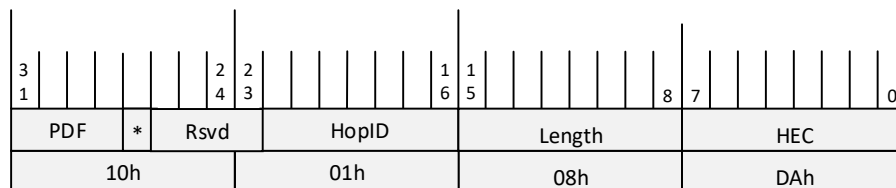
Figure A-1. Examples of Transport Layer Packet HEC Calculation



Example 1



Example 2



Example 3

* = SupplD

A.2 Control Packet CRC

Table A-1 provides examples of CRC calculation for Control Packets.

Table A-1. Examples of Control Packet CRC Calculation

	Route String High	Route String Low	Payload DW 0	Payload DW 1	CRC DW
Example 1 – Read Request	0000 0000h	0000 0000h	0400 2000h	-	2FC9 67ACh
Example 2 – Read Response	8000 0000h	0000 0000h	0428 2000h	1578 8086h	5A9B 0181h

A.3 Sideband Channel AT Transaction CRC

Table A-2 provides an example of a CRC calculation for an AT Transaction that reads a single byte from register address 0Ah.

Table A-2. Example of a Read Command

	Byte	Value
0	DLE	FEh
1	STX	05h

	Byte	Value
2	Data 0	0Ah
3	Data 1	01h
4	CRC (low order byte)	A6h
5	CRC (high order byte)	A1h
6	DLE	FEh
7	ETX	40h

Table A-3 provides an example of a CRC calculation for an AT Transaction that writes 5 bytes to register address 62h. Note that Byte 8 is a duplicate symbol inserted to distinguish Byte 9 from a DLE symbol. It is not part of the symbols protected by the CRC and is thus not included in the CRC calculation.

Table A-3. Example of a Write Command

	Byte	Value
0	DLE	FEh
1	STX	05h
2	Data 0	62h
3	Data 1	85h
4	Data 2	43h
5	Data 3	0Ah
6	Data 4	80h
7	Data 5	51h
8	Data 6	FEh
9	Data 7	FEh
10	CRC (low order byte)	27h
11	CRC (high order byte)	88h
12	DLE	FEh
13	ETX	40h

A.4 Gen 2 and Gen 3 Scrambler

Each row in Table A-4 contains the payload of a 64-bit Symbol scrambled by a transmitter into a 64 bit output. The 64-bit input is listed in its order at the Symbol Encoding stage, prior to bit swap. The 64-bit output is listed in the same order as the input.

Table A-4. Examples of Scrambler Computations

Symbol	Seed	Input	Output
Data	17 8225h	1001 1CB6 8000 26F9h	742E 57A6 CFBF FAACH
Data	7F 0A42h	0000 020E 000B 0782h	33A5 96AB 5625 6764h
Data	25 B41Bh	000D 0DCA 000E 05CDh	3ADA 28D9 392D 6F77h
Data	74 9989h	0011 097D 0013 016Fh	FB4B D87E A250 5964h
OS	1F EEDDh	0100 0110 0400 98F2h	CDC6 B616 282A 68F2h
OS	70 A001h	0100 0110 0400 98F2h	AA11 4439 2C23 3CF2h
OS	27 8D0Dh	0100 0110 0400 98F2h	9B7B 542E 1ED7 88F2h
OS	23 E363h	0100 0110 0400 98F2h	CB81 DDDE 8CA3 58F2h

A.5 Logical Layer RS-FEC**A.5.1 Gen 2 and Gen 3 RS-FEC Examples**

The following examples contain an RS-FEC block as it appears on the wire. Each table entry represents a byte in decimal format. Serial byte 0 is the first to be sent, and serial byte 197 is the last. Within each byte, the most significant bit is sent first. The examples were generated with scrambling disabled.

- Example 1 (Table A-5) – a sequence of 192 bytes with increasing values {1 (oldest), 2, ..., 192 (newest)}, followed by 2 bytes of Sync Bits with value 0333h (indicating these are all data bytes), followed by 4 bytes of redundancy bits.
- Example 2 (Table A-6) – a sequence of 191 null bytes (value = 0), followed by a single byte of value 1, followed by 2 bytes of Sync Bits with value 0333h (indicating these are all data bytes), followed by 4 bytes of redundancy bits.
- Example 3 (Table A-7) – a sequence of 192 bytes of data with decreasing values {192 (oldest), 191, ..., 1 (newest)}, with the 7th 16-byte Symbol payload replaced by a SKIP Ordered Set. These are followed by 2 bytes of Sync Bits, followed by 4 bytes of redundancy bits.
- Example 4 (Table A-8) – a sequence of Idle Packets in the first 192 bytes, followed by 2 bytes of Sync Bits with value 0333h (indicating these are all data bytes), followed by 4 bytes of redundancy bits.

Table A-5. Example 1 – RS-FEC Block (Gen 2/Gen 3)

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
0	1	1	2	2	3	3	4
4	5	5	6	6	7	7	8
8	9	9	10	10	11	11	12
12	13	13	14	14	15	15	16
16	17	17	18	18	19	19	20
20	21	21	22	22	23	23	24
24	25	25	26	26	27	27	28
28	29	29	30	30	31	31	32
32	33	33	34	34	35	35	36
36	37	37	38	38	39	39	40
40	41	41	42	42	43	43	44
44	45	45	46	46	47	47	48
48	49	49	50	50	51	51	52
52	53	53	54	54	55	55	56
56	57	57	58	58	59	59	60
60	61	61	62	62	63	63	64
64	65	65	66	66	67	67	68
68	69	69	70	70	71	71	72
72	73	73	74	74	75	75	76
76	77	77	78	78	79	79	80
80	81	81	82	82	83	83	84
84	85	85	86	86	87	87	88
88	89	89	90	90	91	91	92

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
92	93	93	94	94	95	95	96
96	97	97	98	98	99	99	100
100	101	101	102	102	103	103	104
104	105	105	106	106	107	107	108
108	109	109	110	110	111	111	112
112	113	113	114	114	115	115	116
116	117	117	118	118	119	119	120
120	121	121	122	122	123	123	124
124	125	125	126	126	127	127	128
128	129	129	130	130	131	131	132
132	133	133	134	134	135	135	136
136	137	137	138	138	139	139	140
140	141	141	142	142	143	143	144
144	145	145	146	146	147	147	148
148	149	149	150	150	151	151	152
152	153	153	154	154	155	155	156
156	157	157	158	158	159	159	160
160	161	161	162	162	163	163	164
164	165	165	166	166	167	167	168
168	169	169	170	170	171	171	172
172	173	173	174	174	175	175	176
176	177	177	178	178	179	179	180
180	181	181	182	182	183	183	184
184	185	185	186	186	187	187	188
188	189	189	190	190	191	191	192
192	03	193	51	194	196	195	215
196	142	197	109				

Table A-6. Example 2 – RS-FEC Block (Gen 2/Gen 3)

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
0	0	1	0	2	0	3	0
4	0	5	0	6	0	7	0
8	0	9	0	10	0	11	0
12	0	13	0	14	0	15	0
16	0	17	0	18	0	19	0
20	0	21	0	22	0	23	0
24	0	25	0	26	0	27	0
28	0	29	0	30	0	31	0
32	0	33	0	34	0	35	0
36	0	37	0	38	0	39	0
40	0	41	0	42	0	43	0
44	0	45	0	46	0	47	0

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
48	0	49	0	50	0	51	0
52	0	53	0	54	0	55	0
56	0	57	0	58	0	59	0
60	0	61	0	62	0	63	0
64	0	65	0	66	0	67	0
68	0	69	0	70	0	71	0
72	0	73	0	74	0	75	0
76	0	77	0	78	0	79	0
80	0	81	0	82	0	83	0
84	0	85	0	86	0	87	0
88	0	89	0	90	0	91	0
92	0	93	0	94	0	95	0
96	0	97	0	98	0	99	0
100	0	101	0	102	0	103	0
104	0	105	0	106	0	107	0
108	0	109	0	110	0	111	0
112	0	113	0	114	0	115	0
116	0	117	0	118	0	119	0
120	0	121	0	122	0	123	0
124	0	125	0	126	0	127	0
128	0	129	0	130	0	131	0
132	0	133	0	134	0	135	0
136	0	137	0	138	0	139	0
140	0	141	0	142	0	143	0
144	0	145	0	146	0	147	0
148	0	149	0	150	0	151	0
152	0	153	0	154	0	155	0
156	0	157	0	158	0	159	0
160	0	161	0	162	0	163	0
164	0	165	0	166	0	167	0
168	0	169	0	170	0	171	0
172	0	173	0	174	0	175	0
176	0	177	0	178	0	179	0
180	0	181	0	182	0	183	0
184	0	185	0	186	0	187	0
188	0	189	0	190	0	191	1
192	03	193	51	194	229	195	109
196	52	197	141				

Table A-7. Example 3 – RS-FEC Block (Gen 2/Gen 3)

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
0	192	1	191	2	190	3	189
4	188	5	187	6	186	7	185
8	184	9	183	10	182	11	181
12	180	13	179	14	178	15	177
16	176	17	175	18	174	19	173
20	172	21	171	22	170	23	169
24	168	25	167	26	166	27	165
28	164	29	163	30	162	31	161
32	160	33	159	34	158	35	157
36	156	37	155	38	154	39	153
40	152	41	151	42	150	43	149
44	148	45	147	46	146	47	145
48	144	49	143	50	142	51	141
52	140	53	139	54	138	55	137
56	136	57	135	58	134	59	133
60	132	61	131	62	130	63	129
64	128	65	127	66	126	67	125
68	124	69	123	70	122	71	121
72	120	73	119	74	118	75	117
76	116	77	115	78	114	79	113
80	112	81	111	82	110	83	109
84	108	85	107	86	106	87	105
88	104	89	103	90	102	91	101
92	100	93	99	94	98	95	97
96	212	97	212	98	212	99	212
100	212	101	212	102	206	103	176
104	212	105	212	106	212	107	212
108	212	109	212	110	206	111	176
112	80	113	79	114	78	115	77
116	76	117	75	118	74	119	73
120	72	121	71	122	70	123	69
124	68	125	67	126	66	127	65
128	64	129	63	130	62	131	61
132	60	133	59	134	58	135	57
136	56	137	55	138	54	139	53
140	52	141	51	142	50	143	49
144	48	145	47	146	46	147	45
148	44	149	43	150	42	151	41
152	40	153	39	154	38	155	37
156	36	157	35	158	34	159	33
160	32	161	31	162	30	163	29

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
164	28	165	27	166	26	167	25
168	24	169	23	170	22	171	21
172	20	173	19	174	18	175	17
176	16	177	15	178	14	179	13
180	12	181	11	182	10	183	9
184	8	185	7	186	6	187	5
188	4	189	3	190	2	191	1
192	03	193	115	194	25	195	38
196	17	197	174				

Table A-8. Example 4 – RS-FEC Block (Gen 2/Gen 3)

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
0	16	1	128	2	0	3	136
4	16	5	128	6	0	7	136
8	16	9	128	10	0	11	136
12	16	13	128	14	0	15	136
16	16	17	128	18	0	19	136
20	16	21	128	22	0	23	136
24	16	25	128	26	0	27	136
28	16	29	128	30	0	31	136
32	16	33	128	34	0	35	136
36	16	37	128	38	0	39	136
40	16	41	128	42	0	43	136
44	16	45	128	46	0	47	136
48	16	49	128	50	0	51	136
52	16	53	128	54	0	55	136
56	16	57	128	58	0	59	136
60	16	61	128	62	0	63	136
64	16	65	128	66	0	67	136
68	16	69	128	70	0	71	136
72	16	73	128	74	0	75	136
76	16	77	128	78	0	79	136
80	16	81	128	82	0	83	136
84	16	85	128	86	0	87	136
88	16	89	128	90	0	91	136
92	16	93	128	94	0	95	136
96	16	97	128	98	0	99	136
100	16	101	128	102	0	103	136
104	16	105	128	106	0	107	136
108	16	109	128	110	0	111	136
112	16	113	128	114	0	115	136
116	16	117	128	118	0	119	136

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
120	16	121	128	122	0	123	136
124	16	125	128	126	0	127	136
128	16	129	128	130	0	131	136
132	16	133	128	134	0	135	136
136	16	137	128	138	0	139	136
140	16	141	128	142	0	143	136
144	16	145	128	146	0	147	136
148	16	149	128	150	0	151	136
152	16	153	128	154	0	155	136
156	16	157	128	158	0	159	136
160	16	161	128	162	0	163	136
164	16	165	128	166	0	167	136
168	16	169	128	170	0	171	136
172	16	173	128	174	0	175	136
176	16	177	128	178	0	179	136
180	16	181	128	182	0	183	136
184	16	185	128	186	0	187	136
188	16	189	128	190	0	191	136
192	03	193	51	194	162	195	243
196	190	197	223				

A.5.2 Gen 4 RS-FEC Examples

The following examples contain an RS-FEC block. Each table entry represents a Binary Symbol in decimal format. Serial Symbol 0 is the first to be sent and serial byte 479 is the last. Within each Symbol, the most significant bit is sent first. The examples were generated with scrambling disabled.

- Example 1 (Table A-9) – a sequence of Binary 480 Symbols with increasing values {1 (oldest), 2, ..., 479 (newest)}, followed by 24 Binary Redundancy Symbols.
- Example 2 (Table A-10) – a sequence of 479 null Binary Symbols (value = 0), followed by a single Binary Symbol of value 1, followed by 24 Binary Redundancy Symbols.
- Example 3 (Table A-11) – a sequence of 480 Binary Symbols of data with decreasing values {480 (oldest), 479, ..., 1 (newest)}, followed by 24 Binary Redundancy Symbols.
- Example 4 (Table A-12) – a sequence of Idle Packets in the first 480 Binary Symbols, followed by 24 Binary Redundancy Symbols.

Table A-9. Example 1 – RS-FEC Block (Gen 4)

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
0	1	1	2	2	3	3	4
4	5	5	6	6	7	7	8
476	477	477	478	478	479	479	480
480	1249	481	471	482	1276	483	1640
484	414	485	438	486	1175	487	11

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
488	65	489	1841	490	464	491	909
492	1279	493	1493	494	1472	495	2028
496	1322	497	597	498	1727	499	1933
500	993	501	963	502	47	503	669

Table A-10. Example 2 – RS-FEC Block (Gen 4)

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
0	0	1	0	2	0	3	0
4	0	5	0	6	0	7	0
476	0	477	0	478	0	479	1
480	1984	481	701	482	1575	483	1495
484	996	485	1879	486	1362	487	979
488	1524	489	640	490	897	491	645
492	1812	493	1605	494	1096	495	1173
496	173	497	1891	498	286	499	1498
500	457	501	1788	502	722	503	1455

Table A-11. Example 3 – RS-FEC Block (Gen 4)

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
0	480	1	479	2	478	3	477
4	476	5	475	6	474	7	473
476	4	477	3	478	2	479	1
480	1775	481	937	482	1100	483	1612
484	291	485	394	486	828	487	952
488	774	489	1191	490	88	491	1114
492	1055	493	180	494	1249	495	987
496	1168	497	1009	498	1862	499	1218
500	1114	501	687	502	90	503	1267

Table A-12. Example 4 – RS-FEC Block (Gen 4)

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
0	64	1	64	2	34	3	128
4	128	5	68	6	256	7	256
476	8	477	1056	478	32	479	17
480	1876	481	819	482	1638	483	239
484	151	485	749	486	962	487	134
488	1334	489	453	490	1070	491	1112
492	981	493	895	494	649	495	1936

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
496	717	497	1145	498	1141	499	776
500	1746	501	585	502	1626	503	494

A.6 USB3 Tunneling CRC

Figure A-2 provides examples of CRC calculations for USB3 Tunneled Packets containing LFPS and Ordered Sets.

Figure A-2. Examples of USB3 Tunneling Calculations

31		24				16				8				0	
CRC		R	LBPM En	W R	U3 Wa	U2 Ex	S C D 2	S C D 1	RX T En	LBPM				Rsvd	
0x22		0x11							0x0				0x0		

Example 1 – USB LFPS Tunnel payload (U3 Wake = 1 ; Rx Term En = 1)

31		24		16							8		0
CRC		R	LBPM En	W R	U3 Wa	U2 Ex	S C D 2	S C D 1	RX T En	LBPM		Rsvd	
0xC1		0x41							0x04		0x0		

Example 2 – USB LFPS Tunnel payload (LBPM En = 1 ; Rx Term En = 1 ; LBPM PHY_CAP_10G = 1)

31241680						
CRC	Rsvd	Link Functionality	Rsvd	S D S	T S 2	T S 1
0x83	0x0	0x0	0x2			

Example 3 – USB Ordered Set Tunnel payload (TS2 = 1)

31		24		16		8		0		
CRC		Rsvd		Link Functionality		Rsvd		S D S	T S 2	T S 1
0xFE		0x0		0x0		0x4				

Example 4 – USB Ordered Set Tunnel payload (SDS = 1)

A.7 Host Interface Frame CRC

This section provides an example of CRC calculation for a Host Interface Frame. The Frame payload contains 553 bytes, listed in DW order as delivered to the Transport Layer. Each DW is represented as 4 bytes, each in hexadecimal notation, with bits [31:24] at the left and bits [7:0] at the right.

a6	25	07	03
f3	05	82	49
be	34	db	0d
21	87	2f	14
2f	51	4b	48
56	b8	9a	81

8b	eb	51	a4
a1	bf	bb	73
1d	5f	49	7f
df	77	c2	3a
7e	9b	55	a3
d8	b3	ae	70
fa	ae	92	2e
77	fd	0b	0e
45	04	ef	95
26	08	1e	ef
4b	0c	5b	09
9e	6b	5a	1c
31	57	f8	6b
53	08	6c	94
1e	ab	35	0f
8b	34	70	55
94	7c	de	76
82	d4	8d	67
1c	69	b5	2b
0d	6c	10	2c
a7	09	f0	80
0d	02	91	1f
c5	f6	0e	3e
dd	ed	44	36
78	2c	a7	b9
6a	3f	8a	8d
49	9f	41	83
8e	82	d1	30
af	be	24	bb
dc	53	19	e4
fe	a1	22	91
50	a0	b7	af
8c	a7	43	89
5b	d0	f4	c7
62	44	10	fb
6f	a4	20	04
84	a3	b7	8a
37	44	40	fb
8b	8c	71	99
a4	6d	e8	18
aa	39	42	71
a0	c9	a8	c8
02	31	38	1d
54	7c	29	9e
64	ff	da	9b
a4	df	64	a4
6d	4e	38	d0
af	04	c6	c1
a0	bf	5f	75
e2	7f	44	c5
af	fd	3f	5b
f8	37	b7	44
8f	58	28	17
62	b8	ab	a4
75	7d	fe	b9
10	16	bc	20
ff	9a	79	d5
e7	2e	5c	d4
b9	f5	09	ee

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ab	0e	e2	c4
b0	af	83	7b
73	b0	f2	ca
2b	90	2d	22
8c	e1	bd	3d
12	b6	00	ee
84	21	57	c0
ff	e4	47	68
8f	f1	00	1a
7d	69	8d	9f
91	13	1f	14
0f	cc	53	8e
15	04	81	07
dc	12	38	7b
02	9d	af	c1
a9	d6	66	24
5a	bd	3c	eb
02	eb	ff	b8
d3	2e	0d	48
7b	e2	39	a5
d0	a8	89	0e
80	23	a6	b4
c2	47	a1	97
52	15	75	33
aa	7d	e7	31
d9	41	b6	ca
b6	ab	d9	d1
a3	af	7a	8e
6b	97	21	b4
7f	36	e9	4d
3f	42	bb	09
94	b3	58	19
7e	d6	89	39
45	dc	06	9c
22	f7	07	ee
6b	8a	a6	f9
93	8b	fa	b4
c7	51	85	55
b8	15	7c	d2
2c	93	3b	61
61	74	37	2c
33	d0	0f	d0
c9	83	c3	ac
b0	cb	f2	4a
2a	4f	42	d3
af	3e	7f	99
f4	89	62	c9
44	e4	85	07
98	aa	af	ec
ea	cc	d4	b8
cd	d8	ff	4f
c7	cf	1c	99
d9	07	b1	18
92	2b	da	b7
ef	fd	2d	54
7e	7c	1e	ee
c6	96	0c	a8
4f	cf	97	ef
15	23	16	66

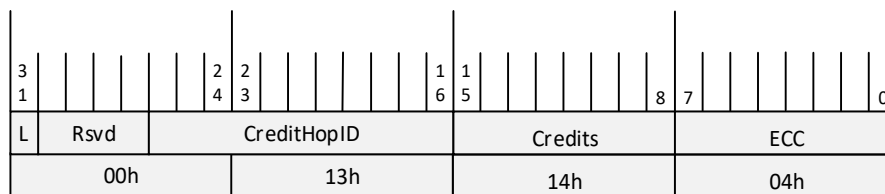
64	9f	9f	01
97	73	09	79
2a	e8	68	66
f0	69	77	cf
4d	6f	8a	18
b4	c9	2d	f1
db	fd	ef	94
ae	d6	27	6f
a3	b2	04	e7
e2	16	af	6b
28	8a	e9	58
a3	6f	8a	33
5d	26	1a	87
51	93	53	4c
1c			

The 32-bits added to the Frame are {45 3e b6 ba} with the same notation as above. The first byte (45h) follows the last payload byte (1ch).

A.8 ECC Examples

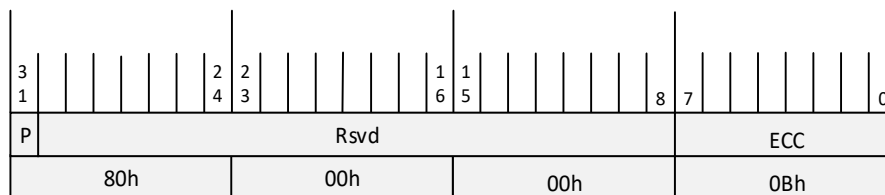
This section shows examples of Transport Layer Packets with *ECC* fields.

Figure A-3. Example of a Credit Grant Record



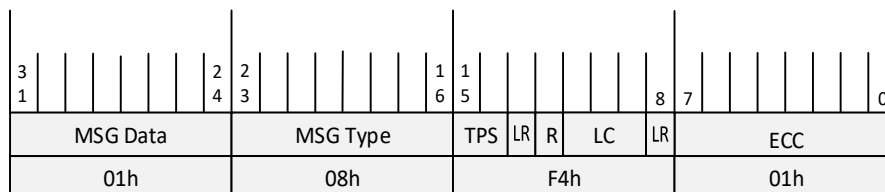
Example of a Credit Grant Record

Figure A-4. Example of an HPD Packet Payload



Example of an HPD Packet Payload

Figure A-5. Example of a SET_CONFIG Packet Payload



Example of a SET_CONFIG Packet Payload

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0120210 1222010 0112111 1001201 2120002 1121210 0211202 0022021 2102002 1112122
1102200 2220000 1121212 0110220 22

PRTS19 – seed 1111111111111111111t

1111111 1111111 1111100 2211002 2110022 1101021 1010211 0102110 1210020 1022120
2110122 1210121 0220211 0122011 01

PRTS19 – seed 1210120212021012101t

1210120 2120210 1210122 1200012 2201001 2112210 1012200 0202201 2201000 2101011
1222102 0101022 2120122 0020002 01

B Summary of Transport Layer Packets

Table B-1 summarizes the values of the header fields for each Transport Layer Packet type. It is included for informative purposes only. Normative requirements regarding specific packet types can be found in the referenced subsections.

Table B-1. Transport Layer Packet Summary

Usage	HopID	PDF	SupplD	Length	Payload
Protocol Adapter Layer Packets					
Tunneled Packet	Target HopID	determined by Protocol Adapter Layer	0b	Varies	Protocol Adapter Layer data
PM Packet	Target HopID	Eh	0b	4	See Section 5.1.3.1.1
Control Packets					
Read Request	00h	1h	0b	16	See Section 6.4.2.3
Read Response	00h	1h	0b	Varies	See Section 6.4.2.4
Write Request	00h	2h	0b	Varies	See Section 6.4.2.5
Write Response	00h	2h	0b	16	See Section 6.4.2.6
Notification Packet	00h	3h	0b	16	See Section 6.4.2.7
Notification Acknowledgment Packet	00h	4h	0b	12	See Section 6.4.2.8
Hot Plug Event Packet	00h	5h	0b	16	See Section 6.4.2.9
Inter-Domain Request	00h	6h	0b	Varies	See Section 6.4.2.11
Inter-Domain Response	00h	7h	0b	Varies	See Section 6.4.2.12
Enhanced Notification Acknowledgment Packet	00h	8h	0b	16	See Section 6.4.2.9
Link Management Packets					
Idle Packet	01h	0h	1b	0	See Section 5.1.3.3.1
Credit Grant Packet	01h	1h	0b	Varies	See Section 5.1.3.3.2
Path Credit Sync Packet	Target HopID (Not 01h)	0h	1b	4	See Section 5.1.3.3.3
Shared Buffers Credit Sync Packet	01h	2h	0b	4	See Section 5.1.3.3.4
Time Sync Packets					
Follow-Up Packet	03h	1h	0b	60	See Section 7.3.3.2
Inter-Domain Time Stamp Packet	03h	2h	0b	28	See Section 7.3.3.3

C Examples of Link Power Management Flows**C.1 Gen 2 and Gen 3 Flows****C.1.1 Entry to Low Power States**

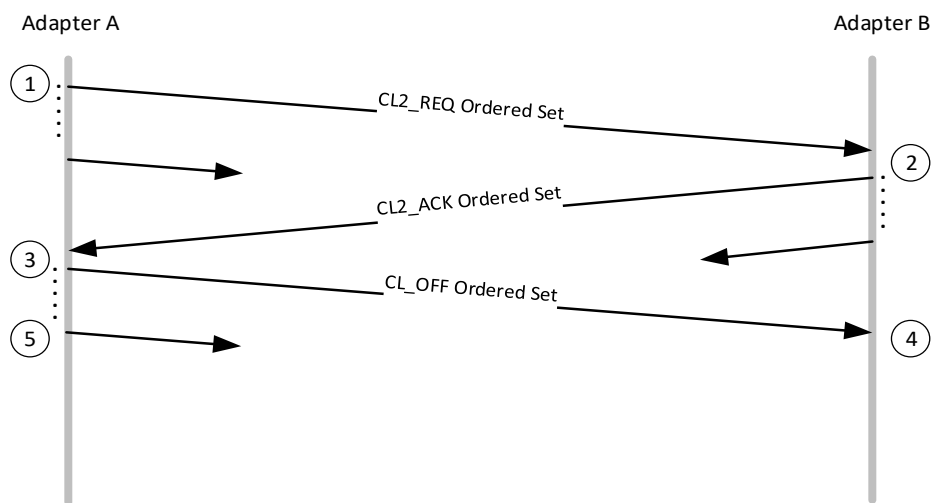
This appendix contains examples of entry to CL2, CL1, or CL0s states.

Note: Re-timers take a passive role in entry flows – they track the flow but do not affect it. They are therefore omitted from the examples in this section.

C.1.1.1 Successful Entry to CL2 State

Figure C-1 shows an example of how the Adapters on a Link transition into the CL2 state. In the example, Adapter A initiates the entry to CL2 state. Adapter B does not have any objections asserted.

Figure C-1. Successful Entry to CL2 State

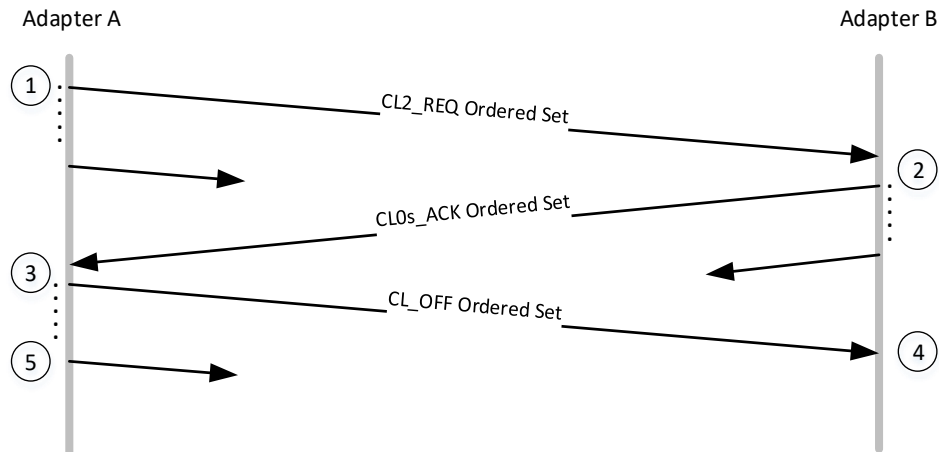


The following steps take place in Figure C-1:

1. Adapter A starts sending CL2_REQ Ordered Sets to Adapter B to initiate a transition to CL2 state.
2. Adapter B receives a CL2_REQ Ordered Set, then starts sending CL2_ACK Ordered Sets to Adapter A to indicate its ability to enter CL2 state.
3. Adapter A receives a CL2_ACK Ordered Set. It then shuts down its receiver and starts sending CL_OFF Ordered Sets to Adapter B.
4. Adapter B receives a CL_OFF Ordered Set. It then shuts down its receiver. After transmitting 375 CL2_ACK Ordered Sets, it shuts down its transmitter.
5. After Adapter A sends 375 CL_OFF Ordered Sets, it shuts down its transmitter within t_{TxOff} time.

C.1.1.2 Successful Entry to CL0s State

Figure C-2 shows an example of how the Adapters on a Link transition to the CL0s state. In the example, Adapter A initiates the entry to CL0s state. Adapter B rejects entry to CL2 and CL1 states because it has CL2 and CL1 objections asserted. CL0s is enabled in Adapter B (*CL0s Enable* bit is 1b).

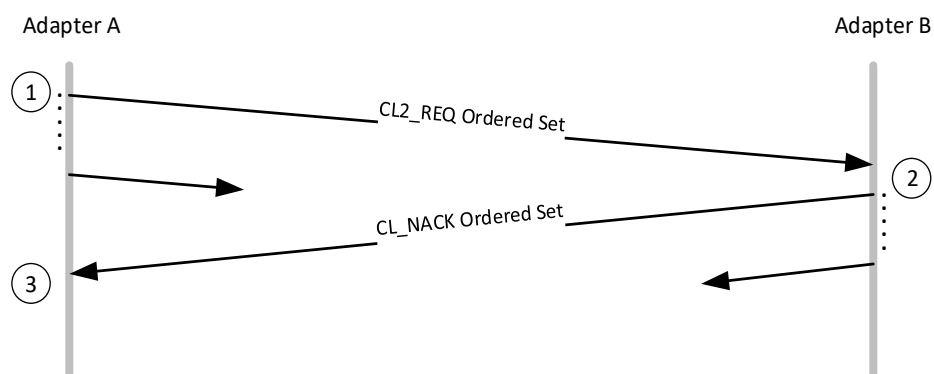
Figure C-2. Successful Entry to CL0s State

The following steps take place in Figure C-2:

1. Adapter A starts sending CL2_REQ Ordered Sets to Adapter B to initiate a transition to CL2 state.
2. Adapter B receives a CL2_REQ Ordered Set, then starts sending CL0s_ACK Ordered Sets to Adapter A to indicate its ability to enter CL0s state.
3. Adapter A receives a CL0s_ACK Ordered Set. It starts sending CL_OFF Ordered Sets to Adapter B.
4. Adapter B receives a CL_OFF Ordered Set. It then shuts down its receiver.
5. After Adapter A sends 375 CL_OFF Ordered Sets, it shuts down its transmitter within t_{TxOff} time.

C.1.1.3 Rejection to Enter CL2 State

Figure C-3 shows an example where the Adapters fail to enter to a Low Power state. In the example, Adapter A initiates entry to CL2 state. Adapter B rejects entry to CL2 and CL1 states because it has CL2 and CL1 objections asserted. CL0s is not enabled in Adapter B (*CL0s Enable* bit is 0b).

Figure C-3. Failure to Enter CL2 State

The following steps take place in Figure C-3:

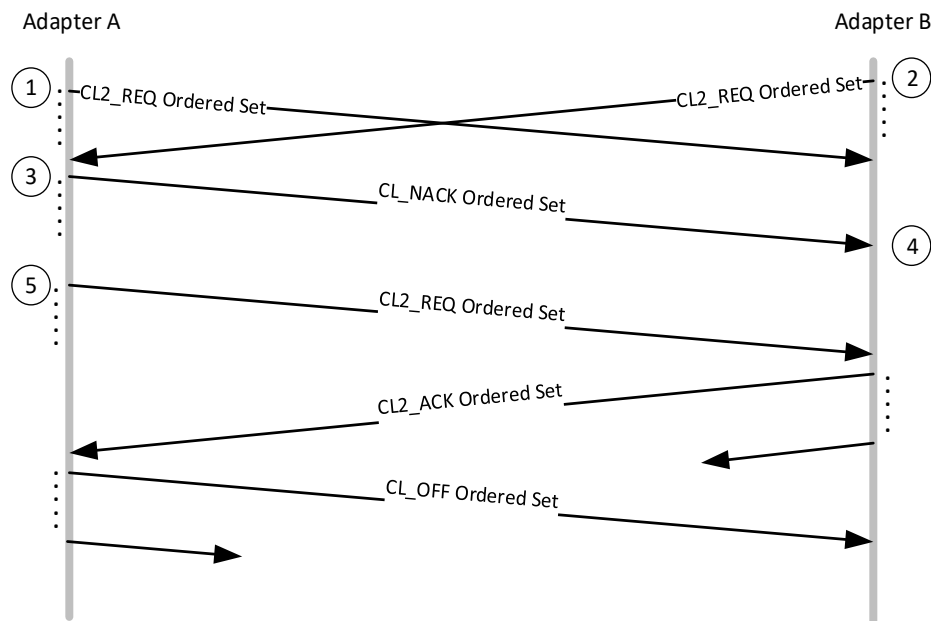
1. Adapter A starts sending CL2_REQ Ordered Sets to Adapter B to initiate a transition to CL2 state.

2. Adapter B receives a CL2_REQ Ordered Set, then starts sending CL_NACK Ordered Sets to Adapter A to indicate its objection to enter Low Power state.
3. Adapter A receives a CL_NACK Ordered Set. It then stops sending CL2_REQ Ordered Sets and resumes CL0 operation.

C.1.1.4 Concurrent Requests to Enter Low Power State

Figure C-4 shows an example where both Adapters on a Link attempt to transition to CL2 state at the same time. In the example, Adapter A has the *PM Secondary* bit set to 0b and Adapter B has the *PM Secondary* bit set to 1b.

Figure C-4. Concurrent Requests to Enter CL2 State

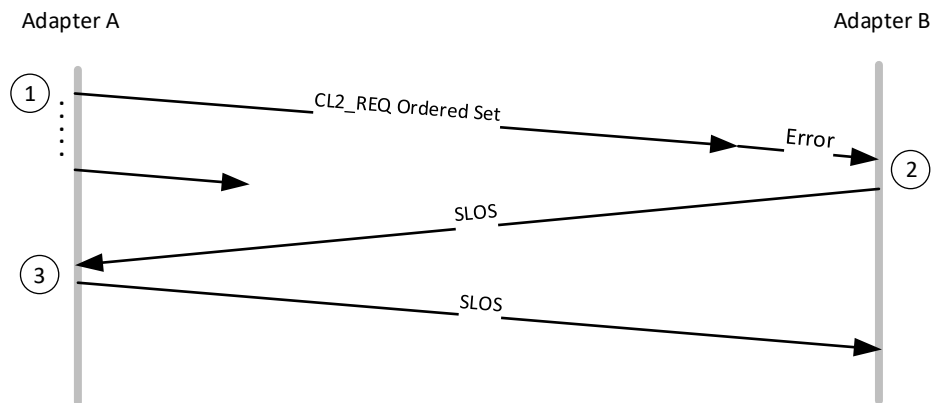


The following steps take place in Figure C-4:

1. Adapter A starts sending CL2_REQ Ordered Sets to Adapter B to initiate a transition to CL2 state.
2. Prior to receiving a CL2_REQ Ordered Set, Adapter B starts sending CL2_REQ Ordered Sets to Adapter A.
3. Adapter A receives a CL2_REQ Ordered Set. It stops sending CL2_REQ Ordered Sets and starts sending CL_NACK Ordered Sets.
4. Adapter B receives a CL_NACK Ordered Set. It then stops sending CL2_REQ Ordered Sets and resumes CL0 operation.
5. After Adapter A stops receiving CL2_REQ Ordered Sets, it stops sending CL_NACK Ordered Sets. It then starts sending CL2_REQ Ordered Sets again and the flow continues as in Section C.1.1.1.

C.1.1.5 CL2_REQ Ordered Sets are Not Received

Figure C-5 shows an example where Adapter A attempts to transition to CL2 state, but Adapter B detects a Link error instead of the CL2_REQ Ordered Set.

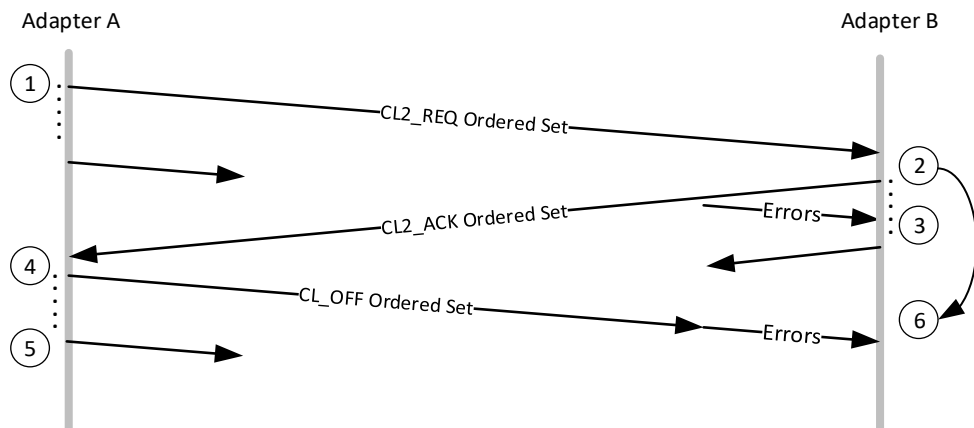
Figure C-5. Error in CL2_REQ Ordered Sets

The following steps take place in Figure C-5:

1. Adapter A starts sending CL2_REQ Ordered Sets to Adapter B to initiate a transition to CL2 state.
2. Adapter B detects a Link error. It then enters Training state and starts transmitting SLOS.
3. Adapter A either detects the Link error or receives an SLOS. It stops sending CL2_REQ Ordered Sets and enters Training state.

C.1.1.6 CL2_REQ Ordered Sets are Partially Received

Figure C-6 shows an example where Adapter A attempts to transition to CL2 state, but a Link error occurs before Adapter B receives all CL2_REQ Ordered Sets required for the transition.

Figure C-6. CL2_REQ Ordered Sets are Partially Received

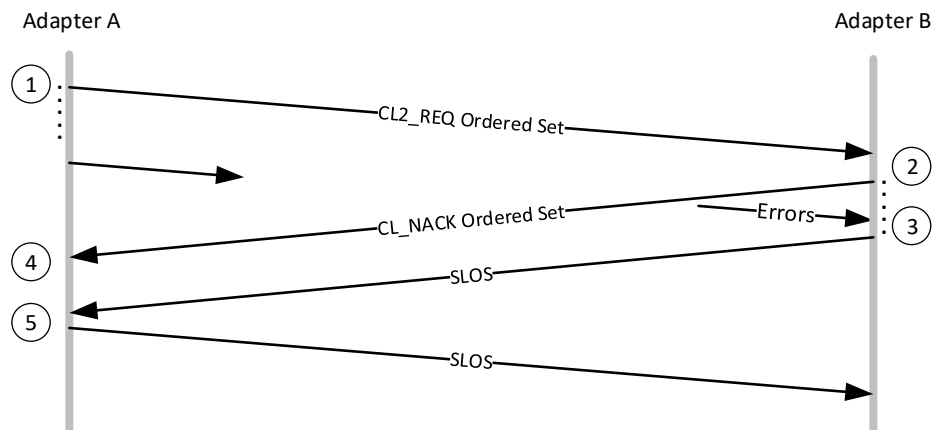
The following steps take place in Figure C-6:

1. Adapter A starts sending CL2_REQ Ordered Sets to Adapter B to initiate a transition to CL2 state.
2. Adapter B receives a CL2_REQ Ordered Set. It starts sending CL2_ACK Ordered Sets to Adapter A, indicating its ability to enter CL2 state.
3. Adapter B detects a Link error on the Lane before 375 copies of the CL2_REQ Ordered Set are received. Adapter B disables RS-FEC on the receive direction to allow detection of SLOS.

4. Adapter A receives a CL2_ACK Ordered Set. It then shuts down its receiver. Adapter A starts sending CL_OFF Ordered Sets to Adapter B.
5. After Adapter A sends 375 CL_OFF Ordered Sets. It shuts down its transmitter within tTxOff time.
6. After Adapter B sends 375 CL2_ACK Ordered Sets, it shuts down its transmitter and receiver.

Figure C-7 shows an example where Adapter A attempts to transition to CL2 state, but a Link error occurs after Adapter B responds with CL_NACK Ordered Sets.

Figure C-7. Errors in CL2_REQ Reception and CL_NACK Response

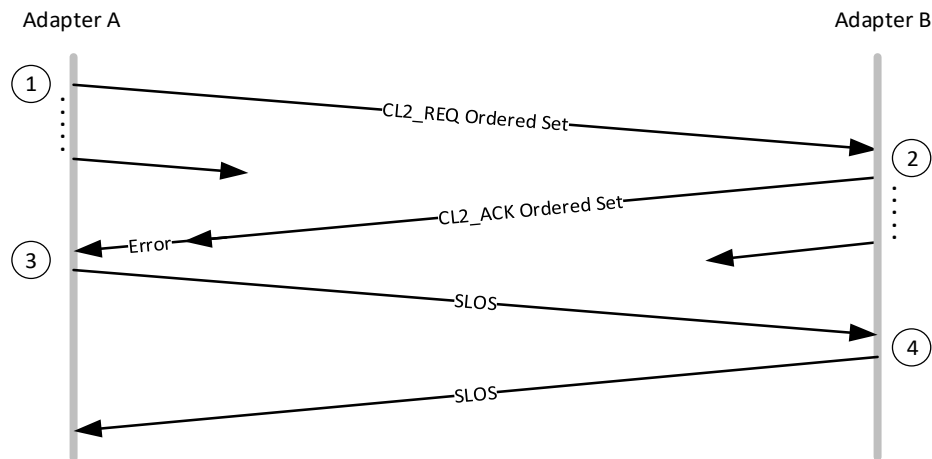


The following steps take place in Figure C-7:

1. Adapter A starts sending CL2_REQ Ordered Sets to Adapter B to initiate a transition to CL2 state.
2. Adapter B receives a CL2_REQ Ordered Set, then starts sending CL_NACK Ordered Sets to Adapter A to indicate its objection to enter Low Power state.
3. Adapter B detects a Link error on the Lane before 375 copies of the CL_NACK Ordered Set have been transmitted. Adapter B transitions the Lane to Training state, then starts sending SLOS.
4. Adapter A receives a CL_NACK Ordered Set. It then stops sending CL2_REQ Ordered Sets and resumes CL0 operation.
5. Adapter A either detects the Link error or receives an SLOS, then enters Training state.

C.1.1.7 Error in CL2_ACK Ordered Sets

Figure C-8 shows an example where Adapter A attempts to transition to CL2 state, but detects a Link error before receiving a CL2_ACK Ordered Set.

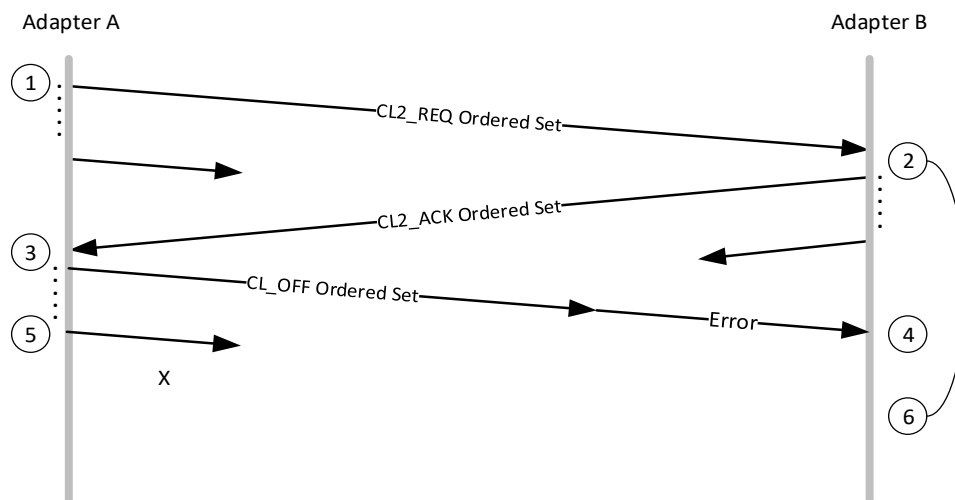
Figure C-8. Error in CL2_ACK Ordered Sets

The following steps take place in Figure C-8:

1. Adapter A starts sending CL2_REQ Ordered Sets to Adapter B to initiate a transition to CL2 state.
2. Adapter B receives a CL2_REQ Ordered Set, then starts sending CL2_ACK Ordered Sets to Adapter A to indicate its ability to enter CL2 state.
3. Adapter A detects a Link error on the Lane before receiving a response to the CL2_REQ Ordered Sets. It transitions the Lane to Training state, then starts sending SLOS.
4. If RS-FEC is on, Adapter B detects Link errors, disables RS-FEC, and then detects SLOS. If RS-FEC is off, Adapter B detects SLOS. After Adapter B detects SLOS, it enters the Training state.

C.1.1.8 Error in CL_OFF Ordered Sets

Figure C-9 shows an example where Adapter A attempts to transition CL2 state, but Adapter B detects a Link error before receiving the CL_OFF Ordered Sets.

Figure C-9. Error in CL_OFF Ordered Sets

The following steps take place in Figure C-9:

1. Adapter A starts sending CL2_REQ Ordered Sets to Adapter B to initiate a transition to CL2 state.
2. Adapter B receives a CL2_REQ Ordered Set. It starts sending CL2_ACK Ordered Sets to Adapter A, indicating its ability to enter CL2 state.
3. Adapter A receives a CL2_ACK Ordered Set. It then shuts down its receiver. Adapter A starts sending CL_OFF Ordered Sets to Adapter B.
4. Adapter B detects a Link error on the Lane before 375 copies of the CL2_ACK Ordered Set are transmitted. Adapter B disables RS-FEC on its receive direction to allow detection of SLOS.
5. After Adapter A sends 375 CL_OFF Ordered Sets, it shuts down its transmitter.
6. After Adapter B sends 375 CL2_ACK Ordered Sets, it shuts down its transmitter and receiver.

C.1.2 Exit from Low Power States

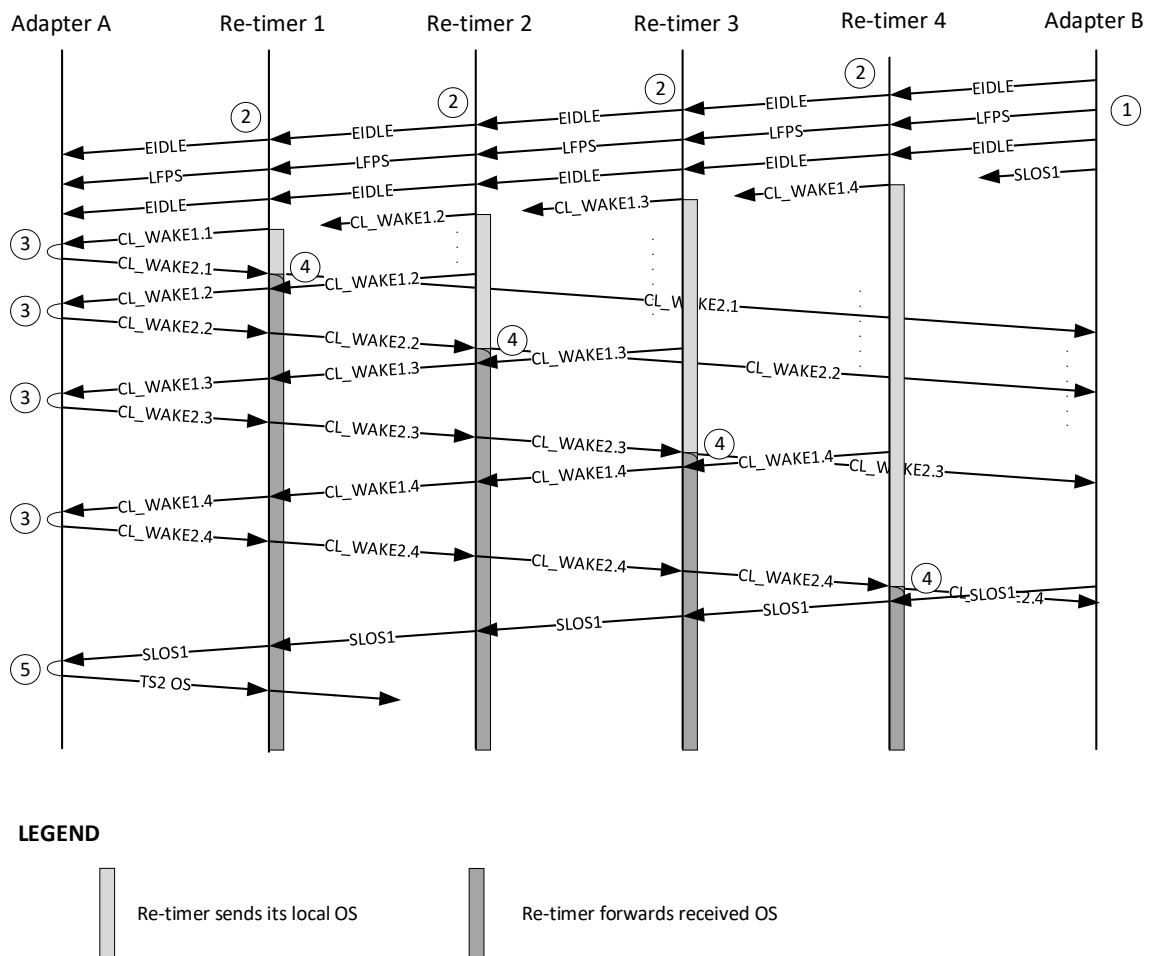
This section contains examples of Adapter behavior during exit from CL2, CL1, or CL0s states.

Note: Re-timers take an active role in exit flows and are therefore shown in the examples in this section.

C.1.2.1 Example: Exit from CL0s State

Figure C-10 shows an example of how the Adapters on a Link exit from CL0s state. In the example, Adapter B initiates the CL0s exit. There are four Re-timers between Adapter A and Adapter B (Re-timer 1 to Re-timer 4).

Note: In the example below, the CL_WAKE2.X Ordered Sets propagate all the way to Router B. Also, Router A continues to send Transport Layer packets to Router B throughout the CL0s exit flow. However, these are omitted in Figure C-10, in order to simplify the figure and maintain readability.

Figure C-10. CL0s Exit

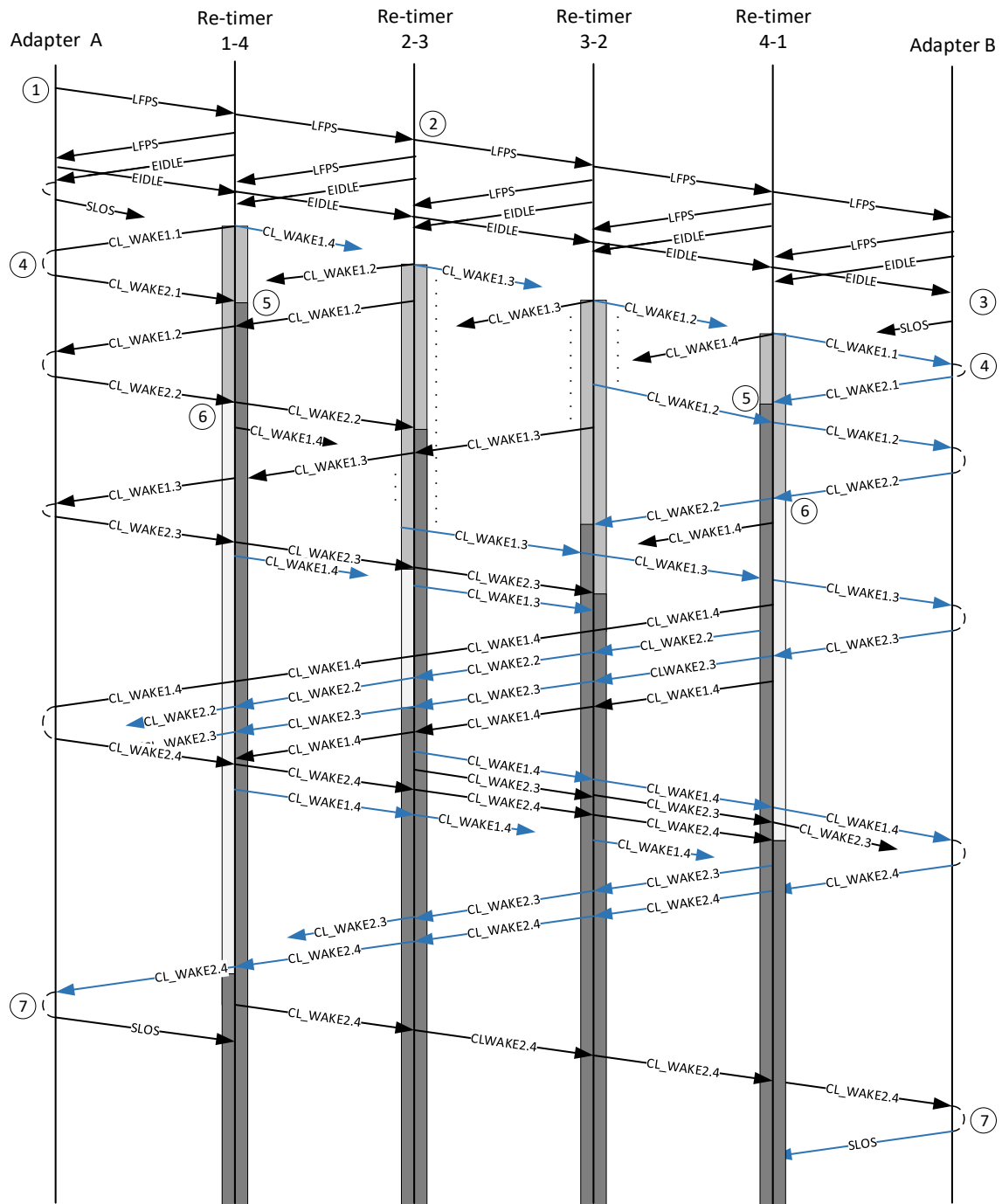
The following steps take place in Figure C-10:

1. Port B initiates exit from CL0s by sending a Low Frequency Periodic Signaling (LFPS) burst on all Lanes of the USB4 Port for the duration of at least 16 LFPS cycles. It then returns to Electrical Idle for tPreData, after which it starts transmitting SLOS1.
2. Upon detecting an LFPS burst on a Lane, each Re-timer sends a Low Frequency Periodic Signaling (LFPS) burst on the Lane for the duration of at least 16 LFPS cycles. It then returns to Electrical Idle for tPreData. The Re-timer then enables the receiver to start calibration, not earlier than tCLxIdleRx after the last LFPS cycle received. The Re-timer also starts transmitting locally-generated CL_WAKE1.X Ordered Set Symbols in the direction of the Lane exiting from CL0s, where X is the Re-timer Index in that direction.
3. On reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, Adapter A transmits at least 8 CL_WAKE2.X Ordered Set Symbols before returning to service other traffic.
4. When a Re-timer with index X detects 3 back-to-back CL_WAKE2.X Ordered Set Symbols, it transitions the Lane in the direction exiting from CL0s to operate on the clock retrieved from the received Symbols rather than on its Local Clock. From this point on, the Re-timer forwards in the direction exiting from CL0s the Symbols it receives from the Lane and stops transmitting its locally-generated CL_WAKE1.X Ordered Set Symbols.
5. On detection of 3 back-to-back SLOS Symbols, Adapter A transmits 16 TS2 Ordered Sets.

C.1.2.2 Example: Exit from CL2 (or CL1) State

Figure C-11 shows an example of CL2 (or CL1) exit that involves 4 Re-timers between the ends of the Link. Adapter A initiates the exit from Low Power state. Each Re-timer has 2 indexes, one in each direction. For example, Re-timer 1-4 uses an index value = 1 when communicating with Adapter A and an index value = 4 when communicating with Re-timer 2-3.

Figure C-11. CL2 (or CL1) Exit



LEGEND

	Re-timer sends its local OS		Re-timer toggles between sending Ordered Set received and sending its local OS		Re-timer forwards received OS
--	-----------------------------	--	--	--	-------------------------------

Notes:

- The bar to the left of a Re-timer indicates its behavior in the direction of Adapter B. The bar to the Right of a Re-timer indicates its behavior in the direction of Adapter A.
- The black arrows show the exit flow of Adapter A. The blue arrows show the exit flow of Adapter B.

The following steps take place in Figure C-11:

1. Port A initiates exit from CL2 (or CL1) state by sending a Low Frequency Periodic Signaling (LFPS) burst on each Lane until the receiver detects an LFPS burst. It then returns to Electrical Idle for tPreData, after which it starts transmitting SLOS1 Ordered Sets.
2. Upon detecting an LFPS burst on a Lane, each Re-timer sends a Low Frequency Periodic Signaling (LFPS) burst in both directions for a duration of at least 5 LFPS cycles. It then returns to Electrical Idle for tPreData. The Re-timer then enables the receiver to start calibration, not earlier than tCLxIdleRx after the last LFPS cycle is received. The Re-timer also starts transmitting CL_WAKE1.X Symbols on the Lane, where X is the index of the Re-timer in the respective direction.
3. Upon detecting an LFPS burst on a Lane, Adapter B sends a Low Frequency Periodic Signaling (LFPS) burst for a duration of at least 5 LFPS cycles. It then returns to Electrical Idle for tPreData. The Router then enables the receiver to start calibration, not earlier than tCLxIdleRx after the last LFPS cycle received. The Router also starts transmitting SLOS1 Ordered Sets on the Lane.
4. Upon reception of 3 back-to-back CL_WAKE1.X Symbols with identical Re-timer Index X, Adapter A and Adapter B each start transmitting CL_WAKE2.X Symbols on the Lane.
 - The Adapters ignore any received CL_WAKE2.X Symbols interleaved with CL_WAKE1.X Symbols when it determines the reception of back-to-back CL_WAKE1.X Symbols.
5. When a Re-timer with the receive side at index X detects 3 back-to-back CL_WAKE2.X Symbols, it transitions the Lane in the opposite direction to operate on the clock retrieved from the received Symbols rather than on its Local Clock. From this point on, the Re-timer forwards the Symbols it receives from the Lane and stops transmitting its locally-generated CL_WAKE1.X Symbols.
 - The Re-timer ignores any received CL_WAKE1.X Symbols interleaved with CL_WAKE2.X Symbols when it determines the reception of back-to-back CL_WAKE2.X Symbols.
6. When a Re-timer detects 3 back-to-back CL_WAKE2.X Symbols, and if the Re-timer is still using its Local Clock to transmit in this direction, the Re-timer starts toggling in this direction between sending the last 2 CL_WAKE2 Symbols received and 2 locally-generated Symbols.
7. When an Adapter detects 7 back-to-back CL_WAKE2.X Symbols, it transitions the Lane to Training state and start transmitting SLOS1.

D Serial Time Link Protocol (STLP)

The Serial Time Link Protocol transmits Host Router Time on a designated single-wire link (called TMU_CLK_OUT). TMU_CLK_OUT can be used for two purposes:

1. To test the Time Sync Protocol as part of silicon compliance testing.
2. To provide a high-precision time source to applications external to the Router. (e.g. for compliance testing or synchronizing multiple audio sampling devices).

The Serial Time Link Protocol also optionally includes a designated input single-wire link (called TMU_CLK_IN) that can receive a stream of Serial Time Link Packets and synchronize the Host Router Clock to the input in a similar manner as over an Inter-Domain Link (see Section 7.3.2).

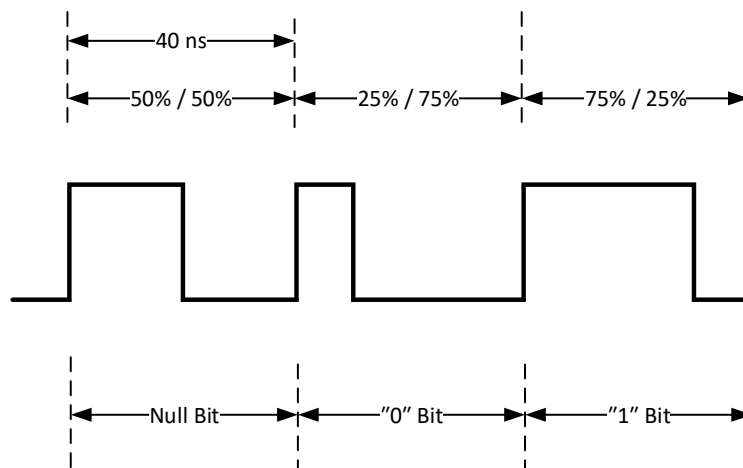
A Router may optionally support the Serial Time Link Protocol. If a Router supports the Serial Time Link Protocol, it shall do so as defined in this section.

D.1 Time Synchronization

A Router shall periodically transmit a Serial Time Link Packet on TMU_CLK_OUT. The period between transmissions is implementation specific, but it is recommended that a Router transmit a Serial Time Link Packet every 16 μ s.

Figure D-1 shows the parameters for the Pulse Width Modulation that shall be used when transmitting on TMU_CLK_OUT.

Figure D-1. Pulse Width Modulation



If TMU_CLK_IN is used for time synchronization, a Router shall use the Inter-Domain equations in Section 7.4.2 to calculate time sync parameters. A Host Router shall use its TMU_CLK_IN input for time synchronization if the *Inter-Domain Enable* bit is 1b, the *IDTR* bit is 0b, and the *IDTI* bit is 0b. Otherwise, a Router shall not use TMU_CLK_IN for time synchronization.



CONNECTION MANAGER NOTE

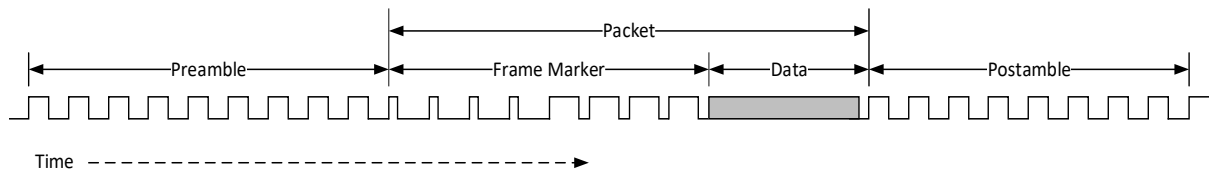
A Connection Manager shall not enable TMU_CLK_IN and Inter-Domain Time Sync at the same time. A Router may want to take precautionary measures to prevent entering a bad state if both are enabled.

D.2 Serial Time Link Packet Format

A Serial Time Link Packet shall begin with preamble that is at least 8 cycles of "NULL" bit and shall end with a postamble that is at least 8 cycles of "NULL" bit.

The Preamble shall be followed by a Frame Marker equal to 0b00001111. This pattern marks the beginning of the packet.

Figure D-2. Serial Time Link Packet Structure



The end of first bit of Frame Marker is the Time Stamp Event later used by the UFP

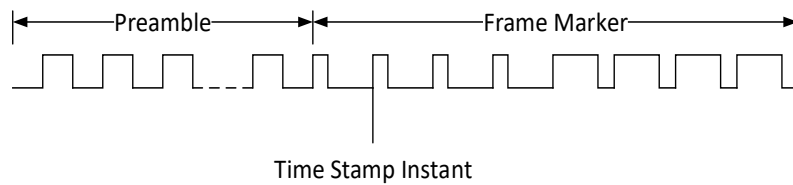


Figure D-3 and Table D-1 define the contents of a Serial Time Link Packet.

A Router shall transmit bit 0 of a Serial Time Link Packet first, followed by subsequent bits in increasing order ending with bit 127.

Figure D-3. Serial Time Link Packet Format

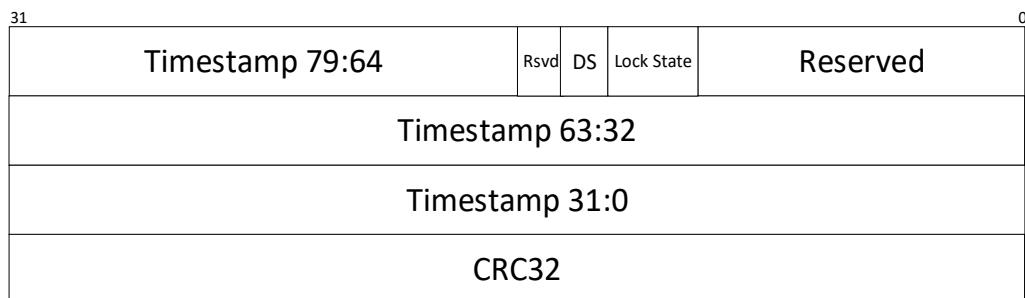
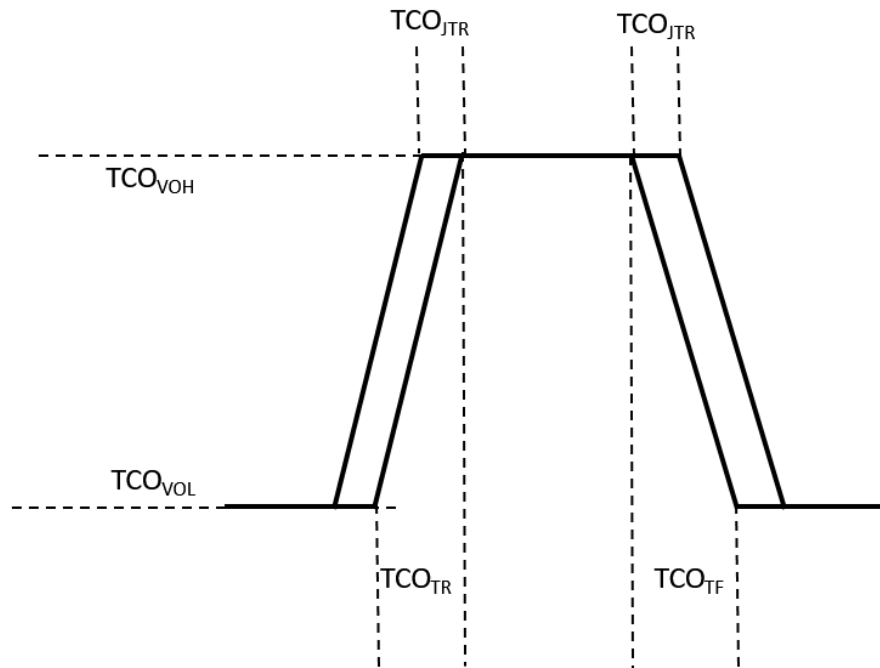
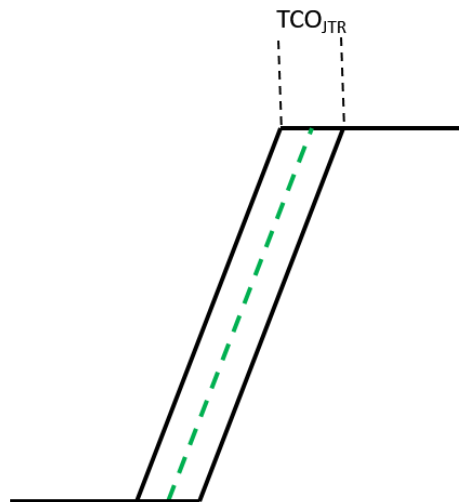


Table D-1. Serial Time Link Packet Fields

DW	Bits	Field	Description
0	11:0	Rsvd	Reserved

DW	Bits	Field	Description
	13:12	Lock State	<p>This field indicates the State of the Router with respect to Host Router Time.</p> <p>Locking means that the Host Router Time is not yet consistent to the accuracy required by this specification and time stamps are not valid.</p> <p>Locked means that Host Router Time is consistent and time stamps are valid.</p> <p>00b – The source is Host Router with no Inter-Domain time sync (<i>Time Stamp</i> field is valid)</p> <p>01b – Locking (<i>Time Stamp</i> field is invalid)</p> <p>10b – Reserved</p> <p>11b – Locked (<i>Time Stamp</i> field is valid)</p> <p><i>Note: When in Locking state, TimeOffsetFromHR changes inconsistently and there is no clear trend for convergence. To calculate consistency, a derivative of the TimeOffsetFromHR shall be computed. TimeOffsetFromHR is expected to grow linearly, so if the growth is not linear, then LOCK is not achieved.</i></p>
0	14	Disruption State (DS)	<p>This field indicates whether there is a Disruption. A disruption occurs when there is a sudden glitch in time continuity.</p> <p>0b – Currently there is no disruption</p> <p>1b – There was a disruption since the last serial packet transmission</p>
	15	Rsvd	Reserved
	31:16	Time Stamp[79:64]	Bits [79:64] of the Time Stamp. The Time Stamp contains the Host Router Time value at the point when the first bit of the frame marker for the packet ends.
1	31:0	Time Stamp[63:32]	Bits [63:32] of the Time Stamp. The Time Stamp contains the Host Router Time value at the point when the first bit of the frame marker for the packet ends.
2	31:0	Time Stamp[31:0]	Bits [31:0] of the Time Stamp. The Time Stamp contains the Host Router Time value at the point when the first bit of the frame marker for the packet ends.
3	31:0	Cyclic Redundancy Check	<p>CRC32 remainder value computed over the entire packet payload. The CRC32 computation in an Inter-Domain Time Stamp Packet shall be based on the following CRC:</p> <ul style="list-style-type: none"> Width: 32 Poly: 1EDC 6F41h Init: FFFF FFFFh RefIn: True RefOut: True XorOut: FFFF FFFFh

Figure D-4. TMU_CLK_OUT and TMU_CLK_IN Parameters**Figure D-5. Definition of TCO_{JTR}** 

The minimum SSC as specified in Section 3.1.3.1.3 shall be present.

D.3 TMU_CLK_OUT and TMU_CLK_IN

Table D-2 contains the electrical specification that a Router shall use for the TMU_CLK_OUT and TMU_CLK_IN signals.

Table D-2. TMU_CLK_OUT and TMU_CLK_IN Specifications

Symbol	Parameter	Min	Max	Units	Conditions
TCO _{VOH}	TMU_CLK_OUT High Voltage	2.2	3.47	Volts	TCO _{IOH} = -600μA (set by 3.4 V/0.5 MΩ). See Note 1.
TCO _{VOL}	TMU_CLK_OUT Low Voltage	-0.2	0.4	Volts	TCO _{IOL} = 600μA (set by 3.4 V/10 KΩ). See Note 1.
TCO _{TR}	TMU_CLK_OUT Rise Time		2.0	ns	10% to 90% Rise time.
TCO _{TF}	TMU_CLK_OUT Fall Time		2.0	ns	90% to 10% Fall time.
TCI _{VIH}	TMU_CLK_IN High Voltage Detection	2.0	3.47	Volts	See Note 2, Note 3.
TCI _{VIL}	TMU_CLK_IN Low Voltage Detection	-0.2	0.5	Volts	See Note 4.
TCI _{IIH}	TMU_CLK_IN High input current		25	μA	Vin = VDD.
TCI _{IIL}	TMU_CLK_IN Low input current		0.4	μA	Vin = 0V.
TCO _{JTR}	TMU_CLK_OUT Jitter	0	2.5	ns	Around ideal signal.
Notes: 1. This parameter shall be verified in both transaction and steady state. The steady state condition shall be measured with a continuous high or low level. The transaction state condition shall be measured when sending TMU_CLK_OUT data. Over/undershoot shall be ignored. 2. A buffer may be used between the connector and the Router to meet these logic levels. When present, this buffer shall meet SBRX _{VIH} and SBRX _{VIL} as defined in Table 3-32. 3. Logical high maps to V _{IH} . 4. Logical low maps to V _{IL} .					

E Ingress Buffer Space

This Appendix contains examples of how a Router implementer can calculate the preferred buffer size in an Ingress Adapter for each Tunneled Protocol. Section E.1 explains the calculation for Protocols that target a specific bandwidth. Section E.2 explains the calculation for DP Main-Link Path.

E.1 Target Bandwidth Buffer Calculation

The formula below can be used to calculate the number of Ingress buffers that are needed to reach a target bandwidth for a specific Tunneled Protocol over a specific USB4 Link speed. The calculation should be repeated for every USB4 Link speed that the Router supports. The Router should implement enough buffer space to accommodate the maximum result.

Number of Ingress Buffers = (Round Trip delay / Packet delay) * (Target Protocol BW / USB4 Link BW)

Packet delay is the transmit time of average sized Packet over the USB4 Link

Round Trip delay is the sum of the following:

1. The transmit time of average sized Packet over the USB4 Link.
2. The transmit time of a Credit Grant Packet over the USB4 Link.
3. The maximum latency of the Re-timers in both directions.
4. Time from Packet reception to Credit Grant Packet transmit.
5. Time from Credit Grant reception to Packet transmit.
6. The time a Packet travel through the cable in both directions.
7. The maximum skew between the 2 Lanes in both directions (if applicable).

The *Round Trip delay* can be calculated as follows:

Round Trip Delay = (AVG_PS / ULS) + (CG size / ULS) + (2 * NoR * Max Re-timer Latency) + (PtoCG) + (CGtoP) + (2 * CD) + (2 * 64)

where:

ULS = USB4 Link Speed

CD = Cable Delay

AVG_PS = Average Packet Size

NoR = Number of Re-timers

PtoCG = Time from Packet reception to Credit Grant Packet transmit

CGtoP = Time from Credit Grant Packet reception to Packet transmit

E.1.1 Example for USB3 Tunneling Ingress Buffer Calculation

The following parameters are assumed for the calculations:

- Target Protocol BW = 8Gbps for Gen 2x1 ; 17Gbps for all other USB4 Links
- CD = 2 Meter Copper * 8 ns/meter
- AVG_PS = 183 Bytes
- NoR = 6
- PtoCG = 400 ns
- CGtoP = 300 ns

Round Trip delay (Gen 2x1) =

$$(183 * 8/10) + (8 * 8/10) + (2 * 6 * 50) + (400) + (300) + (2 * 2 * 8) + (0) = \sim 1485 \text{ ns}$$

Round Trip delay (Gen 2x2) =

$$(183 * 8/20) + (8 * 8/20) + (2 * 6 * 50) + (400) + (300) + (2 * 2 * 8) + (2 * 64) = \sim 1537 \text{ ns}$$

Round Trip delay (Gen 3x1) =

$$(183 * 8/20) + (8 * 8/20) + (2 * 6 * 30) + (400) + (300) + (2 * 2 * 8) + (0) = \sim 1169 \text{ ns}$$

Round Trip delay (40Gbps) =

$$(183 * 8/40) + (8 * 8/40) + (2 * 6 * 30) + (400) + (300) + (2 * 2 * 8) + (2 * 64) = \sim 1259 \text{ ns}$$

The following number of Ingress buffers are needed for each USB4 Link speed, assuming 10% is taken off the USB4 Link bandwidth:

- Number of Buffers (Gen 2x1) = $1485 / (183 * 8/10) * 8/9 = \sim 9$
- Number of Buffers (Gen 2x2) = $1537 / (183 * 8/20) * 17/18 = \sim 19.8$
- Number of Buffers (Gen 3x1) = $1169 / (183 * 8/20) * 17/18 = \sim 15.1$
- Number of Buffers (Gen 3x2) = $1259 / (183 * 8/40) * 17/36 = \sim 16.2$

Therefore, for a Single-Lane Link, the Router needs 16 Ingress buffers to cover the maximum case (15.1), and for an Aggregated Link it needs 20 Ingress buffers to cover the maximum case (19.8).

E.2 Ingress Buffers Calculation for DP Main Path

A DP Main-Link Path operates with the Flow Control Disabled scheme. The amount of buffers at the Ingress Lane Adapter is calculated to accommodate a temporary state where the DP Main-Link Path Packets are not drained immediately. The possible causes for delaying a DP Main-Link Packet are:

- Lower priority Tunneled Packet which started before the DP Main packet has arrived
- Control Packet
- A DP Main-Link Path Packet that arrives from another Adapter
- Credit Grant Packet
- Credit Sync Packet
- Time Sync Packet
- 16 Symbols for Enter or Exit CL0s

In Addition to the above buffers, a Router implementer needs to consider any internal delay from DP Main-Link Path Packet reception to DP Main-Link Path Packet dequeue from the Ingress Lane Adapter.

F Gen 4 Datapath**F.1 Gen 4 Ordered Sets**

Table F-1 contains the Hexadecimal and Ternary values for the Gen 4 Ordered Sets.

Table F-1. Hexadecimal and Ternary values for Gen 4 Ordered Sets

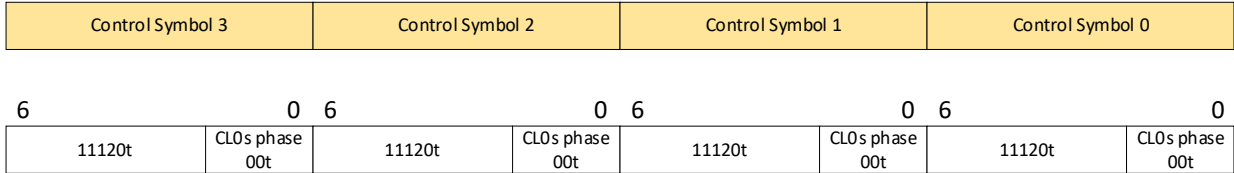
Control Symbol	Ternary	Binary (Hexadecimal)
DESKEW.0	1110000t	0x4C0
DESKEW.1	1110001t	0x4C1
DESKEW.2	1110002t	0x4C2
DESKEW.3	1110010t	0x4C3
DESKEW.4	1110011t	0x698
DESKEW.5	1110012t	0x4C4
DESKEW.6	1110020t	0x4C5
DESKEW.7	1110021t	0x4C6
DESKEW.8	1110022t	0x4C7
DESKEW.9	1110100t	0x4C8
DESKEW.10	1110101t	0x4C9
DESKEW.11	1110102t	0x4CA
DESKEW.12	1110110t	0x4CB
DESKEW.13	1110111t	0x699
DESKEW.14	1110112t	0x4CC
DESKEW.15	1110120t	0x4CD
DESKEW.16	1110121t	0x4CE
DESKEW.17	1110122t	0x4CF
TSNOS	1110211t	0x69A
IGNORE	1110212t	0x4D4
UBOND	1110220t	0x4D5
CL0s_EXIT.AckLFPS	1112000t	0x4E8
CL0s_EXIT.StartP3	1112001t	0x4E9
CL0s_EXIT.StartClkSw	1112002t	0x4EA
CL0s_EXIT.ClkSwAck	1112010t	0x4EB
CL_OFF.CL1.0	1112100t	0x4F0
CL_OFF.CL1.1	1112101t	0x4F1
CL_OFF.CL1.2	1112102t	0x4F2
CL_OFF.CL1.3	1112110t	0x4F3
CL_OFF.CL1.4	1112111t	0x69E
CL_OFF.CL1.5	1112112t	0x4F4
CL_OFF.CL1.6	1112120t	0x4F5
CL_OFF.CL2.0	1112200t	0x4F8
CL_OFF.CL2.1	1112201t	0x4F9
CL_OFF.CL2.2	1112202t	0x4FA
CL_OFF.CL2.3	1112210t	0x4FB
CL_OFF.CL2.4	1112211t	0x69F

CL_OFF.CL2.5	1112212t	0x4FC
CL_OFF.CL2.6	1112220t	0x4FD

F.2 Ordered Sets Transmission Example

Figure F-1 shows an example of a CL0s_EXIT.AckLFPS Ordered Set as it is transmitted on each transmitter at the beginning of an RS-FEC block.

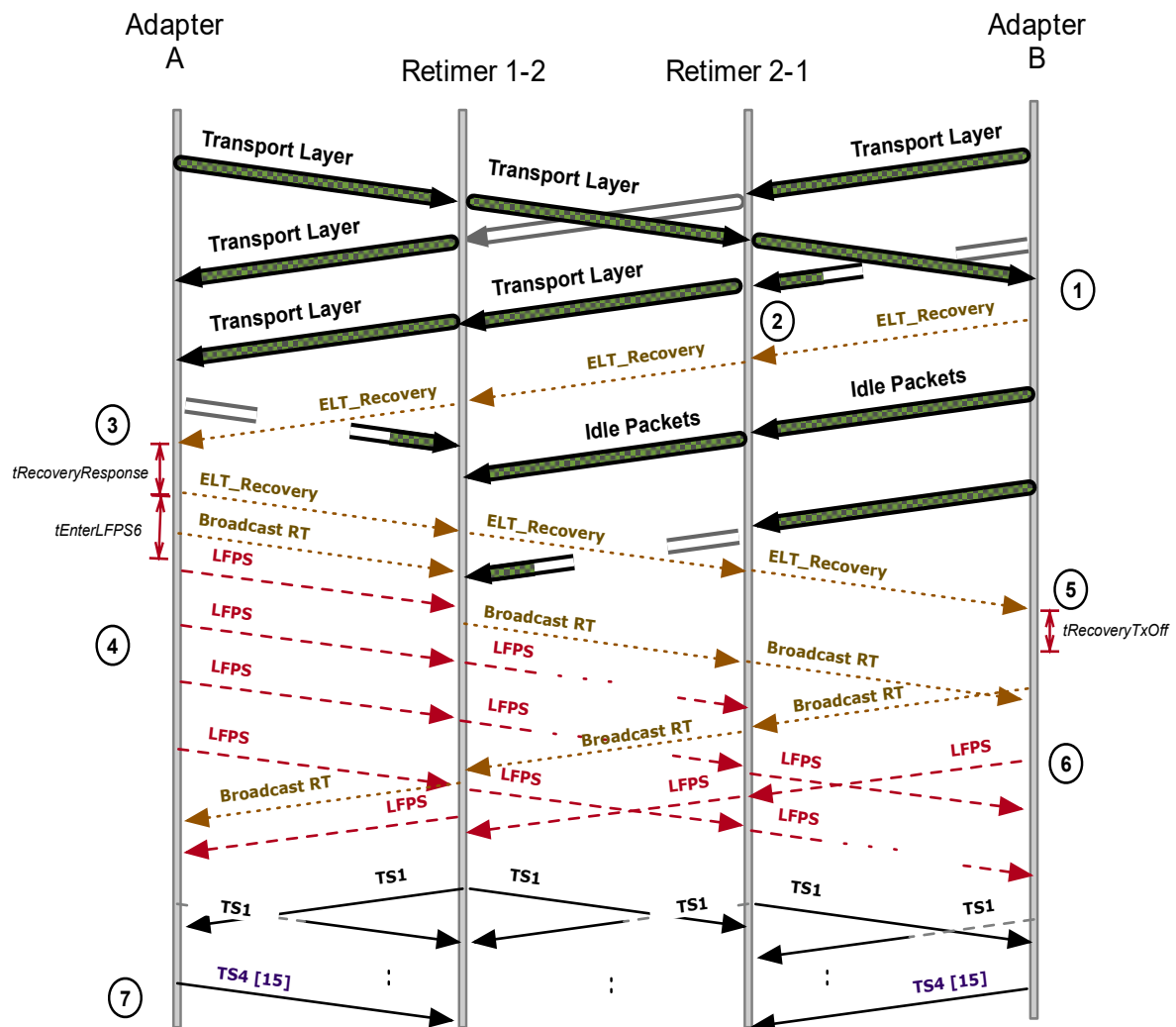
Figure F-1. CL0s_EXIT Ordered Set Example



The Ordered Set is transmitted from the most significant Control Symbol to the least significant Control Symbol. Within each Control Symbol, the most significant Trit is sent first on the wire.

On a Symmetric Link, the Ordered set is sent 12 times on each transmitter, so the following pattern is repeated in the first 672 trits of the RS-FEC block:

1112000 1112000 1112000 1112000 ...

G Gen 4 Link Recovery Example

1. Adapter B detects an error and initiates Gen 4 Link Recovery. It stops its receivers and sends an ELT_Recovery Transaction, sending the last bit within $t_{\text{RecoveryRxOff}}$ after the receivers have stopped. The transmitter continues to send Idle Packets.
1. ~~Adapter B detects an error and initiates Gen 4 Link Recovery. It sends an ELT_Recovery Transaction and stops its receiver within $t_{\text{RecoveryRxOff}}$ after sending the last bit of the ELT_Recovery Transaction. The transmitter continues to send Idle Packets.~~
2. Re-timer 2-1 receives the ELT_Recovery Transaction. In response, it turns off its transmitters towards Adapter B within $t_{\text{RecoveryTxOff}}$ after receiving the ELT_Recovery Transaction. High speed forwarding continues to Re-timer 1-2.
3. Adapter A receives an ELT_Recovery Transaction. It turns off its transmitter towards Re-timer 1-2 and sends an ELT_Recovery Transaction within $t_{\text{RecoveryResponse}}$ after receiving ~~the ELT_Recovery Transaction~~. ELT_Recovery Transaction is sent, with the last bit delivered within $t_{\text{RecoveryRxOff}}$ after the ~~The receivers~~ are ~~turned off within $t_{\text{RecoveryRxOff}}$ after sending the ELT_Recovery Transaction.~~
4. Adapter A starts Lane Initialization from Phase 4. After sending at least 2 Broadcast RT Transactions, it starts sending LFPS.
5. Adapter B receives an ELT_Recovery Transaction and turns off its transmitter towards Re-timer 2-1.
6. Adapter B starts Lane Initialization from Phase 4. After sending at least two Broadcast RT Transactions, it starts sending LFPS.

7. Since Adapter A is a Downstream Adapter, the Router sends a Notification Packet with Event Code LINK_RECOVERY on its Upstream Adapter, indicating the Adapter Number of Adapter A. The Connection Manager can then query any error status bits for Adapter A and Adapter B, and the status of any Protocol Adapters that are using the Link.